MOS Memory Data Book

1984

European Edition

Commercial and Military Specifications

SMYD002-EUR
0184-464PP-142M

TEXAS INSTRUMENTS

Printed in ITALY

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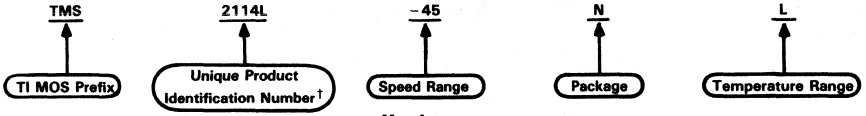
(Numbers in parenthesis indicate overall complexity.)

PART 1 – ALTERNATE VENDOR PART NUMBERING (EXAMPLES)

TEXAS INSTRUMENTS (TI)

EXAMPLE:



TMS Commercial MOS
SMJ Military MOS

Max Access

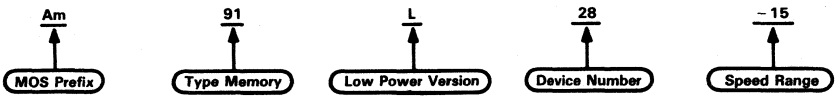
– 4	45 ns	–20	200 ns
– 5	55 ns	–25	250 ns
– 7	70 ns	–30	300 ns
–10	100 ns	–35	350 ns
–12	120 ns	–45	450 ns
–15	150 ns		

FP Plastic Chip Carrier
J Cerpak/Cerdip
JD Side Braze
MC Chip-on-Board
N Plastic DIP

E –40°C to 80°C
L 0°C to 70°C
M –55°C to 125°C
S –55°C to 100°C

† Inclusion of an "L" in the product identification indicates the device operates at low power.

ADVANCED MICRO DEVICES (AMD)

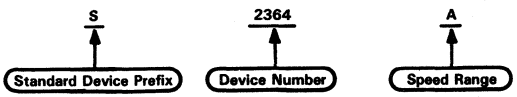


90 DRAM
91 SRAM
92 ROM
17/27 EPROM

Max Access

–70	70 ns
–10	100 ns
–15	150 ns
–20	200 ns

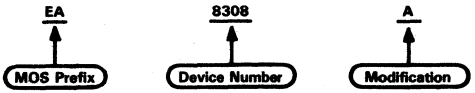
AMERICAN MICROSYSTEMS, INC. (AMI)



Max Access

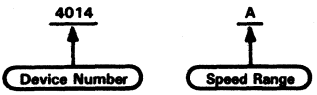
A 350 ns
B 250 ns

ELECTRONIC ARRAYS, INC. (EA)



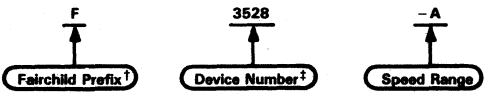
27XX EPROM
Other ROM

EMM/SEMI



Max Access
A Slow
B Fast

FAIRCHILD



Max Access
-1 (or A) Slowest
-2 (or B)
-3
-4
-5 Fastest

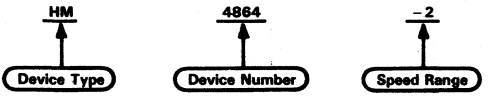
† May be omitted.
‡ Inclusion of an "L" indicates low power version.

FUJITSU

MB Fujitsu
MBM Industry Standard Prefix

Max Access	
-10	100 ns
-12	120 ns
-15	150 ns

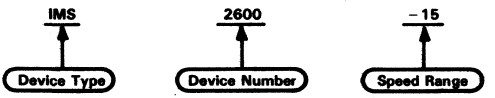
HITACHI



HM RAM
HN ROM

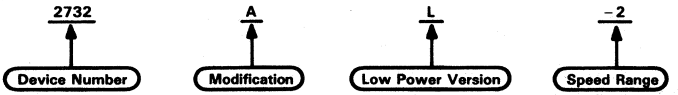
Max Access	
-1	Fastest
-2	
-3	
-4	Slowest

INMOS



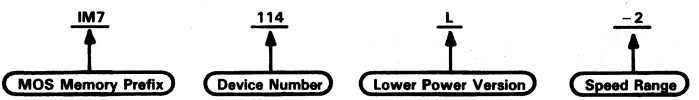
Max Access	
-45	45 ns
-55	55 ns
-10	100 ns
-12	120 ns
-15	150 ns

INTEL



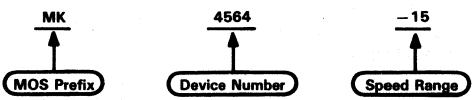
Max Access
-1 Fastest
-2
-3
-4
-5
-6 Slowest

INTERSIL/AMS



Max Access
-1 (-11) Fastest
-2 (-12)
-3
-4 Slowest

MOSTEK

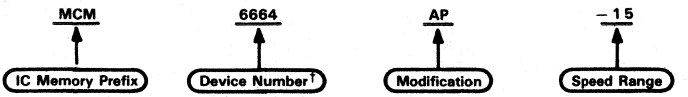


Max Access

-55 55 ns	- 4 250 ns
-70 70 ns	- 5 300 ns
-90 90 ns	- 6 350 ns
- 1 120 ns	-15 150 ns‡
- 2 150 ns	-20 200 ns‡
- 3 200 ns†	-25 250 ns‡

† 550 ns for SRAMs and ROMs
‡ DRAMs

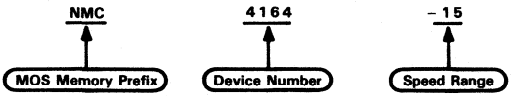
MOTOROLA



Max Access	
–10	100 ns
–12	120 ns
–15	150 ns
–20	200 ns
–25	250 ns
–30	300 ns
–45	450 ns

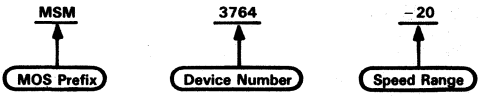
† Inclusion of an "L" indicates low power version.

NATIONAL SEMICONDUCTOR



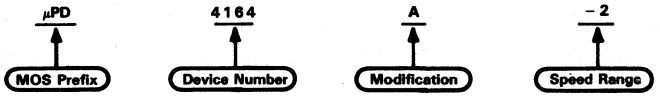
Max Access	
–12	120 ns
–15	150 ns
–20	200 ns

OKI SEMICONDUCTOR (OKI)



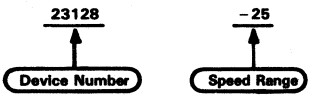
Max Access	
–12	120 ns
–15	150 ns
–20	200 ns

NIPPON ELECTRIC CORPORATION (NEC)



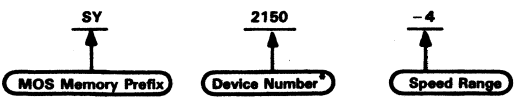
Max Access	
-0	200 ns
-1	250 ns
-2	100 ns
-3	150 ns

SIGNETICS



Max Access	
-20	200 ns
-25	250 ns
-30	300 ns
-45	450 ns

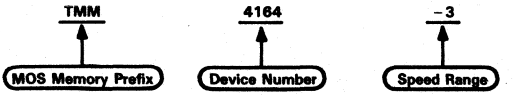
SYNERTEK



Max Access	
-2	200 ns
-3	300 ns
-4	45 ns
-5	55 ns

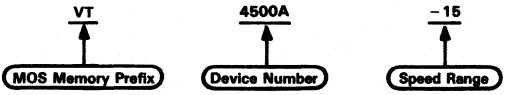
*Inclusion of an alpha character indicates a device modification.

TOSHIBA



Max Access
-1 Fastest
-2
-3
-4
-5 Slowest

VLSI TECHNOLOGY



Max Access
-15 150 ns
-20 200 ns
-25 250 ns

PART II – SECOND SOURCES*

*Based on available published data. (Official second sourcing agreements not necessarily implied.)
All devices listed operate over the 0°C to 70°C temperature range.

DYNAMIC RAMS

ORGANIZATION	MAX ACCESS	VENDOR		PART NUMBER
		TI	SECOND SOURCES	
16K × 1	Max Access = 250 ns	TI		TMS4116
(3 Supply)			AMD	Am9016
			Fairchild	F4116
			Fujitsu	MB8116
			Hitachi	HM4716A
			Intersil	IM4116
			ITT	ITT4116
			Mitsubishi	M5K4116
			Mostek	MK4116
			Motorola	MCM4116B
			National	MM5290
			NEC	μPD416
			Toshiba	TMM416
64K × 1	Max Access = 200 ns	TI		TMS4164†
(5 V)			Fairchild	F4164
			Fujitsu	MB8264A
			Hitachi	HM4864
			INMOS	IMS2600†
			Intel	2164
			Micron Tech.	MT4264†
			Mitsubishi	M5K4164
			Mostek	MK4564
			Motorola	MCM6665
			National	NMC4164†
			NEC	μPD4164
			OKI	MSM3764
			Toshiba	TMM4164
16K × 4	Max Access = 200 ns	TI		TMS4416
(5 V)			Fujitsu	MB81416
			Hitachi	HM48416AP
			INMOS	IMS2620
256K × 1	Max Access = 200 ns	TI		TMS4256/TMS4257
(5 V)			Fujitsu	MB81257/MB81256
			Hitachi	HM50257
			Mitsubishi	MSM4256
			Motorola	MCM6256
			NEC	μPD41256/μPD41257
			OKI	MSM37256
			Toshiba	TMM41256
			Western Electric	WCM41256

†These devices have a 256 cycle, 4 ms refresh scheme. All others refresh in 2 ms.

STATIC RAMS

ORGANIZATION	MAX ACCESS	VENDOR		PART NUMBER
		TI	SECOND SOURCES	
4K × 1	Max Access = 450 ns	TI		TMS4044/TMS40L44
(5 V)			AMD	Am4044
			Intersil	IM7141/IM7141L
			Intel	2141/2141L
			National SC	MM2141
			Mitsubishi	M5T4044
			Mostek	MK4104
			NEC	μPD4104
			Synertek	SY2141/SY2141L
1K × 4	Max Access = 450 ns	TI		TMS2114/TMS2114L
(5 V)			AMD	Am9114E/91L14E
			EA	EA2114L
			EMM/SEMI	2114
			Fairchild	2114
			Hitachi	HM472114A
			Intel	2114A/2114AL
			Mitsubishi	M5L2114L
			Motorola	MCM2114/MCM21L14
			National SC	MM2114/MM21L14
			NEC	μPD2114/μPD2114L
			OKI	MSM2114/MSM2114L
			Synertek	SY2114/SY2114A
2K × 8	Max Access = 250 ns	TI		TMS4016
(5 V)			Fairchild	F3528
			Fujitsu	MB8128
			Mitsubishi	M58725
			Mostek	MK4802
			OKI	MSM2128
			Toshiba	TMM2016

INTERCHANGEABILITY GUIDE

EPROMS

ORGANIZATION	MAX ACCESS	VENDOR		PART NUMBER
		TI	SECOND SOURCES	
1K × 8	Max Access = 450 ns	TI		TMS2708/TMS27L08
(3 Supply)			AMD	2708
			Fairchild	F2708
			Fujitsu	MB8518
			Intel	2708/2708L
			Motorola	MCM2708
			National SC	MM2708
			OKI	MSM2708
2K × 8	Max Access = 450 ns	TI		TMS2716
(3 Supply)			Motorola	TMS2716/TMS27A16
2K × 8	Max Access = 450 ns	TI		TMS2516
(5 V)			AMD	2716
			Fujitsu	MBM2716
			Hitachi	HN462716
			Intel	2716
			Mitsubishi	M5L2716
			Mostek	MK2716
			Motorola	MCM2716/MCM27L16
			National	MM2716
			NEC	μPD2716
			OKI	MSM2716
			Toshiba	TMM323
4K × 8	Max Access = 450 ns	TI		TMS2532
(5 V)			Hitachi	HN62532
			Motorola	MCM2532/MCM25L32
			National	MM2532
4K × 8	Max Access = 450 ns	TI		TMS2732A
(5 V)			AMD	Am2732
			Fairchild	F2732
			Fujitsu	MBM2732A
			Hitachi	HN462732
			Intel	2732A
			Mitsubishi	M5L2732
			NEC	μPD2732
			OKI	MSM2732
			Toshiba	TMM2732
8K × 8	Max Access = 450 ns	TI		TMS2564
(5 V)			Motorola	MCM68764
8K × 8	Max Access = 450 ns	TI		TMS2764
(5 V)			AMD	Am2764
			Fairchild	2764
			Fujitsu	MBM2764
			Hitachi	HN482764
			Intel	2764
			Mitsubishi	M5L2764
			OKI	MSM2764A
16K × 8	Max Access = 250 ns	TI		TMS27128
(5 V)			Fujitsu	MBM27128
			Intel	27128

PART I – GENERAL CONCEPTS AND TYPES OF MEMORIES

Address – Any given memory location in which data can be stored or from which it can be retrieved.

Automatic Chip-Select/Power Down – (see Chip Enable Input)

Bit – Contraction of Binary digIT, i.e., a 1 or a 0; in electrical terms the value of a bit may be represented by the presence or absence of charge, voltage, or current.

Byte – A word of 8 bits (see word)

Chip Enable Input – A control input to an integrated circuit that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced power standby mode.

Chip Select Input – Chip select inputs are gating inputs that control the input to and output from the memory. They may be of two kinds:

1. Synchronous – Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
2. Asynchronous – Has direct asynchronous control of inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Column Address Strobe (CAS) – A clock used in dynamic RAMs to control the input of column addresses. It can be active high (CAS) or active low ($\overline{\text{CAS}}$).

Data – Any information stored or retrieved from a memory device.

Dynamic (Read/Write) Memory (DRAM) – A read/write memory in which the cells require the repetitive application of control signals in order to retain the stored data.

NOTES:
1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

Electrically Alterable Read-Only Memory (EAROM) – A nonvolatile memory that can be field-programmed like a PROM or EPROM, but that can be electrically erased by a combination of electrical signals at its inputs.

Erasable and Programmable Read-Only Memory (EPROM)/Reprogrammable Read-Only Memory – A field-programmable read-only memory that can have the data content of each memory cell altered more than once.

Erase – Typically associated with EPROMs and EAROMs. The procedure whereby programmed data is removed and the device returns to its unprogrammed state.

Field-Programmable Read-Only Memory – A read-only memory that after being manufactured, can have the data content of each memory cell altered.

Fixed Memory – A common term for ROMs, EPROMs, EAROMs, etc., containing data that is not normally changed. A more precise term for EPROMs and EAROMs is nonvolatile since their data may be easily changed.

Fully Static RAM – In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need for clocks. There is no precharge required for static periphery.

K – When used in the context of specifying a given number of bits of information, $1K = 2^{10} = 1024$ bits. Thus, $64K = 64 \times 1024 = 65{,}536$ bits.

Large-Scale Integration (LSI) – The description of any IC technology that enables condensing more than 100 gates onto a single chip.

Mask-Programmed Read-Only Memory — A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory — A medium capable of storage of information from which the information can be retrieved.

Memory Cell — The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Metal-Oxide Semiconductor (MOS) — The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

NMOS — A type of MOS technology in which the basic conduction mechanism is governed by electrons. (Short for N-channel MOS)

Nonvolatile Memory — A memory in which the data content is maintained whether the power supply is connected or not.

Output Enable — A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select)

PMOS — A type of MOS technology in which the basic conduction mechanism is governed by holes. (Short for P-channel MOS)

Parallel Access — A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

Power Down — A mode of a memory device during which the device is operating in a low-power or standby mode. Normally read or write operations of the memory are not possible under this condition.

Program — Typically associated with EPROM memories, the procedure whereby logical 0's (or 1's) are stored into various desired locations in a previously erased device.

Program Enable — An input signal that when true, puts a programmable memory device into the program mode.

Programmable Read-Only Memory (PROM) — A memory that permits access to any of its address locations in any desired sequence with similar access time to each location.
NOTE: The term as commonly used denotes a read/write memory.

Read — A memory operation whereby data is output from a desired address location.

Read-Only Memory (ROM) — A memory in which the contents are not intended to be altered during normal operation.
NOTE: Unless otherwise qualified, the term "read-only memory" implies that the content is determined by its structure and is unalterable.

Read/Write Memory — A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electrical input signals.

Row Address Strobe (RAS) — A clock used in dynamic RAMs to control the input of the row addressed. It can be active high (RAS) or active low ($\overline{\text{RAS}}$).

Scaled-MOS (SMOS) — MOS technology under which the device is scaled down in size in three dimensions and in operating voltages allowing improved performance.

Semi-Static (Quasi-Static, Pseudo-Static) RAM — In a semi-static RAM, the periphery is clock-activated (i.e., dynamic). Thus the periphery is inactive until clocked, and only one memory cycle is permitted per clock. The peripheral circuitry must be allowed to reset after each active memory cycle for a minimum precharge time. No refresh is required.

Serial Access — A feature of a memory by which all the bits are entered sequentially at a single input or retrieved sequentially form a single output.

Static RAM (SRAM) — A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMs.

Very-Large-Scale Integration (VLSI) — The description of any IC technology that is much more complex than large-scale integration (LSI), and involves a much higher equivalent gate count. At this time an exact definition including a minimum gate count has not been standardized by JEDEC or the IEEE.

Volatile Memory — A memory in which the data content is lost when power supplied is disconnected.

Word — A series of one or more bits that occupy a given address location and that can be stored and retrieved in parallel.

Write — A memory operation whereby data is written into a desired address location.

Write Enable — A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode.

PART II – OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

Capacitance

The inherent capacitance on every pin, which can vary with various inputs and outputs.

Example symbology:

C_i	Input capacitance
C_o	Output capacitance
$C_{i(D)}$	Input capacitance, data input

Current

High-level input current, I_{IH}
The current into an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current I_{BB}, I_{CC}, I_{DD}, I_{PP}
The current into, respectively, the V_{BB}, V_{CC}, V_{DD}, V_{PP} supply terminals.

Operating Free-Air Temperature

The temperature (T_A) range over which the device will operate and meet the specified electrical characteristics.

Operating Case Temperature

The case temperature (T_C) range over which the device will operate and meet the specified electrical characteristics.

* Current out of a terminal is given as a negative value.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Supply Voltages, V_{BB}, V_{CC}, V_{DD}, V_{PP}

The voltages supplied to the corresponding voltage pins that are required for the device to function. From one to four of these supplies may be necessary, along with ground, V_{SS}.

Time Intervals

New or revised data sheets in this book use letter symbols in accordance with standards recently adopted by JEDEC, the IEEE, and the IEC. Two basic forms are used. The first form is usually used in this book when intervals can easily be classified as access, cycle, disable, enable, hold, refresh, setup, transition, or valid times and for pulse durations. The second form can be used generally but in this book is used primarily for time intervals not easily classifiable. The second (unclassified) form will be described first. Since some manufacturers use this form for all time intervals, symbols in the unclassified form are given with the examples for most of the classified time intervals.

Unclassified time intervals

Generalized letter symbols can be used to identify almost any time interval without classifying it using traditional or contrived definitions. Symbols for unclassified time intervals identify two signal events listed in from-to sequence using the format:

$$t_{AB\text{-}CD}$$

Subscripts A and C indicate the names of the signals for which changes of state or level or establishment of state or level constitute signal events assumed to occur first and last, respectively, that is, at the beginning and end of the time interval. Every effort is made to keep the A and C subscript length down to one letter, if possible (e.g., R for $\overline{RAS}$ and C for $\overline{CAS}$ of TMS 4116).

Subscripts B and D indicate the direction of the transitions and/or the final states or levels of the signals represented by A and C, respectively. One or two of the following is used:

H = high or transition to high
L = low or transition to low
V = a valid steady-state level
X = unknown, changing, or "don't care" level
Z = high-impedance (off) state

The hyphen between the B and C subscripts is omitted when no confusion is likely to occur.

For examples of symbols of this type, see TMS 4116 (e.g., t_{PLCL})

Classified time intervals (general comments, specific times follow)

Because of the information contained in the definitions, frequently the identification of one or both of the two signal events that begin and end the intervals can be significantly shortened compared to the unclassified forms. For example, it is not necessary to indicate in the symbol that an access time ends with valid data at the output. However, if both signals are named (e.g., in a hold time), the from-to sequence is maintained.

Access time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

Example symbology:

Classified	Unclassified	Description
$t_{a(A)}$	t_{AVQV}	Access time from address
$t_{a(S)}$, $t_{a(CS)}$	t_{SLQV}	Access time from chip select (low)

Cycle time

The time interval between the start and end of a cycle.

NOTE: The cycle time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval that must be allowed for the digital circuit to perform a specified function (e.g., read, write, etc.) correctly.

Example symbology:

Classified	Unclassified	Description
$t_{c(R)}$, $t_{c(rd)}$	$t_{AVAV(R)}$	Read cycle time
$t_{c(W)}$	$t_{AVAV(W)}$	Write cycle time

NOTE: R is usually used as the abbreviation for "read"; however, in the case of dynamic memories, "rd" is used to permit R to stand for RAS.

Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Example symbology:

Classified	Unclassified	Description
$t_{dis(S)}$	t_{SHQZ}	Output disable time after chip select (high)
$t_{dis(W)}$	t_{WLQZ}	Output disable time after write enable (low)

These symbols supersede the older forms t_{PVZ} or t_{PXZ}.

Enable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

NOTE: For memories these intervals are often classified as access times.

Example symbology:

Classified	Unclassified	Description
$t_{en(SL)}$	t_{SLQV}	Output enable time after chip select low

These symbols supercede the older form t_{PZV}.

Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{h(D)}$	t_{WHDX}	Data hold time (after write high)
$t_{h(RHrd)}$	t_{RHWH}	Read (write enable high) hold time after $\overline{RAS}$ high)
$t_{h(CHrd)}$	t_{CHWH}	Read (write enable high) hold time after $\overline{CAS}$ high)
$t_{h(CLCA)}$	t_{CL-CAX}	Column address hold time after $\overline{CAS}$ low
$t_{h(RLCA)}$	t_{RL-CAX}	Column address hold time after $\overline{RAS}$ low
$t_{h(RA)}$	t_{RL-RAX}	Row address hold time (after $\overline{RAS}$ low)

These last three symbols supersede the older forms:

NEW FORM	OLD FORM
$t_{h(CLCA)}$	$t_{h(ACL)}$
$t_{h(RLCA)}$	$t_{h(ARL)}$
$t_{h(RA)}$	$t_{h(AR)}$

NOTE: The from-to sequence in the order of subscripts in the unclassified form is maintained in the classified form. In the case of hold times, this causes the order to seem reversed from what would be suggested by the terms.

Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Example symnbology:

Classified	Unclassified	Description
$t_{w(W)}$	t_{WLWH}	Write pulse duration
$t_{w(RL)}$	t_{RLRH}	Pulse duration, $\overline{RAS}$ low

Refresh time interval

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE: The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
t_{rf}		Refresh time interval

Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

Example symbology:

Classified	Unclassified	Description
$t_{su(D)}$	t_{DVWH}	Data setup time (before write high)
$t_{su(CA)}$	t_{CAV-CL}	Column address setup time (before $\overline{CAS}$ low)
$t_{su(RA)}$	t_{RAV-RL}	Row address setup time (before $\overline{RAS}$ low)

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Example symbology:

Classified	Unclassified	Description
t_t		Transition time (general)
$t_{t(CH)}$	t_{CHCH}	Low-to-high transition time of $\overline{CAS}$
$t_{r(C)}$	t_{CHCH}	$\overline{CAS}$ rise time
$t_{f(C)}$	t_{CLCL}	$\overline{CAS}$ fall time

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

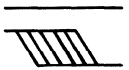
The time interval in which output data contines to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Example symbology:

Classified	Unclassified	Description
$t_{v(A)}$	t_{AXQX}	Output data valid time after change of address.

This supersedes the older form t_{PVX}.

PART III – TIMING DIAGRAMS CONVENTIONS

TIMING DIAGRAM SYMBOL	MEANING	
	INPUT FORCING FUNCTIONS	OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low some time during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Centerline represents high-impedance (off) state.

PART IV – BASIC DATA SHEET STRUCTURE

The front page of the data sheet begins with a list of key *features* such as organization, interface, compatibility, operation (static or dynamic), access and cycle times, technology (N or P channel, silicon or metal oxide gate), and power. In addition, the top view of the device is shown with the *pinout* provided. Next a general *description* of the device, system interface considerations, and elaboration on other device chracteristics are presented. The next section is an explanation of the device's *operation* which includes the function of each pin (i.e., the relationship between each input (output) and a given type of memory). The functions basically involve starting, achieving, and ending a given type of memory cycle (e.g., programming or erasing EPROMs, or reading a memory location).

Augmenting the descriptive text there appears a *logic symbol* prepared in accordance with forthcoming IEEE and IEC standards and explained in the section of this book following this one. Following the symbol is usually a *functional block diagram,* a flow chart of the basic internal structure of the device showing the signal paths for data, addresses, and control signals, as well as the internal architecture. Usually the next few pages contain the absolute maximum ratings (e.g., voltage supplies, input voltage, and temperature) applicable over the *operating free-air temperature range.* If the device is used outside of these values, it may be permanently destroyed or at least it would not function as intended. Next, typically, are the *recommended operating conditions* (e.g., supply voltages, input voltages, and operating temperature). The memory device is guaranteed to work reliably and to meet all data sheet parameters when operated in accord with the recommended operating conditions and within the specified timing. If the device is operated outside of these limits (minimum/maximum), the device's operation is no longer guaranteed to meet the data sheet parameters. Operation beyond the absolute maximum ratings as just described can result in catastrophic failures.

The next section provides a table of *electrical characteristics over full ranges of recommended operating conditions* (e.g., input and output currents, output voltages, etc.). These are presented as minimum, typical, and maximum values. Typical values are representative of operation at an ambient temperature of T_A = 25°C with all power supply voltages at nominal value. Next, input and output capacitances are presented. Each pin has a capacitance (whether an input, an output, or control pin). Minimum capacitances are not given, as the typical and maximum values are the most crucial.

The next few tables involve the device timing characteristics. The parameters are presented as minimum, typical (or nominal), and maximum. The *timing requirements over recommended supply voltage range and operating free-air temperature* indicate the device control requirements such as hold times, setup times, and transition times. These values are referenced to the relative positioning of signals on the timing diagrams, which follow. The *switching characteristics over recommended supply voltage range* are device performance characteristics inherent to device

operation once the inputs are applied. These parameters are guaranteed for the test conditions given. The interrelationship of the timing requirements to the switching characteristics is illustrated in *timing diagrams* for each type of memory cycle (e.g., read, write, program).

At the end of a data sheet additional *applications information* may be provided such as how to use the device, graphs of electrical characteristics, or other data on electrical characteristics.

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is available from Texas Instruments in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

Please contact

Texas Instruments
P.O. Box 401560
Dallas, Texas 75240

to obtain this brochure.

TMS4116
16,384-BIT DYNAMIC RANDOM-ACCESS MEMORY

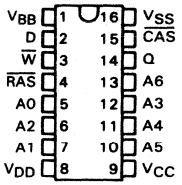
OCTOBER 1977 – REVISED MAY 1982

- **16,384 X 1 Organization**
- **10% Tolerance on All Supplies**
- **All Inputs Including Clocks TTL-Compatible**
- **Unlatched Three-State Fully TTL-Compatible Output**
- **3 Performance Ranges:**

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY-WRITE† CYCLE (MIN)
TMS4116-15	150 ns	100 ns	375 ns	375 ns
TMS4116-20	200 ns	135 ns	375 ns	375 ns
TMS4116-25	250 ns	165 ns	410 ns	515 ns

- **Page-Mode Operation for Faster Access Time**
- **Common I/O Capability with "Early Write" Feature**
- **Low-Power Dissipation**
  - **Operating 462 mW (Max)**
  - **Standby 20 mW (Max)**
- **1-T Cell Design, N-Channel Silicon-Gate Technology**
- **16-Pin 300-Mil (7.62 mm) Package Configuration**

TMS4116 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A6	Addresses
$\overline{CAS}$	Column Address Strobe
D	Data Input
Q	Data Output
$\overline{RAS}$	Row Address Strobe
V_{BB}	−5-V Power Supply
V_{CC}	+5-V Power Supply
V_{DD}	+12-V Power Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4116 series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories organized as 16,384 one-bit words, and employs single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe $\overline{RAS}$ (or $\overline{R}$) and Column Address Strobe $\overline{CAS}$ (or $\overline{C}$). All address lines (A0 through A6) and data in (D) are latched on chip to simplify system design. Data out (Q) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 350 milliwatts active and 6 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 10 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS4116 series is offered in a 16-pin dual-in-line plastic (NL suffix) package and is guaranteed for operation from 0°C to 70°C. Package is designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers.

† The term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".

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operation

address (A0 through A6)

Fourteen address bits are required to decode 1 of 16,384 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address trobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle, the output goes active after the enable time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 128 row addresses (A0 through A6) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

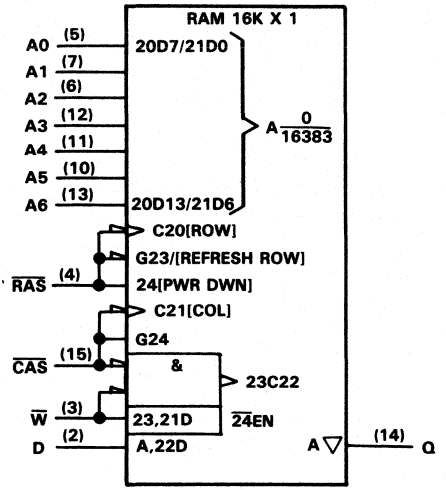
page-mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses on the same page is eliminated. To extend beyond the 128 column locations on a single RAM, the row address and $\overline{RAS}$ is applied to multiple 16K RAMs; $\overline{CAS}$ is decoded to select the proper RAM.

power-up

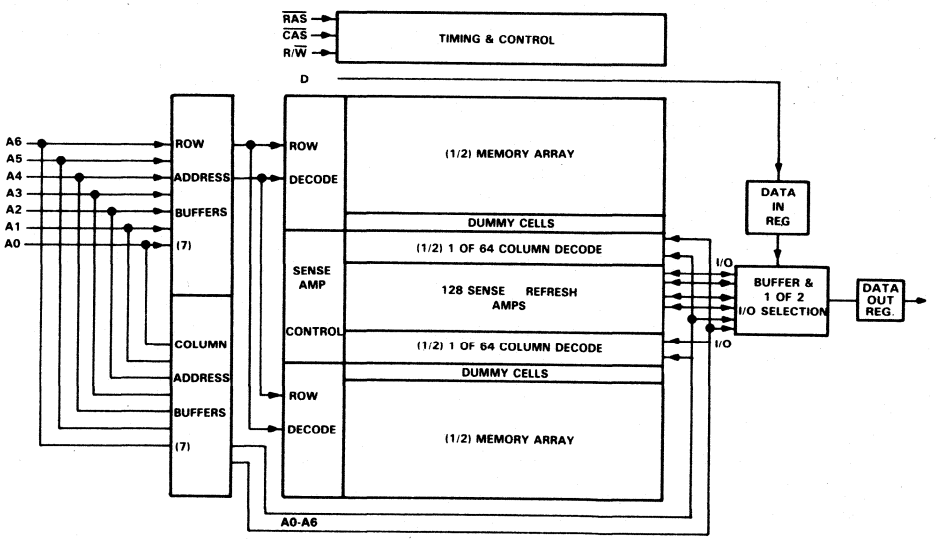
V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applies to system use, where failure of the V_{BB} supply must immediately shut down the other supplies. After power up, eight $\overline{RAS}$ cycles must be performed to achieve proper device operation.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin (see Note 1)	−0.5 V to 20 V
Voltage on V_{CC}, V_{DD} supplies with respect to V_{SS}	−1 V to 15 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}		−4.5	−5	−5.5	V
Supply voltage, V_{CC}		4.5	5	5.5	V
Supply voltage, V_{DD}		10.8	12	13.2	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}	All inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7	
Low-level input voltage, V_{IL} (see Note 2)		−1	0	0.8	V
Operating free-air temperature, T_A		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 7 V, All other pins = 0 V except V_{BB} = −5 V			10	μA
I_O	Output current (leakage)	V_O = 0 to 5.5 V, $\overline{CAS}$ high			±10	μA
I_{BB1}	Average operating current during read or write cycle	Minimum cycle time		50	200	μA
I_{CC1}‡					4§	mA
I_{DD1}				27	35	mA
I_{BB2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		10	100	μA
I_{CC2}					±10	μA
I_{DD2}				0.5	1.5	mA
I_{BB3}	Average refresh current	Minimum cycle time, $\overline{RAS}$ cycling, $\overline{CAS}$ high		50	200	μA
I_{CC3}					±10	μA
I_{DD3}				20	27	mA
I_{BB4}	Average page-mode current	Minimum cycle time, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50	200	μA
I_{CC4}‡					4§	mA
I_{DD4}				20	27	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ V_{CC} is applied only to the output buffer, so I_{CC} depends on output loading.
§ Output loading two standard TTL loads.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	7	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

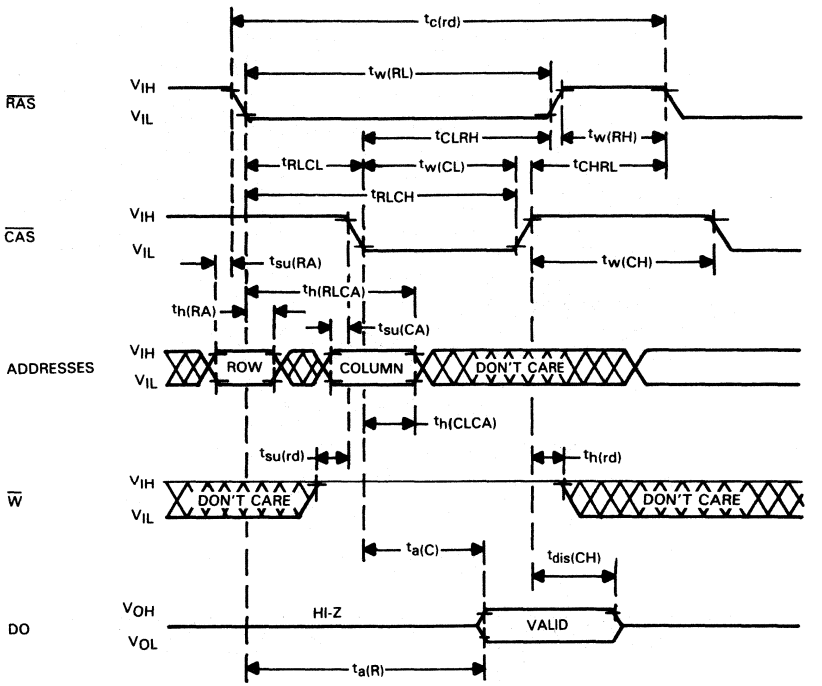
PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4116-15		TMS4116-20		TMS4116-25		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series, 74 TTL gates	t_{CAC}		100		135		165	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series, 74 TTL gates	t_{RAC}		150		200		250	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	50	0	60	ns

† All typical values are at T_A = 25°C and nominal supply voltages.

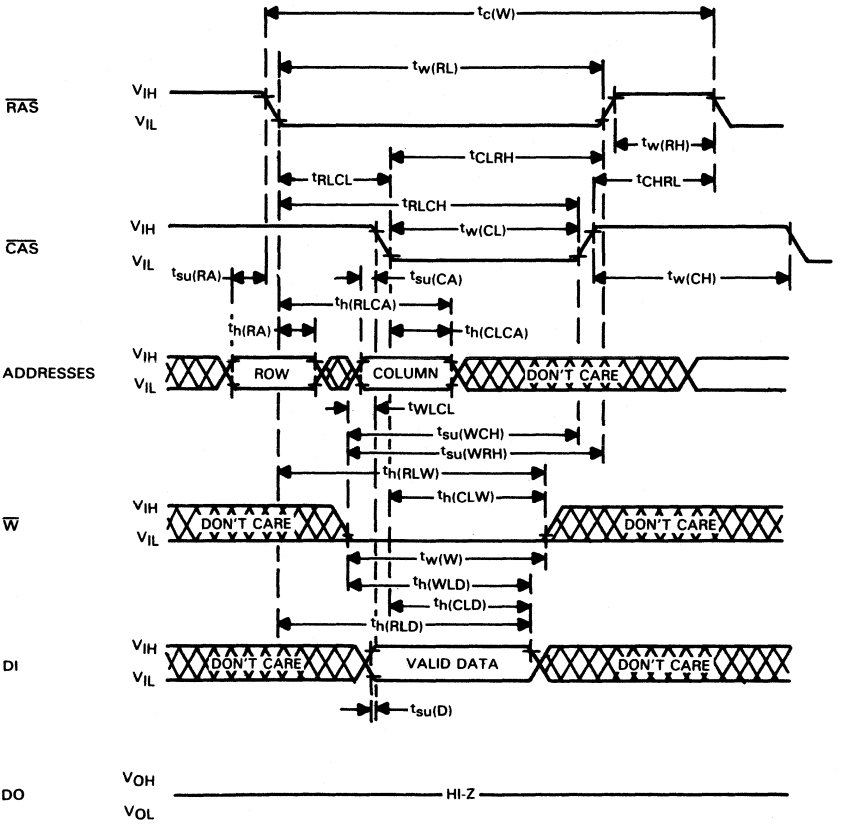
timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4116-15		TMS4116-20		TMS4116-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	170		225		275		ns
$t_{c(rd)}$	Read cycle time	t_{RC}	375		375		410		ns
$t_{c(W)}$	Write cycle time	t_{WC}	375		375		410		ns
$t_{c(rdW)}$	Read, modify-write cycle time	t_{RWC}	375		375		515		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)	t_{CP}	60		80		100		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low	t_{CAS}	100	10,000	135	10,000	165	10,000	ns
$t_{w(RH)}$	Pulse width $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		150		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low	t_{RAS}	150	10,000	200	10,000	250	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	45		55		75		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	35	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	−10		−10		−10		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		100		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		100		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		75		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	20		25		35		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	95		120		160		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		75		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		120		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		75		ns
$t_{h(rd)}$	Read command hold time	t_{RCH}	0		0		0		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		75		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		250		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	−20		−20		−20		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		165		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)	t_{CWD}	70		95		125		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	25	65	35	85	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)	t_{RWD}	120		160		200		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−20		−20		−20		ns
t_{rf}	Refresh time interval	t_{REF}		2		2		2	ms

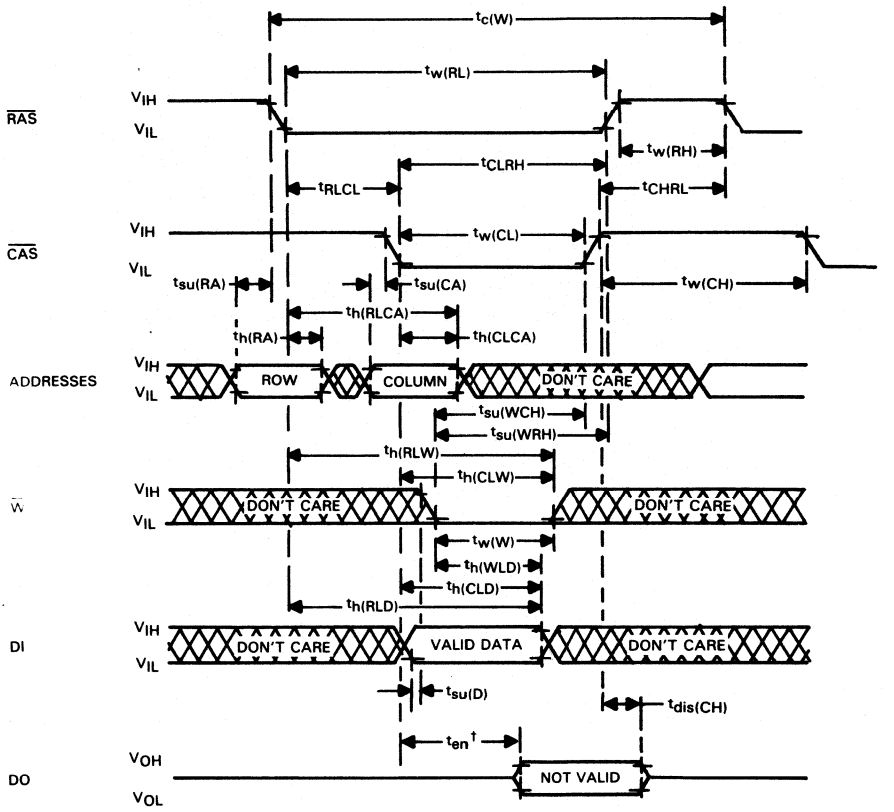
read cycle timing



early write cycle timing

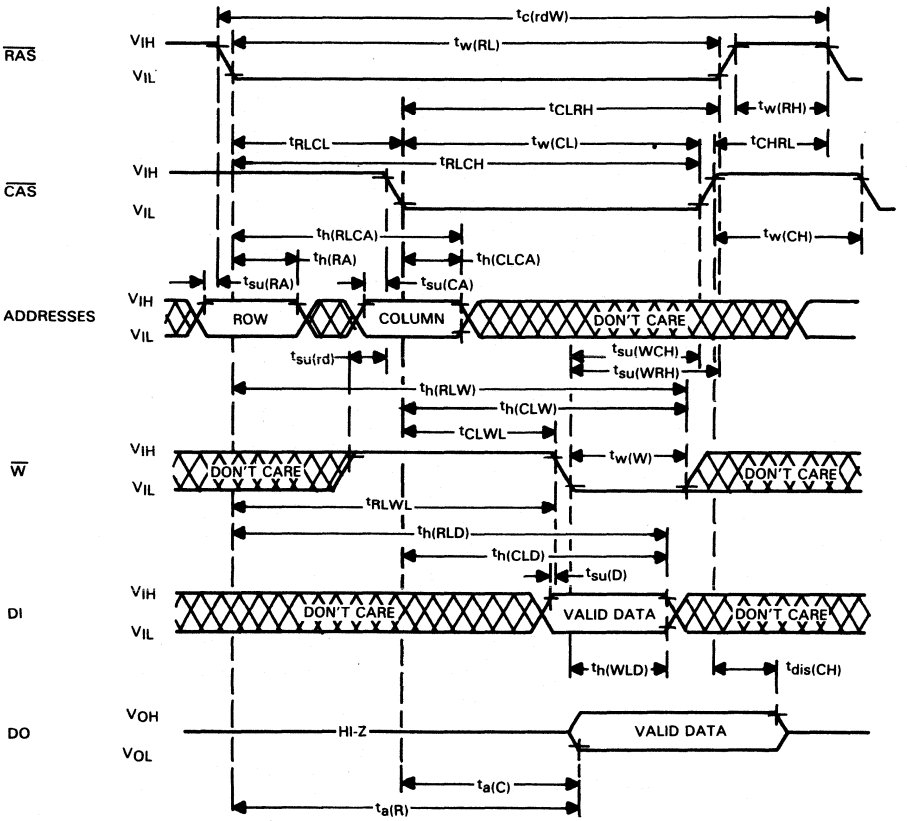


write cycle timing

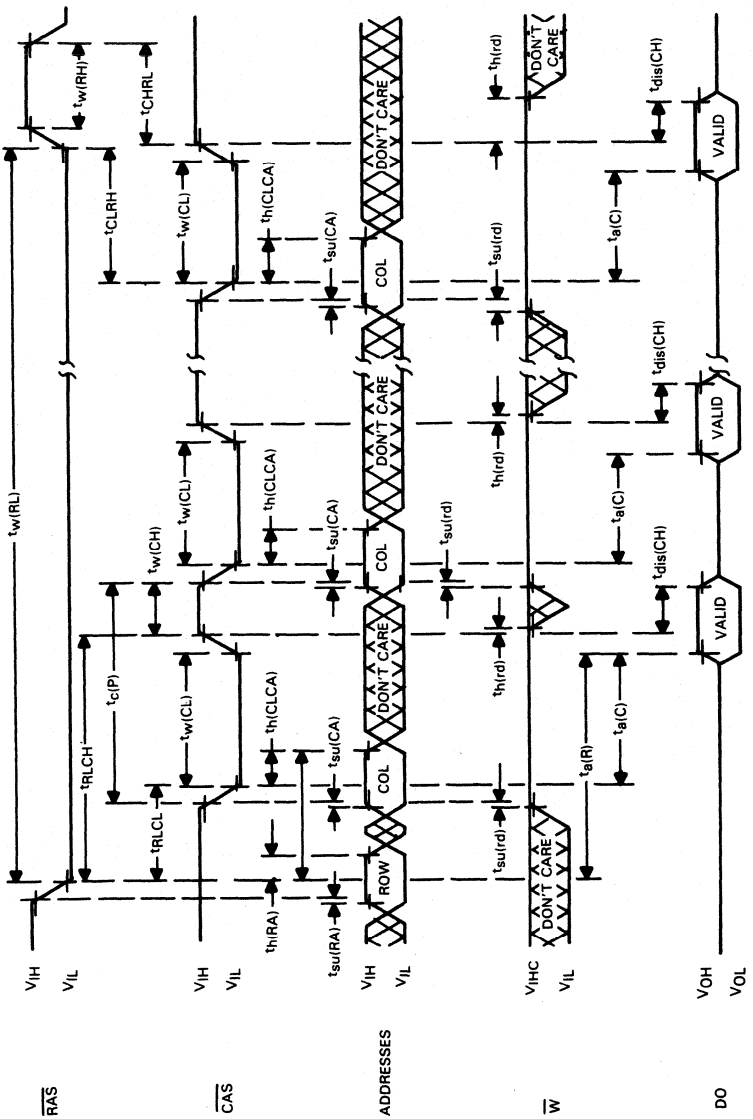


† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

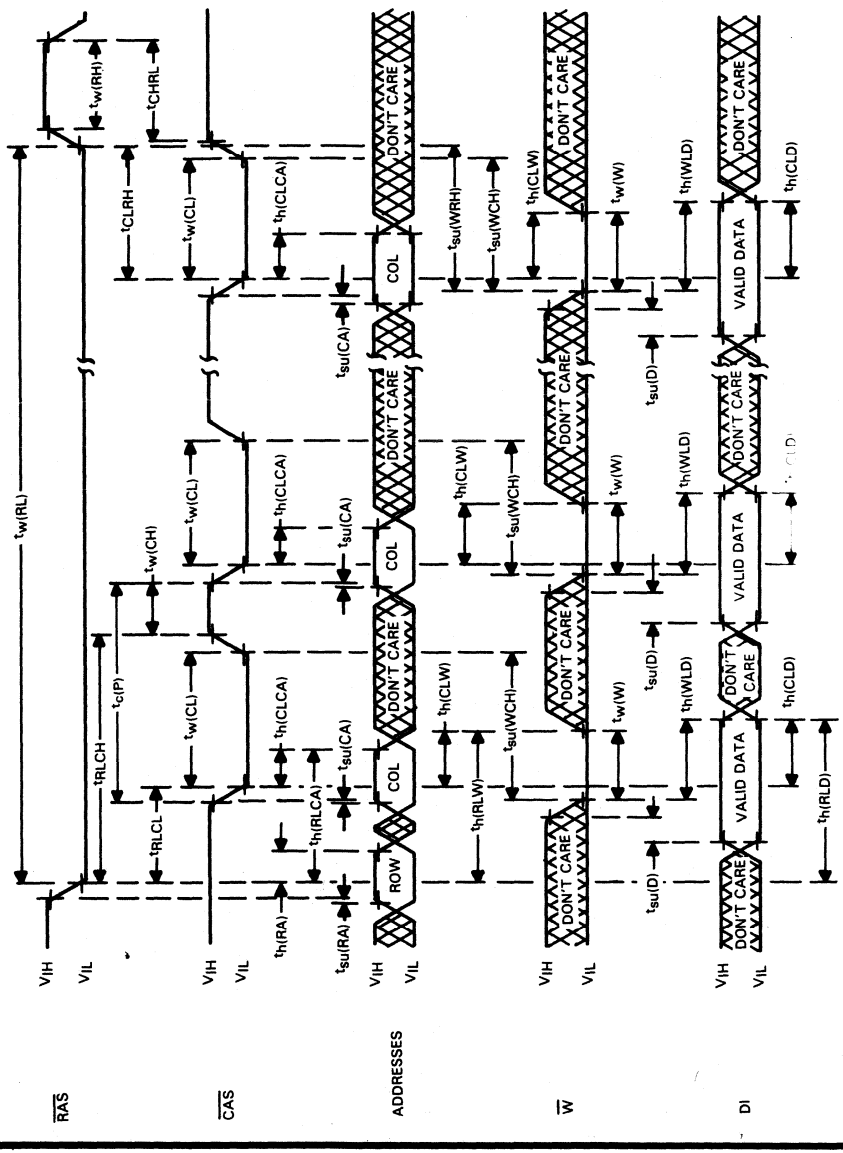
read-write/read-modify-write cycle timing



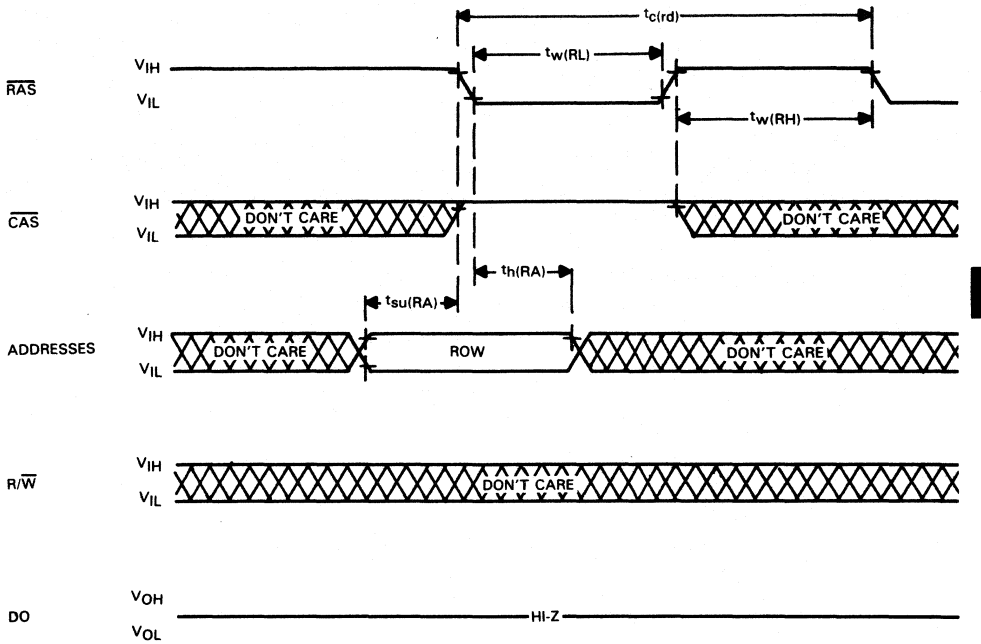
page-mode read cycle timing



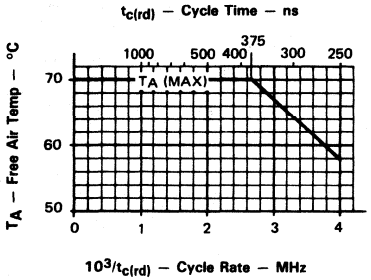
page-mode write cycle timing



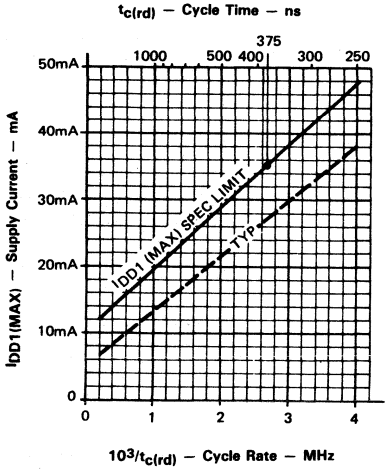
$\overline{\text{RAS}}$-only refresh timing



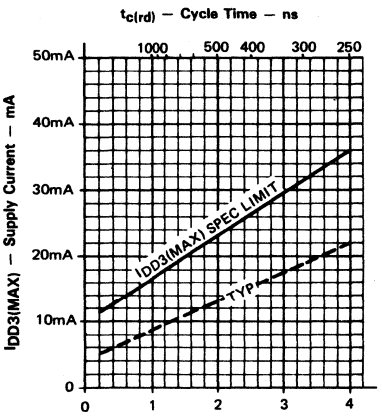
CYCLE RATE (& TIME) VS TEMPERATURE



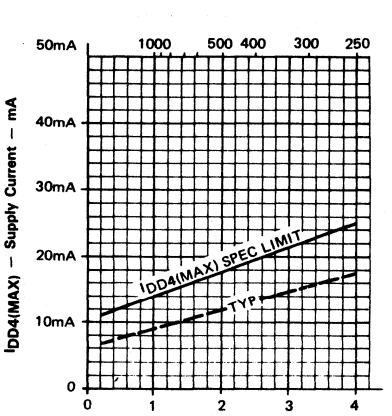
CYCLE RATE (& TIME) VS MAX SUPPLY CURRENT, I_{DD1}



CYCLE RATE (& TIME) VS MAX SUPPLY CURRENT, I_{DD3}



PAGE-MODE CYCLE RATE (& TIME) VS MAX SUPPLY CURRENT, I_{DD4}



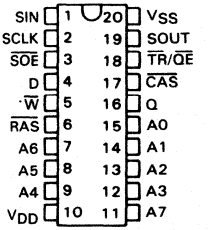
Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS4161
65,536-BIT MULTIPORT MEMORY

JULY 1983

- Dual Accessability – One Port Sequential Access, One Port Random Access
- Four Cascaded 64-Bit Serial Shift Registers for Sequential Access Applications
- Shift Register Loaded Once Every 64, 128, 192, or 256 Shift Cycles as Desired by User
- Fast Serial Port . . . 25 MHz Shift Rate
- $\overline{TR}/\overline{QE}$ as Output Enable Allows Direct Connection of D, Q and Address Lines to Simplify System Design
- Random Access Port Looks Exactly Like a TMS4164
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- 65,536 × 1 Organization
- Maximum Access Time from $\overline{RAS}$ Less Than 150 ns
- Minimum Cycle Time (Read or Write) Less Than 260 ns
- Long Refresh Period . . . 4 Milliseconds
- Low Refresh Overhead Time . . . As Low As 1.6% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs for Both Random and Serial Access
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation (TMS4161-15)
  - Operating . . . 175 mW (Typical)
  - Standby . . . 40 mW (Typical)
- New SMOS (Scaled-MOS) N-Channel Technology
- $\overline{SOE}$ Simplifies Multiplexing of Video Data Streams

TMS4161 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Random Access Data-In
Q	Random Access Data-Out
$\overline{RAS}$	Row Address Strobe
SCLK	Serial Data Clock
SIN	Serial Data-In
$\overline{SOE}$	Serial Output Enable
SOUT	Serial Data-Out
$\overline{TR}/\overline{QE}$	Register Transfer/Q Output Enable
$\overline{W}$	Write Enable
V_{DD}	+5-V Supply
V_{SS}	Ground

- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges in the Future

description

The TMS4161 is a high-speed, dual-access 65,536-bit dynamic random-access memory. The random-access port makes the memory look like it is organized as 65,536 words of one bit each like the TMS4164. The sequential access port is interfaced to an internal 256-bit dynamic shift register organized as four 64-bit shift registers which makes the memory look like it is organized as up to 256 words of up to 256 bits each which are accessed serially. One,

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two, three, or four 64-bit shift registers can be sequentially read out depending on a two-bit code applied to the two most significant column address inputs. The TMS4161 employs state-of-the-art SMOS (Scaled-MOS) N-channel double level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS4161 features full asynchronous dual access capability except when transferring data between the shift register and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift register also refreshes that row.

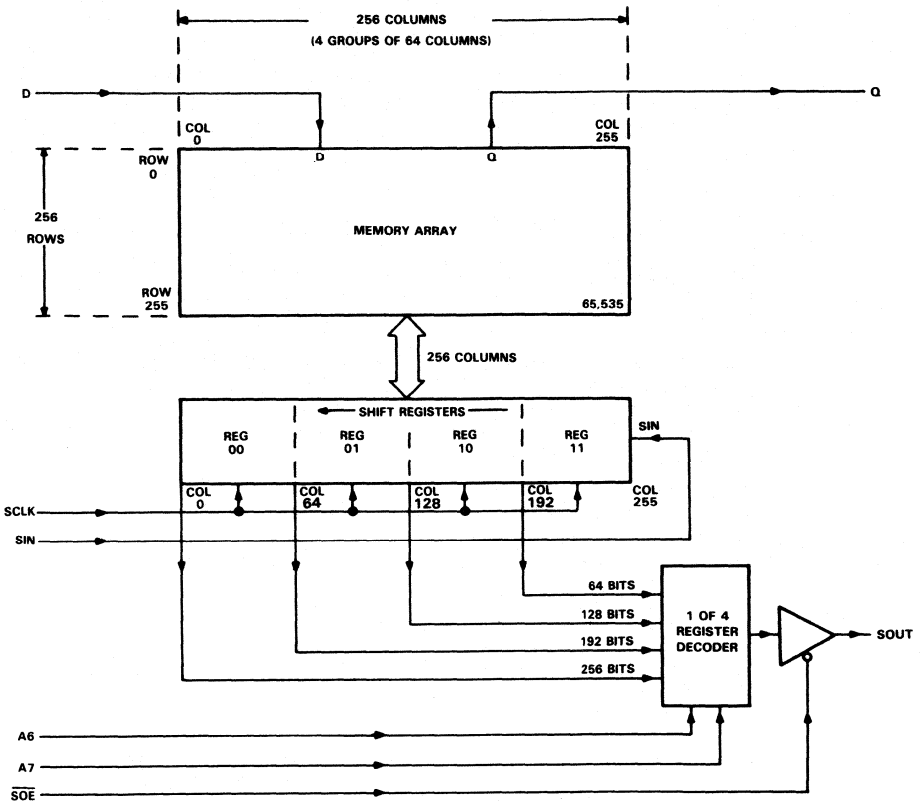
All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The TMS4161 is offered in a 20-pin dual-in-line-plastic package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil (7,62 mm) centers.

random access address space to sequential address space mapping

The TMS4161 is designed with each row divided into four, 64-column sections. The first column section to be shifted out is selected by the two most significant column address bits. If the two bits represent binary 00, then one to four registers can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) registers can be shifted out in order. If the two bits represent 10, then one to two of the most significant registers can be shifted out in order. Finally, if the two bits represent 11 only the most significant register can be shifted out. All registers are shifted out with the least significant bit (bit 0) first and the most significant bit (bit 63) last. Note that if the two column address bits equal 00 during the last register transfer cycle ($\overline{TR}/\overline{QE}$ equal to 0) a total of 256 bits can be sequentially read out.

functional block diagram



random access operation

$\overline{TR}/\overline{QE}$

The $\overline{TR}/\overline{QE}$ pin has two functions. First, it selects either register transfer or random-access operation as $\overline{RAS}$ falls, and second, if this is a random-access operation, it functions as an output enable after $\overline{CAS}$ falls.

To use the TMS4161 in the random-access mode, $\overline{TR}/\overline{QE}$ must be high as $\overline{RAS}$ falls. Holding $\overline{TR}/\overline{QE}$ high disconnects the 256 elements of the shift registers from the corresponding 256 bit lines of the memory array. If data is to be shifted, the shift registers must be disconnected from the bit lines. Holding $\overline{TR}/\overline{QE}$ low enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

Once $\overline{CAS}$ has been pulled low, $\overline{TR}/\overline{QE}$ controls when the data will appear at the Q output (if this is a read cycle). Whenever $\overline{TR}/\overline{QE}$ is held high, the Q output will be in the high-impedance state. This feature removes the possibility

of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state as long as $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ is held high. Data will not appear on the output until after both $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if t_{CQE} is greater than t_{CQE} MAX, and t_{RLCL} is greater than t_{RLCL} MAX. Likewise, $t_{a(C)}$ MAX is valid only if t_{RLCL} is greater than t_{RLCL} MAX. Once the output is valid, it will remain valid while $\overline{CAS}$ and $\overline{TR}/\overline{QE}$ are both low; $\overline{CAS}$ or $\overline{TR}/\overline{QE}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power. Note that the shift registers are also dynamic storage elements and that the data held in the registers will be lost unless SCLK goes high to shift the data one bit position or else the data is reloaded from the memory array. See specifications for maximum register data retention times.

page-mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

sequential access operation

$\overline{TR}/\overline{QE}$

Memory operations involving parallel use of the shift register are first indicated by bringing $\overline{TR}/\overline{QE}$ low before $\overline{RAS}$ falls low. This enables the switches connecting the 256 elements of the shift register to the 256 bit lines of the memory array. The $\overline{W}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{W}$)

In the sequential access mode, $\overline{W}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{W}$ is held low as $\overline{RAS}$ falls, and, to transfer from the memory array to the shift registers, $\overline{W}$ is held high as $\overline{RAS}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{RAS}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. The A0-A7, $\overline{W}$, and the $\overline{TR}/\overline{QE}$ line are latched on the falling edge of $\overline{RAS}$.

register column address (A7, A6)

To select one of the four shift registers (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{CAS}$ falls. However, the $\overline{CAS}$ and register address signals need not be supplied every cycle, only when it is desired to change or select a new register.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view the shift registers as though it were made of 256 rising edge D flip-flops connected D to Q. The TMS4161 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pin not only on the rising edge of SCLK but also after an access time of $t_{a(RSO)}$ from $\overline{RAS}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pin and is shifted out through the SOUT pin. The TMS4161 is designed such that it requires 0 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least 8 ns after SLCK rises. These features make it possible to easily connect TMS4161s together, to allow SOUT to be connected to SIN, and to give external circuitry a full SLCK cycle time to allow manipulation of the serial data. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before serial data is applied at SIN.

$\overline{SOE}$

The serial output enable pin controls the impedance of the serial output allowing multiplexing of more than one bank of TMS4161 memories into the same external video circuitry. When $\overline{SOE}$ is at a low logic level, SOUT will be enabled and the proper data read out. When $\overline{SOE}$ is at a high logic level, SOUT will be disabled and be in the high-impedance state.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1)	−1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS}	−1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.4		$V_{DD}+0.3$	V
Low-level input voltage, V_{IL} (see Note 2)	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4161-15			TMS4161-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage (Q, SOUT)	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage (Q, SOUT)	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	$t_{c(rd)}$ = minimum cycle time, $\overline{TR}/\overline{QE}$ low after RAS falls,‡ SCLK and SIN low, $\overline{SOE}$ high		35	50		30	45	mA
I_{DD2}§	Standby current	After 1 − $\overline{RAS}$ cycle, $\overline{RAS}$ and $\overline{CAS}$ high, SCLK low, SIN low, $\overline{SOE}$ high		8	10		6	8	mA
I_{DD3}	Average refresh current	$t_{c(rd)}$ = minimum cycle time, $\overline{CAS}$ high, SCLK low, SIN low, $\overline{SOE}$ high, $\overline{TR}/\overline{QE}$ high		30	40		25	35	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle time, $\overline{RAS}$ low, $\overline{CAS}$ cycling, $\overline{TR}/\overline{QE}$ low after RAS falls,‡ SCLK and SIN low, $\overline{SOE}$ high		30	40		20	32	mA
I_{DD5}‖	Average shift register current (includes I_{DD2})	$\overline{RAS}$ high, $\overline{CAS}$ high, $t_{c(SCLK)}$ = 100 ns		16	27		15	25	mA

NOTE: I_{DD1} thru I_{DD5} assume no load on Q and SOUT. Additional information on these parameters on last page.

† All typical values are at T_A = 25°C and nominal supply voltages.

‡ See appropriate timing diagram.

§ V_{IL} > −0.6 V.

‖ See power versus cycle time derating curve on last page.

capacitance over recommended supply voltage and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
$C_{i(CK)}$	Input capacitance, serial clock	8	10	pF
$C_{i(SI)}$	Input capacitance, serial in	4	5	pF
$C_{i(SOE)}$	Input capacitance, serial output enable	4	5	pF
$C_{i(TR)}$	Input capacitance, register transfer input	4	5	pF
$C_{o(Q)}$	Output capacitance, random-access data	5	7	pF
$C_{o(SOUT)}$	Output capacitance, serial out	5	7	pF

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see figure 1)

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4161-15		TMS4161-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF	t_{CAC}		100		135	ns
$t_{a(QE)}$	Access time of Q from $\overline{TR/QE}$ low	C_L = 100 pF			40		40	
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF	t_{RAC}		150		200	
$t_{a(RSO)}$	SOUT access time from $\overline{RAS}$ high	C_L = 50 pF			60		60	
$t_{a(SOE)}$	Access time from $\overline{SOE}$ low to SOUT	C_L = 50 pF			20		25	
$t_{a(SO)}$	Access time from SCLK	C_L = 50 pF			30		30	
$t_{dis(CH)}$‡	Q output disable time from $\overline{CAS}$ high		t_{OFF}		20		25	
$t_{dis(QE)}$‡	Q output disable time from $\overline{TR/QE}$ high				20		25	
$t_{dis(SOE)}$‡	Serial output disable time from $\overline{SOE}$ high				20		25	

‡ The maximum values for $t_{dis(CH)}$, $t_{dis(QE)}$, and $t_{dis(SOE)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	ALT. SYMBOL	TMS4161-15 MIN	TMS4161-15 MAX	TMS4161-20 MIN	TMS4161-20 MAX	UNIT
$t_{c(P)}$	Page-mode cycle time	t_{PC}	160		225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	235		310		ns
$t_{c(W)}$	Write cycle time	t_{WC}	235		310		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		325		ns
$t_{c(SCLK)}$	Serial clock cycle time	t_{SCC}	40	50,000	40	50,000	ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low§	t_{CAS}	100	10,000	135	10,000	ns
$t_{w(RH)}$	Pulse width, $\overline{RAS}$ high (precharge time)	t_{RP}	75		100		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low¶	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	45		45		ns
$t_{w(CKL)}$	Pulse width, SCLK low		10		10		ns
$t_{w(CKH)}$	Pulse width, SLCK high		10		10		ns
$t_{w(QE)}$	$\overline{TR}/\overline{QE}$ pulse width low time		40		40		ns
t_t	Transition times (rise and fall) $\overline{RAS}$, $\overline{CAS}$, and SCLK	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(RW)}$	$\overline{W}$ setup time before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	−5		−5		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		ns
$t_{su(SI)}$	Serial data setup time before SCLK high		10		10		ns
$t_{su(TR)}$	$\overline{TR}/\overline{QE}$ setup time before $\overline{RAS}$ low		0		0		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	20		25		ns
$t_{h(RW)}$	$\overline{W}$ hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		20		20		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	95		140		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	110		145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	110		145		ns
$t_{h(RSO)}$	Serial data out hold time after $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low		30		30		ns
$t_{h(SI)}$	Serial data in hold time after SCLK high		0		0		ns

(continued next page)

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition; V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_T = 5 ns.

‡ Page-mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

	PARAMETER	ALT. SYMBOL	TMS4161-15		TMS4161-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{h(SO)}$	Serial data out hold time after SCLK high		8		8		ns
$t_{h(TR)}$	$\overline{TR}/\overline{QE}$ hold time after $\overline{RAS}$ low		20		20		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLQEH}	Delay time, $\overline{CAS}$ low to $\overline{QE}$ high		100		135		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		65		ns
t_{CQE}	Delay time, $\overline{CAS}$ low to $\overline{QE}$ low (maximum value specified only to guarantee $t_{a(QE)}$ access time)			60		95	ns
t_{RHSC}	Delay time, $\overline{RAS}$ high to SCLK high		50	50,000	50	50,000	ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee $t_{a(R)}$)	t_{RCD}	20	50	25	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	110		130		ns
t_{CKRL}	Delay time, SCLK high before $\overline{RAS}$ low with $\overline{TR}/\overline{QE}$ low¶		10	50,000	10	50,000	ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

¶ SCLK be high or low during $t_{w(RL)}$.

PARAMETER MEASUREMENT INFORMATION

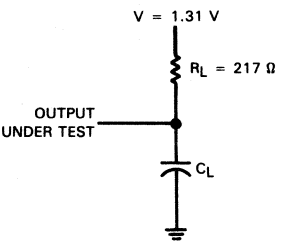
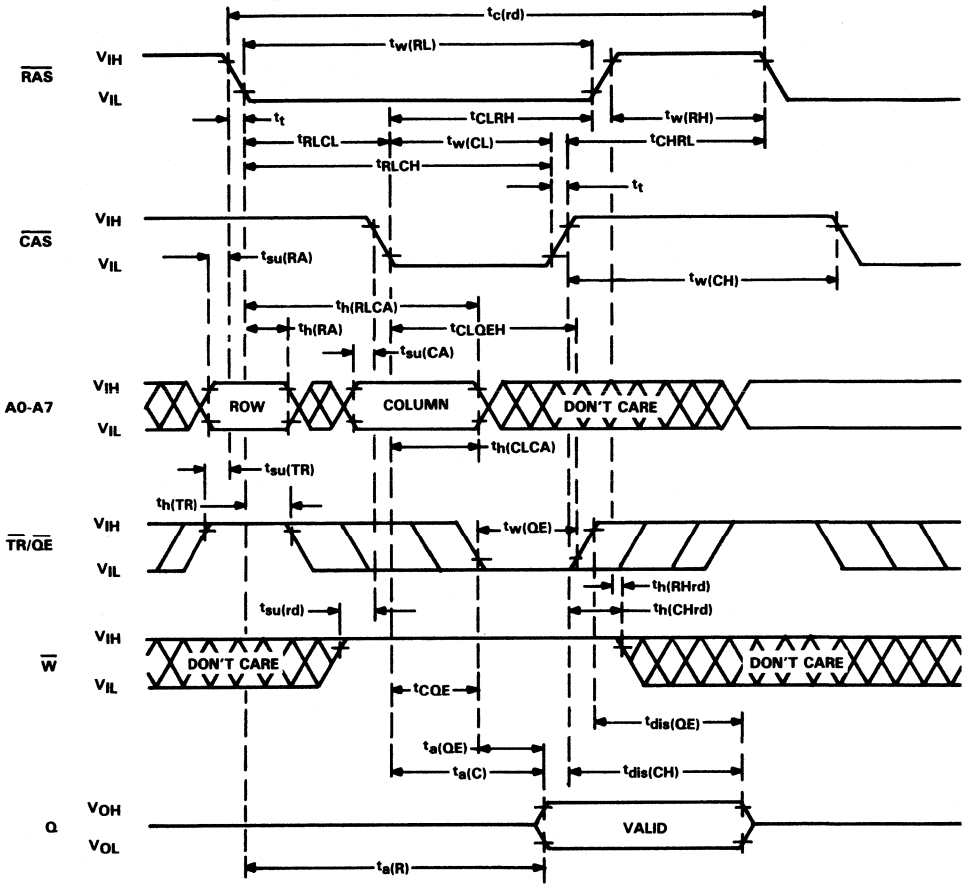
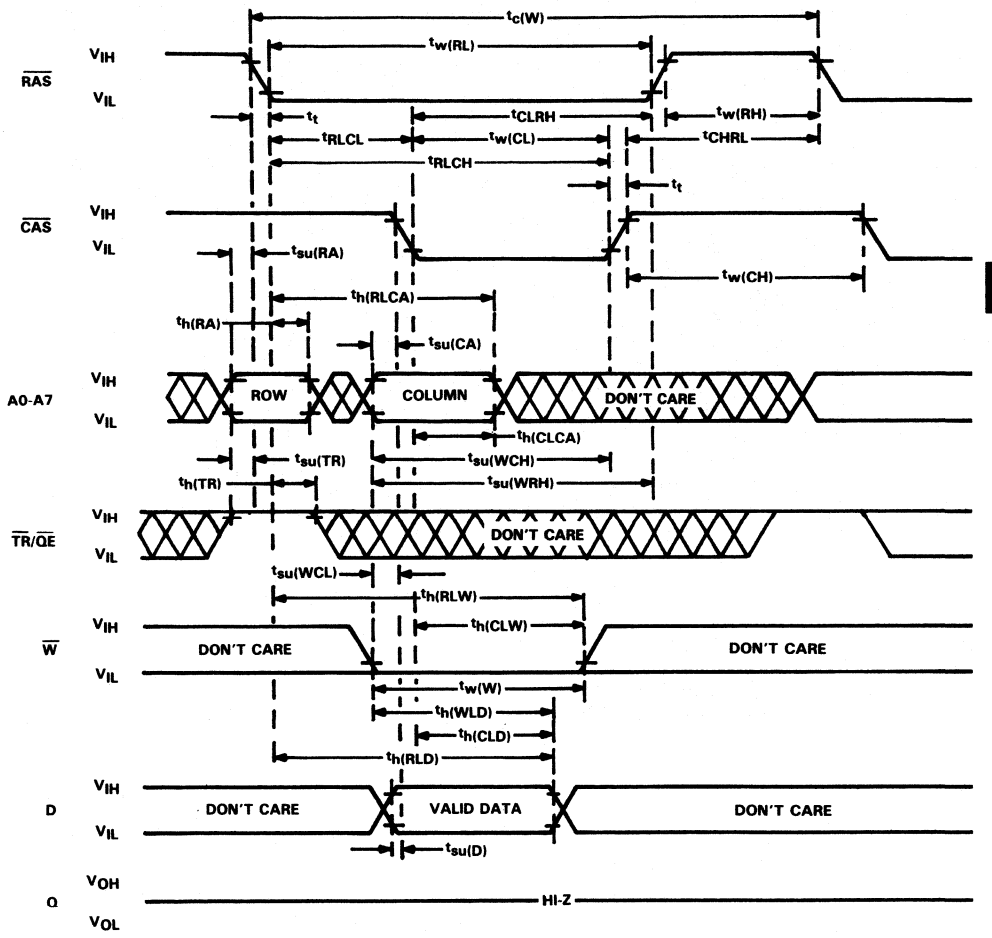


FIGURE 1 – LOAD CIRCUIT

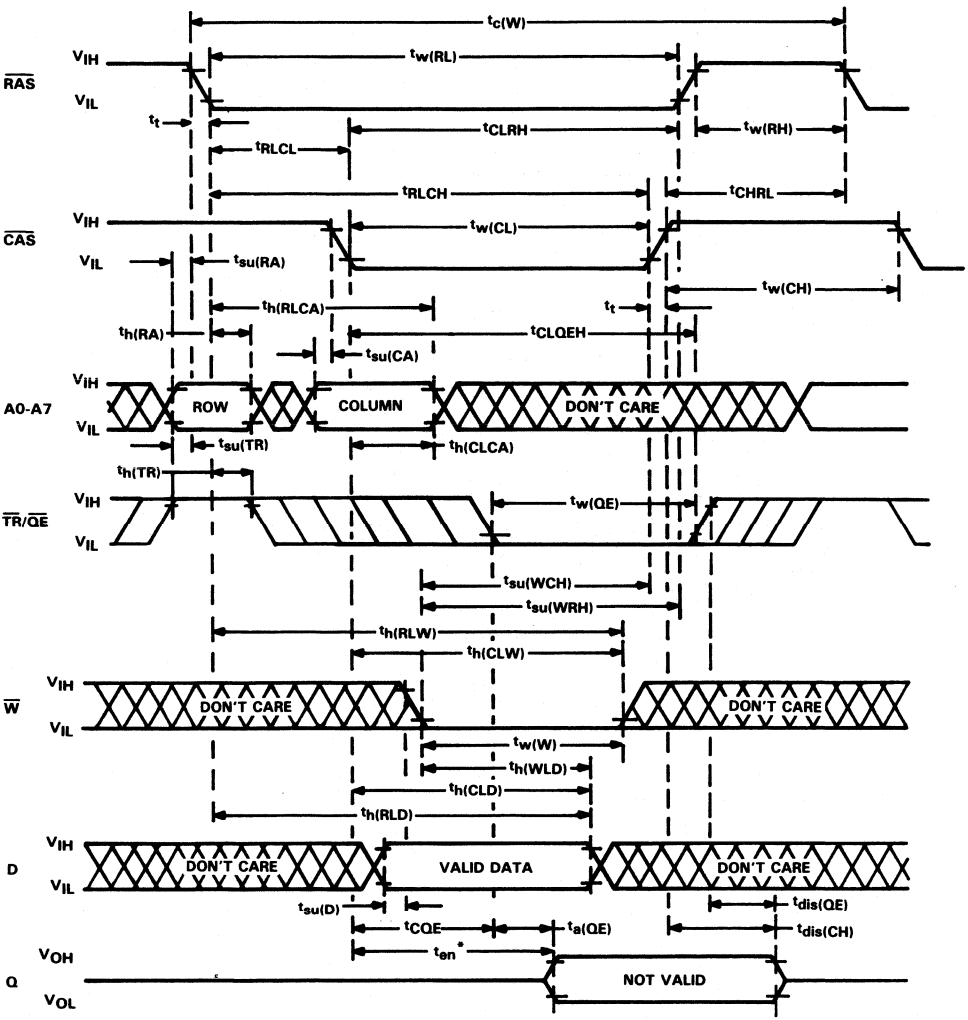
read cycle timing



early write cycle timing

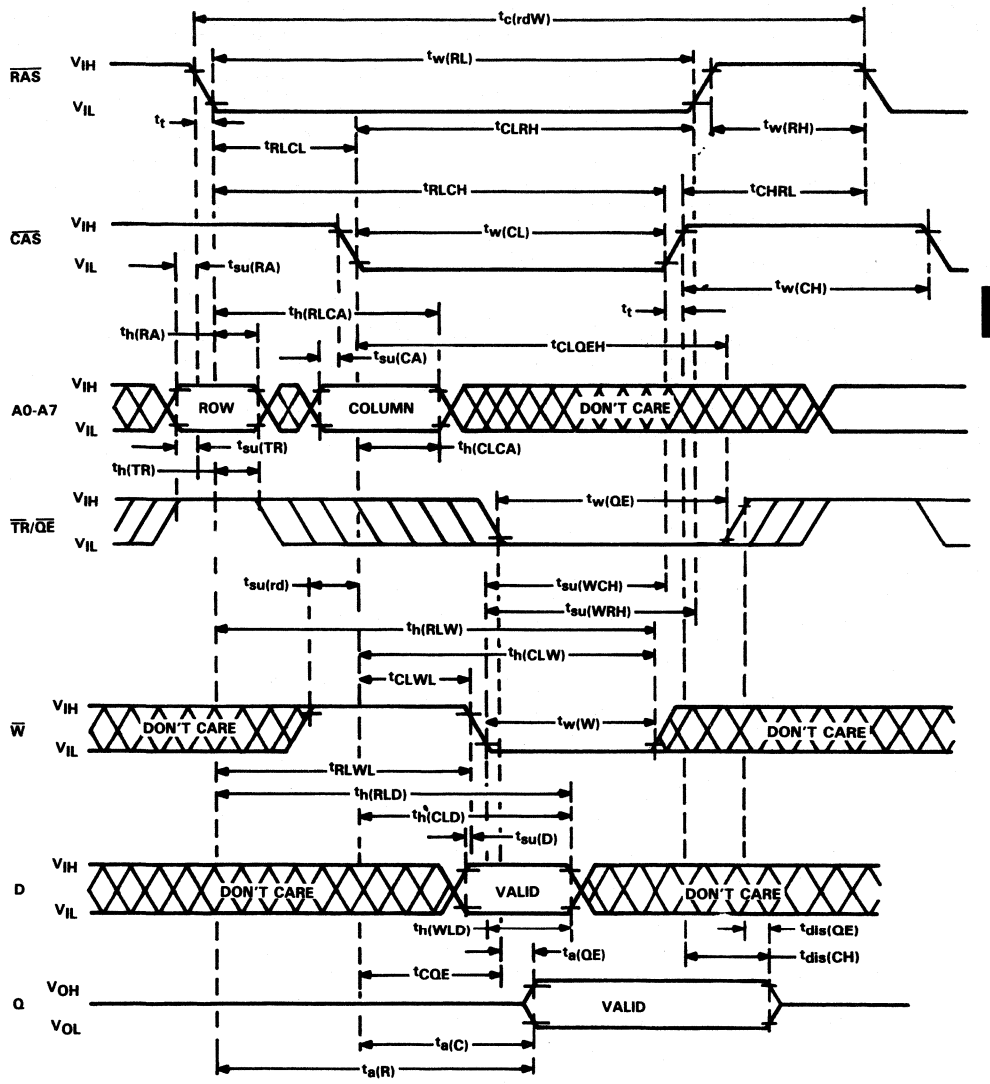


write cycle timing

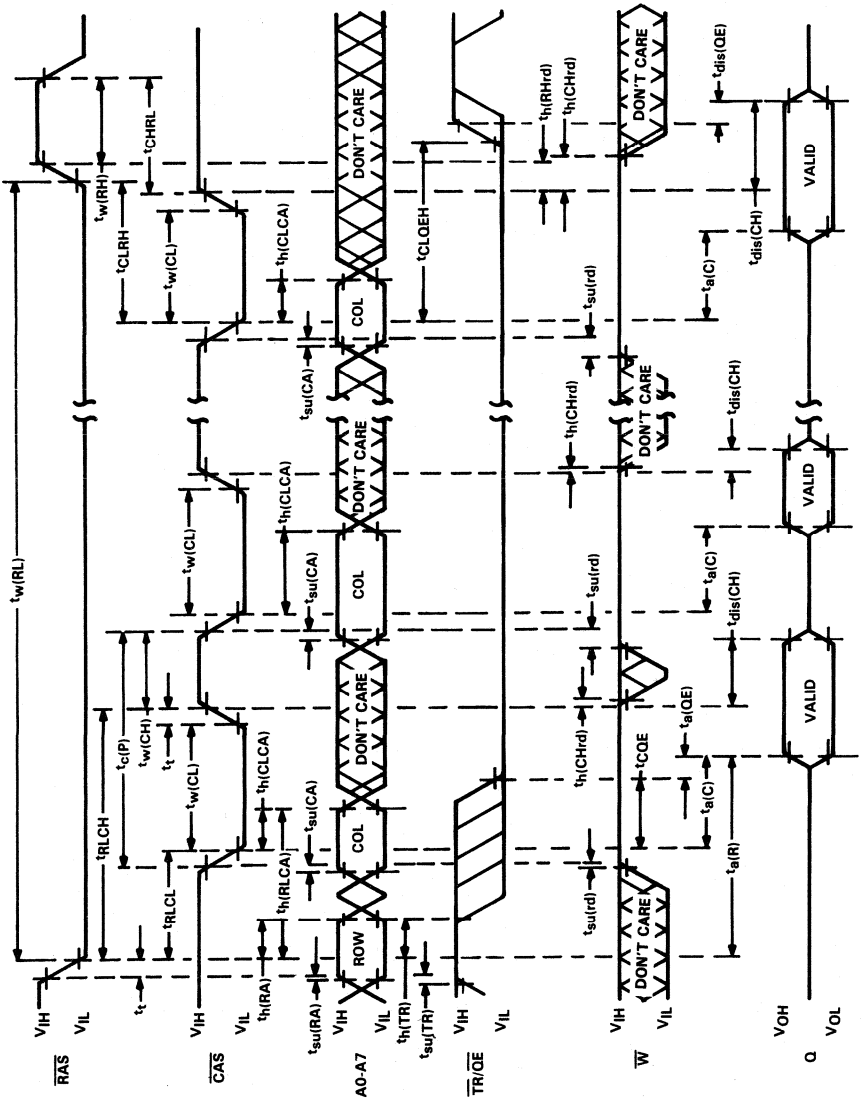


* The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing

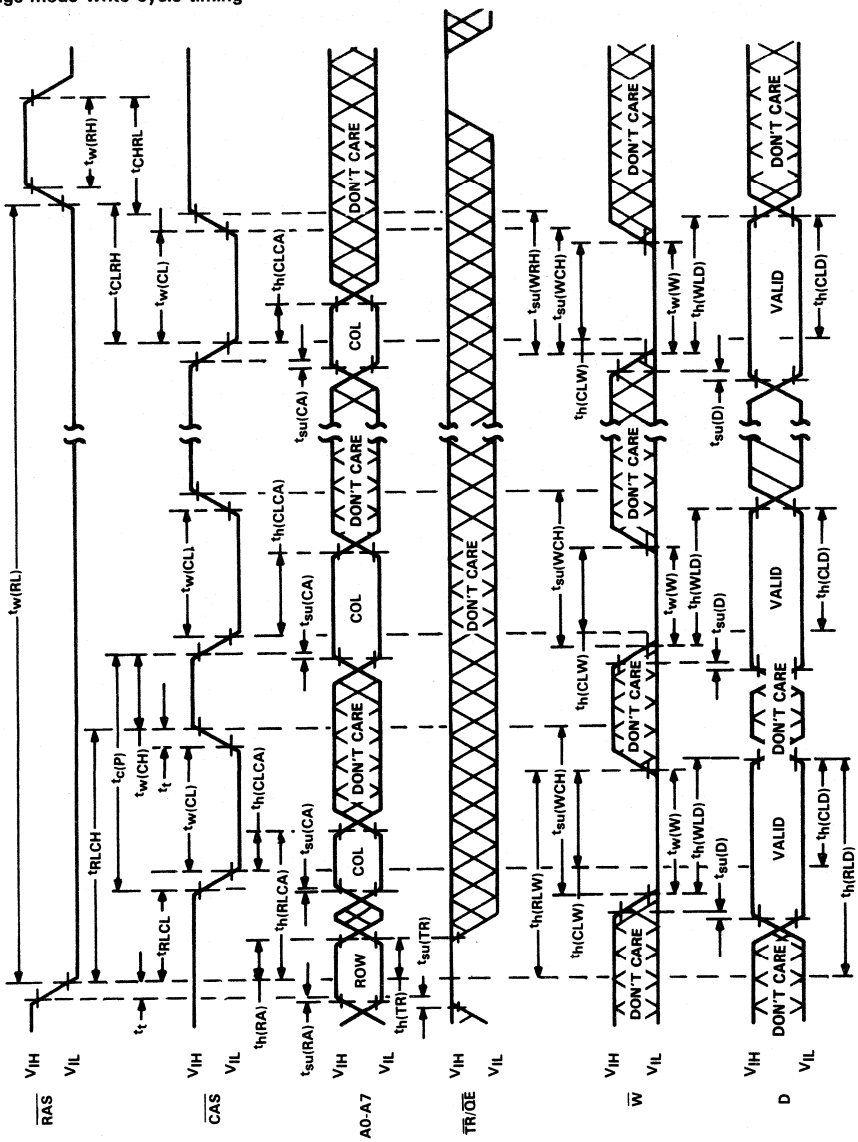


page-mode read cycle timing



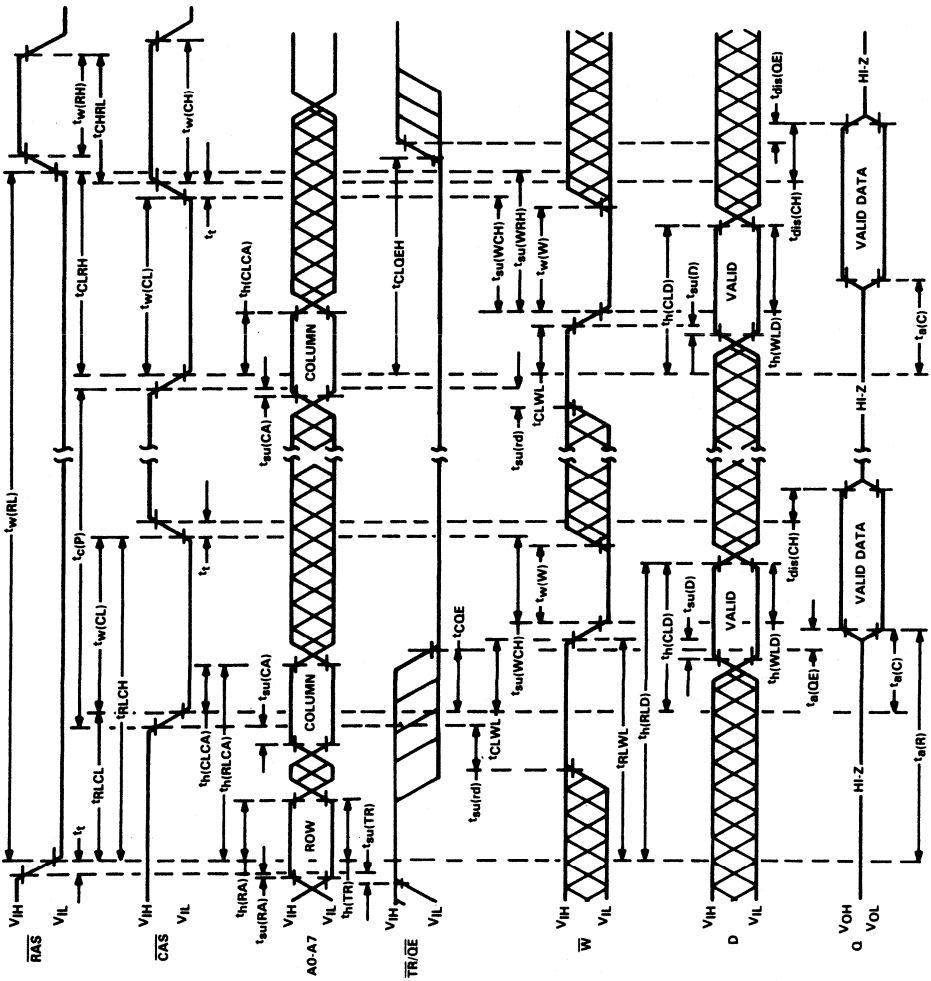
NOTE: Timing is for non-multiplexed D, Q, and Address lines.

page-mode write cycle timing



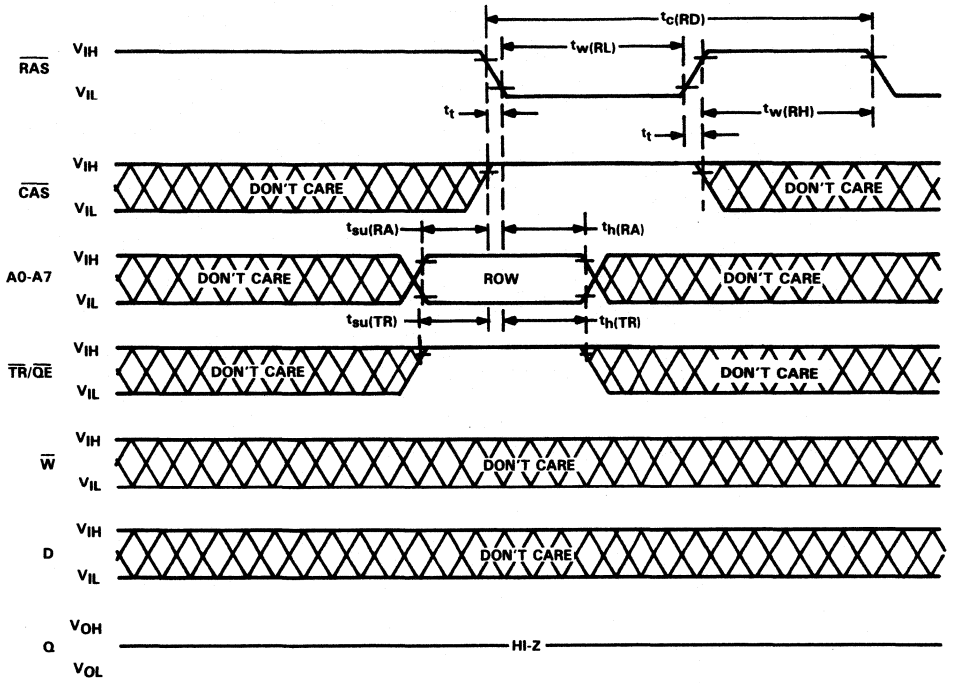
NOTE 1: Timing is for non-multiplexed D, Q and Address lines.

page-mode read-modify-write cycle timing

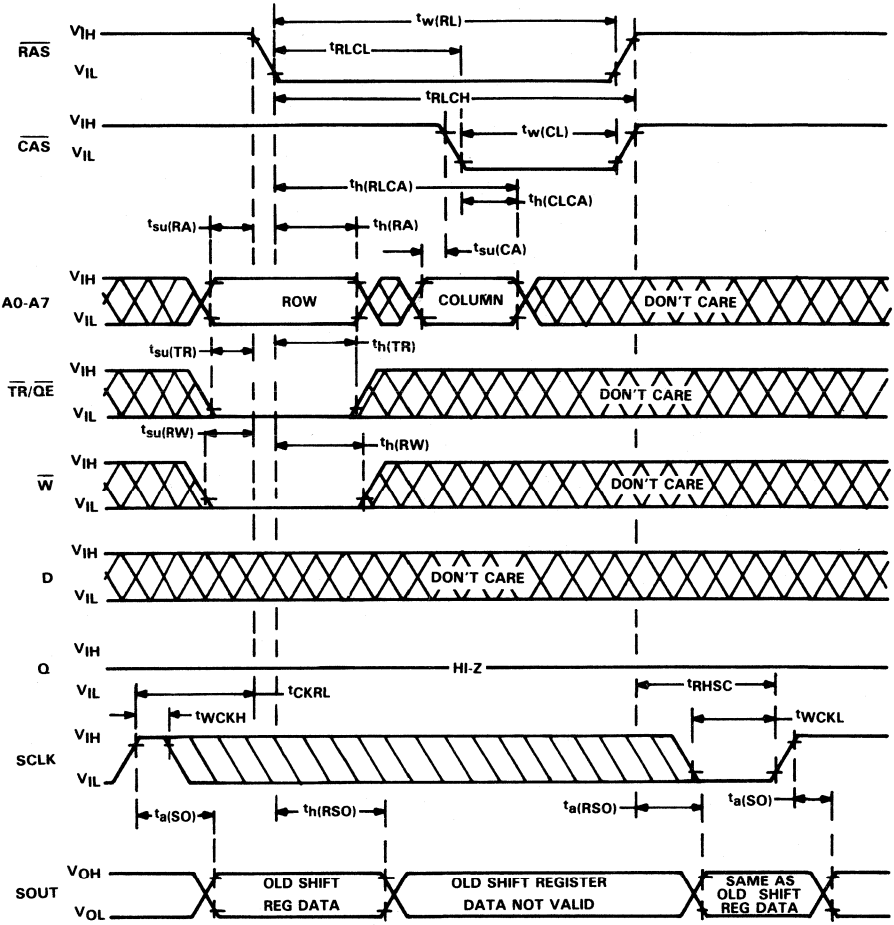


NOTE: Timing is for non-multiplexed D, Q, and Address lines.

$\overline{RAS}$ only refresh timing



shift register to memory timing

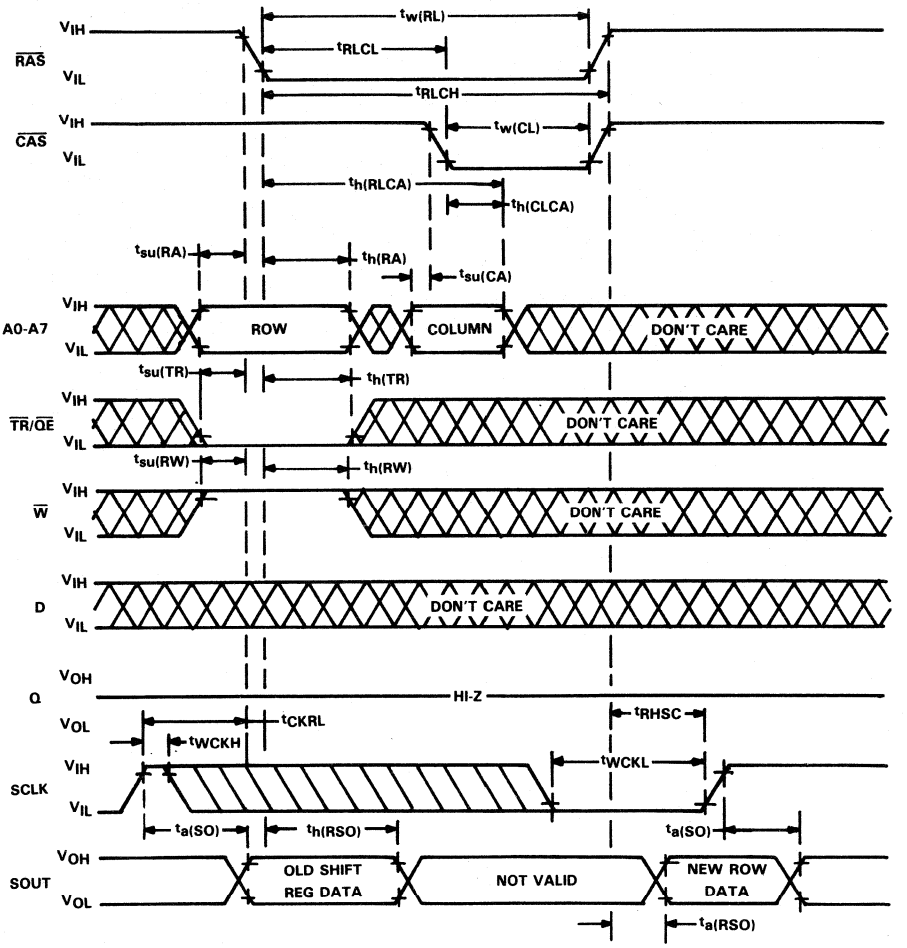


NOTES: 1. The shift register to memory cycle is used to transfer data from the shift register to the memory array. Every one of the 256 locations in the shift register is written into the 256 columns of the selected row. Note that the data that was in the shift register may have resulted, either from a serial shift in or from a parallel load of the shift register from one of the memory array rows.

2. $\overline{SOE}$ assumed low.

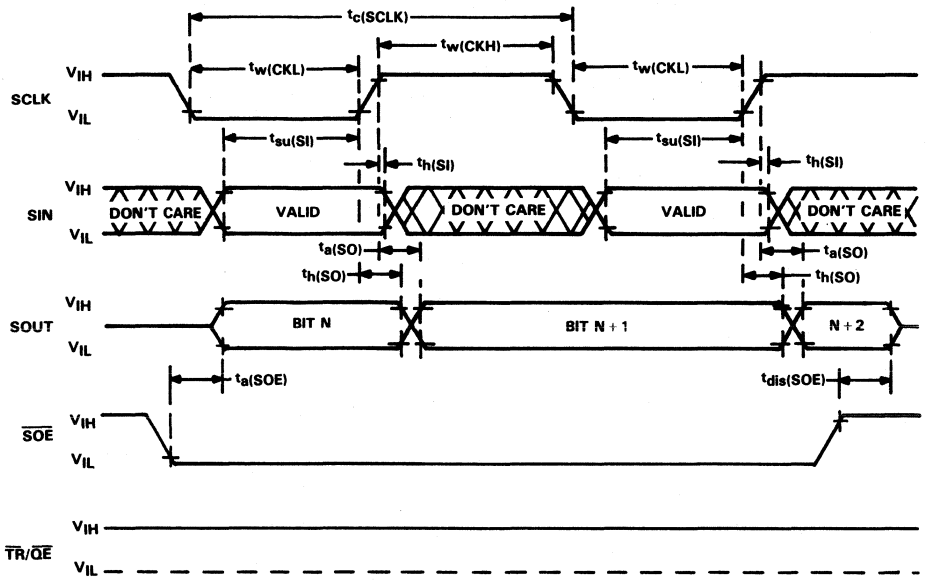
3. SCLK may be high or low during $t_{w(RL)}$.

memory to shift register timing



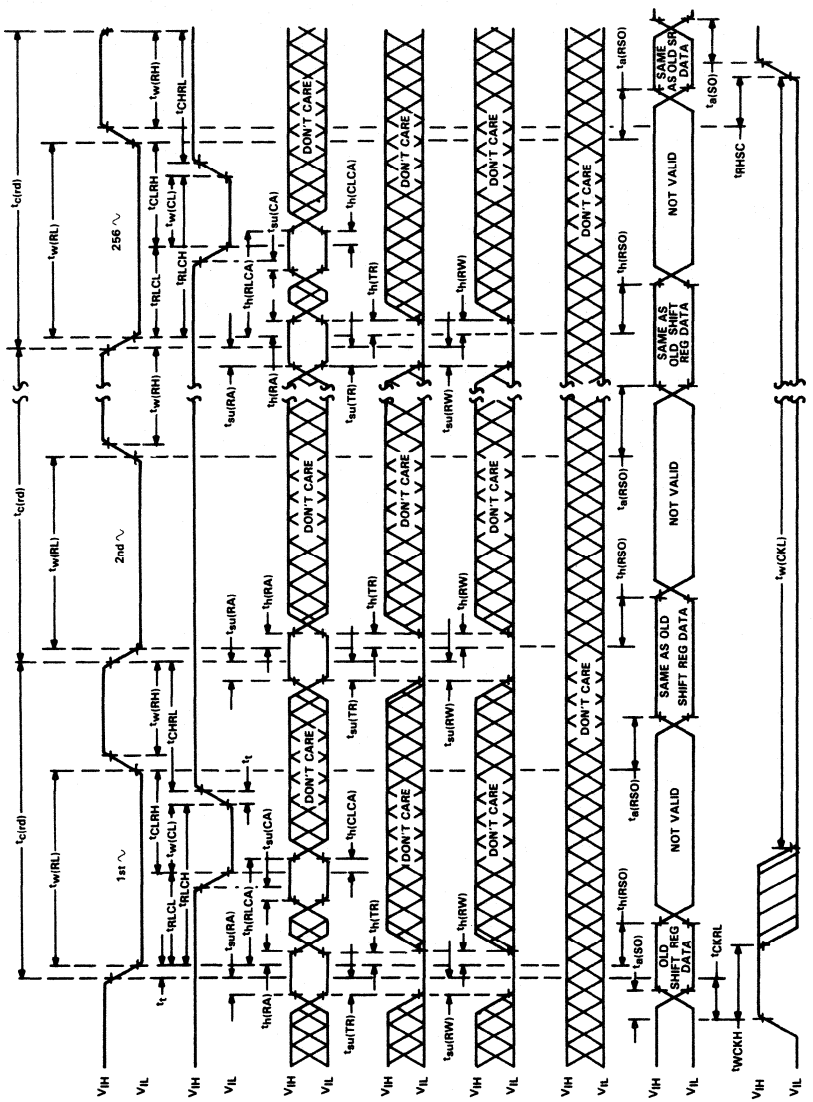
NOTES: 1. The memory to shift register cycle is used to load the shift register in parallel from the memory array. Every one of the 256 locations in the shift register re written into from the 256 columns of the selected row. Note that the data that is loaded into the shift register may be either shifted out or written back into another row.
2. $\overline{SOE}$ assumed low.
3. SCLK may be high or low during $t_{w(RL)}$.

serial data transfer timing



NOTE: While shifting data through the serial shift register, the state of $\overline{TR}/\overline{QE}$ is a don't care as long as $\overline{TR}/\overline{QE}$ is held high when $\overline{RAS}$ goes low and $t_{su(TR)}$ and $t_{h(TR)}$ timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift register.

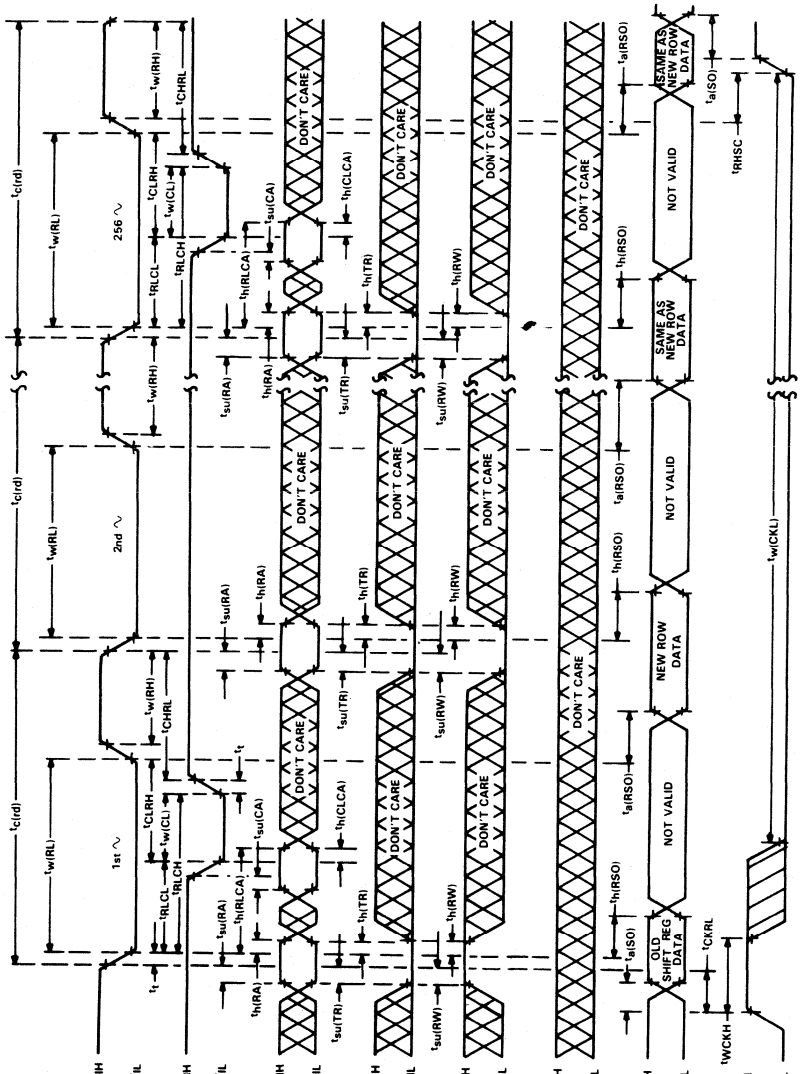
shift register to memory multiple timing



* $\overline{CAS}$ and register address need not be supplied every cycle, only when it is desired to change or select a new register length.

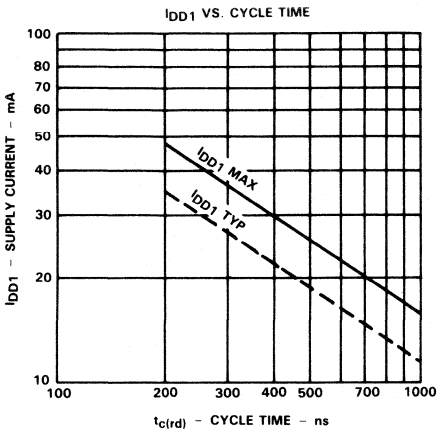
NOTES: 1. The shift register to memory multiple cycle is used to write the shift register data to more than one row of the memory array. An application of this could be clearing all memory. To do this, the SIN line would be held at 0 to fill all locations in the shift register with 0's. The shift register would then be written into all 256 rows of the memory array in 256 cycles. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.
2. $\overline{SOE}$ assumed low.

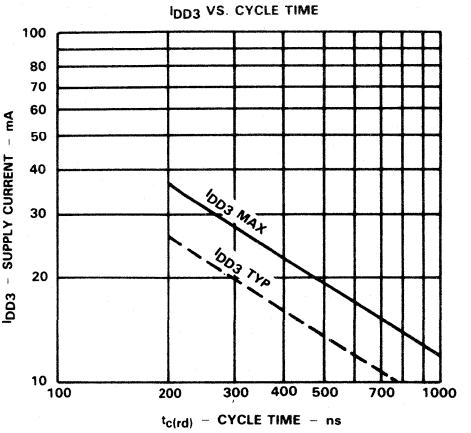
memory to shift register to memory multiple timing

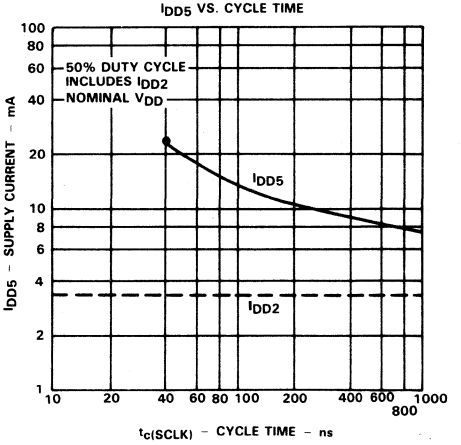


* $\overline{CAS}$ and register address need not be supplied every cycle, only when it is desired to change from one register address to another.

NOTES: 1. The memory to shift register to memory multiple cycle is used to reorder the rows within the memory array itself. First, the data in a row is stored in the shift register and then it is written into other selected rows. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.
2. $\overline{SOE}$ assumed low.







Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS4164, SMJ4164
65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

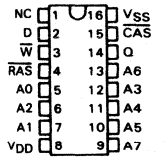
JULY 1980 – REVISED OCTOBER 1983

- 65,536 X 1 Organization
- Single +5-V Supply (10% Tolerance)
- JEDEC Standardized Pin-Out in Dual-In-Line Packages
- Upward Pin Compatible with TMS4116 (16K Dynamic RAM)
- First Military Version of 64K DRAM
- Available Temperature Ranges:
  - M . . . −55°C to 125°C
  - S . . . −55°C to 100°C
  - E . . . −40°C to 85°C
  - L . . . 0°C to 70°C
- Long Refresh Period . . . 4 milliseconds
- Low Refresh Overhead Time . . . As Low As 1.8% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 125 mW (TYP)
  - Standby . . . 17.5 mW (TYP)
- Performance Ranges (S, E, L Temperature Ranges):

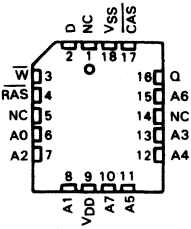
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4164-12	120 ns	70 ns	230 ns	260 ns
'4164-15	150 ns	85 ns	260 ns	285 ns
'4164-20	200 ns	135 ns	326 ns	345 ns

- New SMOS (Scaled-MOS) N-Channel Technology

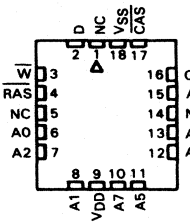
TMS4164 . . . NL PACKAGE
SMJ4164 . . . JD PACKAGE
(TOP VIEW)



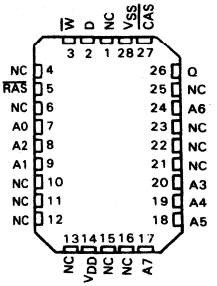
TMS4164 . . . FPL PACKAGE
(TOP VIEW)



SMJ4164 . . . FG PACKAGE
(TOP VIEW)



SMJ4164 . . . FE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Data-In
NC	No-Connection
Q	Data-Out
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The '4164 is a high-speed, 65,536-bit, dynamic random-access memory, organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

ADVANCE INFORMATION
MILITARY PRODUCTS (SMJ) ONLY
This document contains information on a new product.
Specifications are subject to change without notice.

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The '4164 features $\overline{RAS}$ access times of 120 ns, 150 ns, and 200 ns maximum. Power dissipation is 125 mW typical operating and 17.5 mW typical standby.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility. Pin 1 has no internal connection to allow compatibility with other 64K RAMs that use this pin for an additional function.

The TMS4164 is offered in a 16-pin dual-in-line plastic package and is guaranteed for operation from 0°C to 70°C. This package is designed for insertion in mounting-hole rows on 300 mil (7,62 mm) centers. An 18-pin plastic chip carrier (FP suffix) package is also available.

The SMJ4164 is offered in a 16-pin dual-in-line ceramic sidebraze package (JD) and in leadless ceramic chip carrier packages (FE and FG). The JD package is designed for insertion in mounting-hole rows on 300 mil (7,62 mm) centers whereas the FE and FG packages are intended for surface mounting on solder lands on 0.050 inch (1,27 mm) centers. The FE package offers a three layer, 28-pad, rectangular chip carrier with dimensions of 0.350 × 0.550 × 0.072 inches (8,89 × 13,97 × 1,83 mm). The FG package is a three layer, 18-pad, rectangular chip carrier with dimensions of 0.290 × 0.425 × 0.065 inches (7,37 × 10,8 × 1,65 mm).

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on Pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, W is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 54/74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early-write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

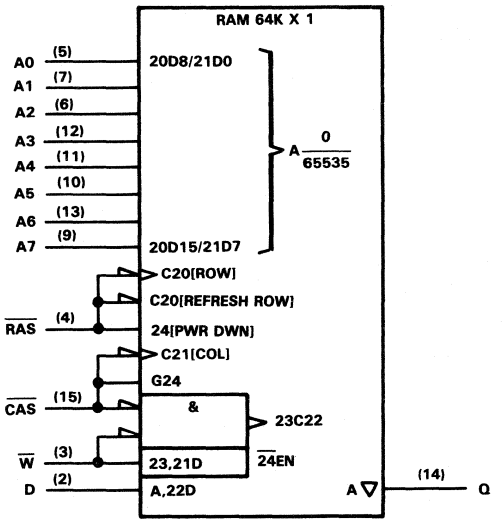
page-mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power-up

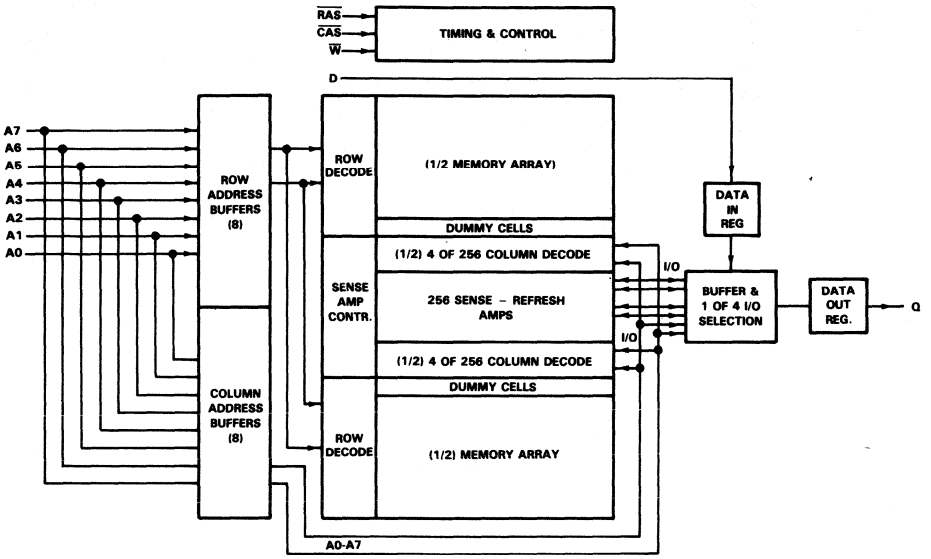
After power-up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{RAS}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1)		−1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS}		−1 V to 6 V
Short circuit output current		50 mA
Power dissipation		1 W
Operating free-air temperature range:	TMS'	0°C to 70°C
Operating case temperature range:	SMJ' – M version	−55°C to 125°C
	– S version	−55°C to 100°C
	– E version	−40°C to 85°C
Storage temperature range		−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

PARAMETER		TMS4164			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{DD}		4.5	5	5.5	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}	V_{DD} = 4.5 V	2.4		4.8	V
	V_{DD} = 5.5 V	2.4		6	
Low-level input voltage, V_{IL} (see Notes 2 and 3)		−0.6		0.8	V
Operating free-air temperature, T_A		0		70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions should comprehend this occurrence.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4164-12			TMS4164-15			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle		40	48		35	45	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high		28	40		25	37	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		28	40		25	37	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ Additional information on last page.
§ V_{IL} > −0.6 V.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4164-20			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle		27	37	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high		20	32	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		20	32	mA

† All typical values are at T_A = 25°C and nominal supply voltages.
‡ Additional information on last page.
§ V_{IL} > −0.6 V.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TMS4164		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(D)}$	Input capacitance, data input	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	8	pF

† All typical values are at T_A = 25 °C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4164-12		TMS4164-15		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	40	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4164-20		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF Load = 2 Series 74 TTL gates	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, Load = 2 Series 74 TTL gates	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4164-12		TMS4164-15		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		285		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low§	t_{CAS}	70	10,000	85	10,000	ns
$t_{w(RH)}$	Pulse width, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	−5		−5		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	85		95		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	85		95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		45		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	40		45		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	85		95		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	40		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	15	50	20	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	85		100		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4164-20 MIN	TMS4164-20 MAX	UNIT
$t_{c(P)}$	Page mode cycle time	t_{PC}	206		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	326		ns
$t_{c(W)}$	Write cycle time	t_{WC}	326		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low§	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse width, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	−5		
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	55		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	55		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

recommended operating conditions

PARAMETER	SMJ4164									UNIT
	M VERSION			S VERSION			E VERSION			
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{SS}		0			0			0		
High-level input voltage, V_{IH}	2.4		$V_{CC}+0.3$	2.4		$V_{CC}+0.3$	2.4		$V_{CC}+0.3$	V
Low-level input voltage, V_{IL} (see Notes 2 and 3)	−0.6		0.8	−0.6		0.8	−0.6		0.8	V
Operating case temperature, T_C	−55		125	−55		100	−40		85	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions should comprehend this occurrence.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4164-15 M VERSION			SMJ4164-20 M VERSION			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 4.5 V to 5.5 V, output open			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle			48			45	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high			7			7	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high			40			37	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling			40			37	mA

† All typical values are at T_C = 25°C and nominal supply voltages.
‡ Additional information on last page.
§ V_{IL} > −0.6 V.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4164-12 S,E VERSIONS			SMJ4164-15 S,E VERSIONS			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 4.5 V to 5.5 V, output open			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle		40	48		35	45	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high		28	40		25	37	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		28	40		25	37	mA

† All typical values are at T_C = 25°C and nominal supply voltages.
‡ Additional information on last page.
§ V_{IL} > −0.6 V.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4164-20 S,E VERSIONS			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=4.5 V to 5.5 V, output open			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	t_c = minimum cycle		27	37	mA
I_{DD2}§	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high		20	32	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		20	32	mA

† All typical values are at T_C = 25°C and nominal supply voltages.
‡ Additional information on last page.
§ V_{IL} > −0.6 V.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		SMJ4164		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(D)}$	Input capacitance, data input	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	8	pF

† All typical values are at T_A = 25 °C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4164-15 M VERSION		SMJ4164-20 M VERSION		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, see Figure 1	t_{CAC}		100		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, see Figure 1	t_{RAC}		150		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, see Figure 1	t_{OFF}	0	50	0	60	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4164-12 S,E VERSION		SMJ4164-15 S,E VERSIONS		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, see Figure 1	t_{CAC}		70		85	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, see Figure 1	t_{RAC}		120		150	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, see Figure 1	t_{OFF}	0	40	0	40	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4164-20 S,E VERSION		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 80 pF, see Figure 1	t_{CAC}		135	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, see Figure 1	t_{RAC}		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 80 pF, see Figure 1	t_{OFF}	0	50	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	SMJ4164-15 M VERSION		SMJ4164-20 M VERSION		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	160		225		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	330		410		ns
$t_{c(W)}$	Write cycle time	t_{WC}	330		410		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		425		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low§	t_{CAS}	100	1,500	135	1,500	ns
$t_{w(RH)}$	Pulse width, $\overline{RAS}$ high (precharge time)	t_{RP}	160		200		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low¶	t_{RAS}	150	1,500	200	1,500	ns
$t_{w(W)}$	Write pulse width	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	20	3	20	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	5		5		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	60		70		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	95		140		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	70		90		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	125		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	50		60		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	70		90		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	125		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	100		135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	60		65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	25	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	110		130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	5		5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	SMJ4164-12 S,E VERSIONS		SMJ4164-15 S,E VERSIONS		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	130		160		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	230		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	260		285		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		50		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low§	t_{CAS}	70	10,000	85	10,000	ns
$t_{w(RH)}$	Pulse width, $\overline{RAS}$ high (precharge time)	t_{RP}	80		100		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low¶	t_{RAS}	120	10,000	150	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		45		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	−5		−5		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	50		50		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	50		50		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	40		45		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	85		95		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		45		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	85		95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		45		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	40		45		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	85		95		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	120		150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		100		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	40		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	15	50	20	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	85		100		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	SMJ4164-20 S,E VERSIONS MIN	SMJ4164-20 S,E VERSIONS MAX	UNIT
$t_{c(P)}$	Page mode cycle time	t_{PC}	206		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	326		ns
$t_{c(W)}$	Write cycle time	t_{WC}	326		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)‡	t_{CP}	80		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low§	t_{CAS}	135	10,000	ns
$t_{w(RH)}$	Pulse width, $\overline{RAS}$ high (precharge time)	t_{RP}	120		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low¶	t_{RAS}	200	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	−5		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	55		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	120		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	145		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	55		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	5		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	55		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	145		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	135		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	65		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	130		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ Page mode only.

§ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page mode read-modify-write also.

¶ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

PARAMETER MEASUREMENT INFORMATION

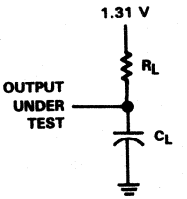
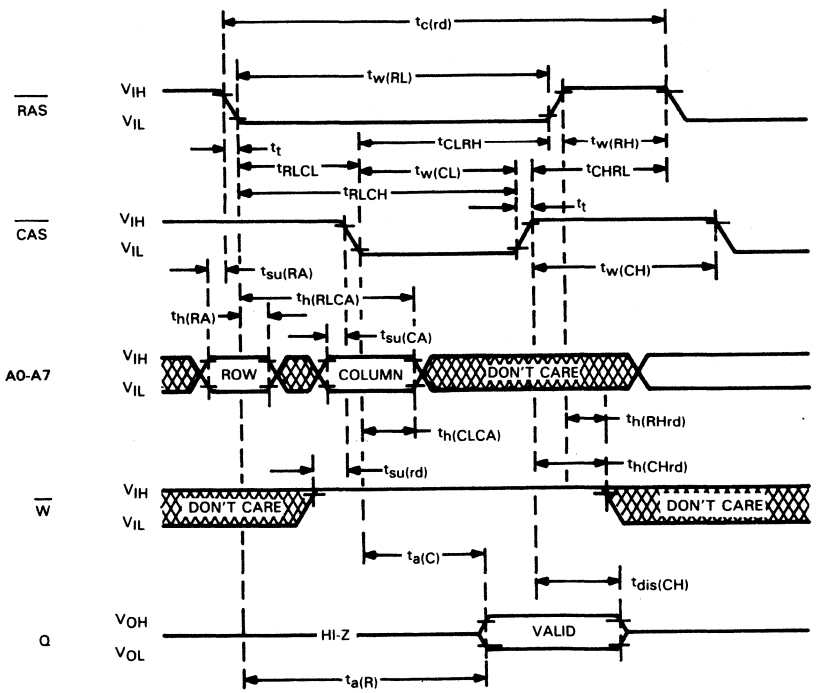
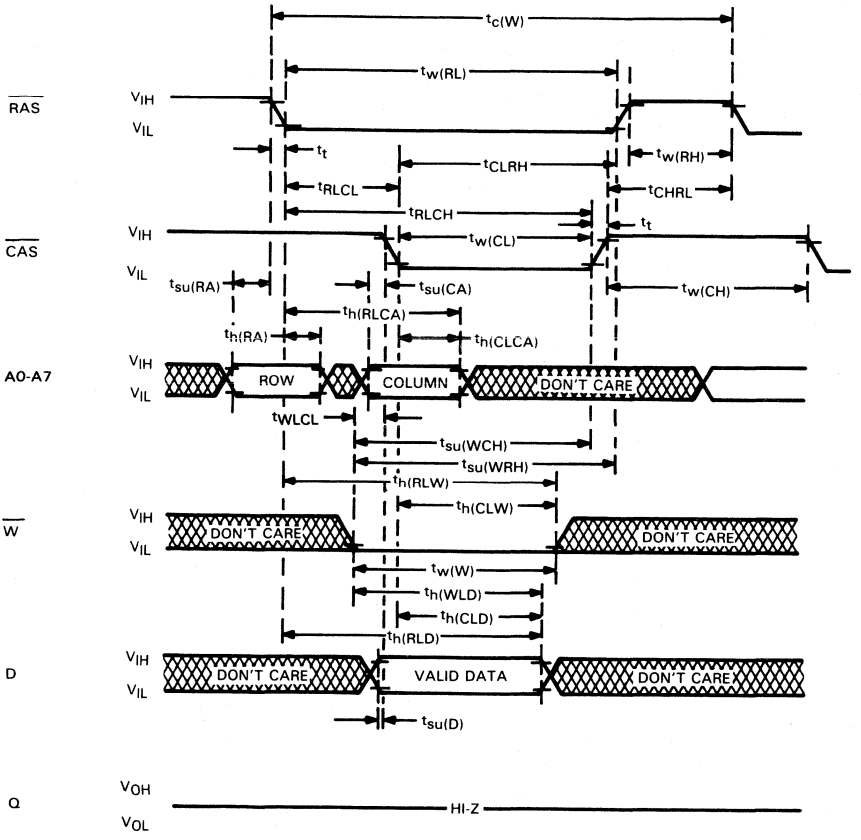


FIGURE 1 – LOAD CIRCUIT

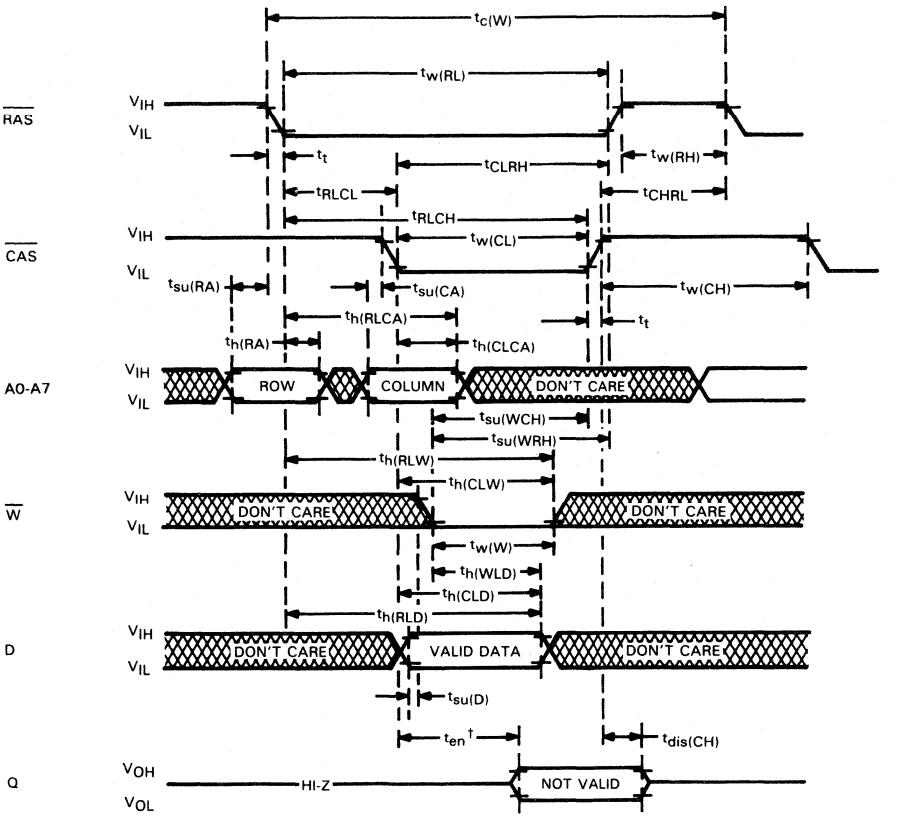
read cycle timing



early write cycle timing

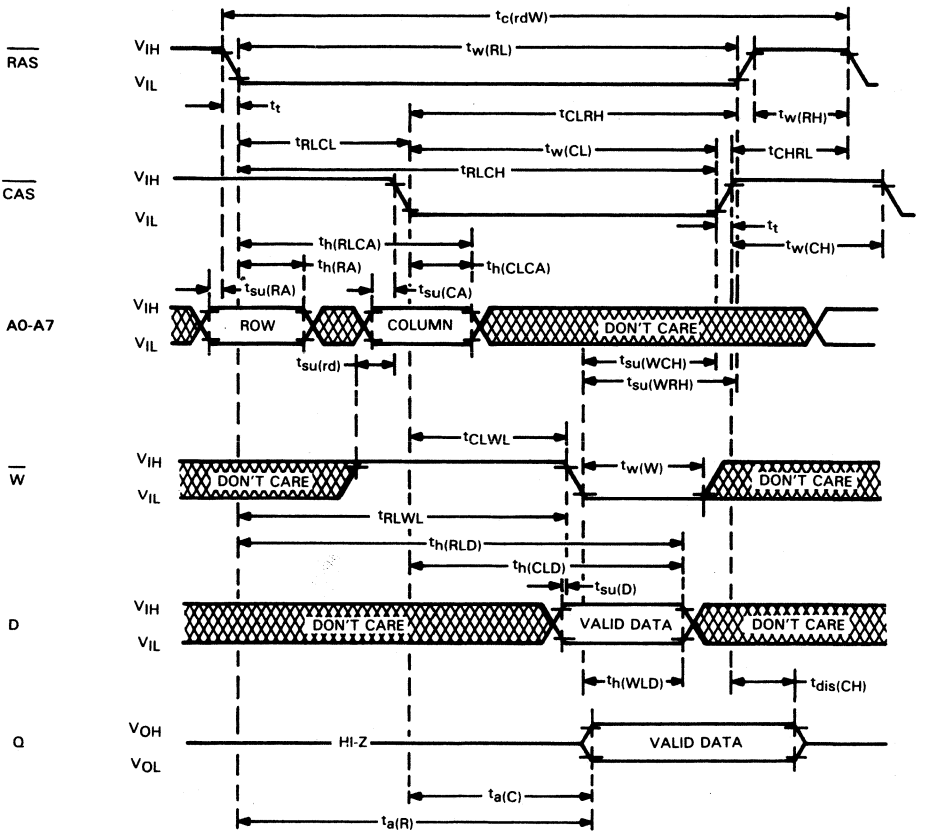


write cycle timing

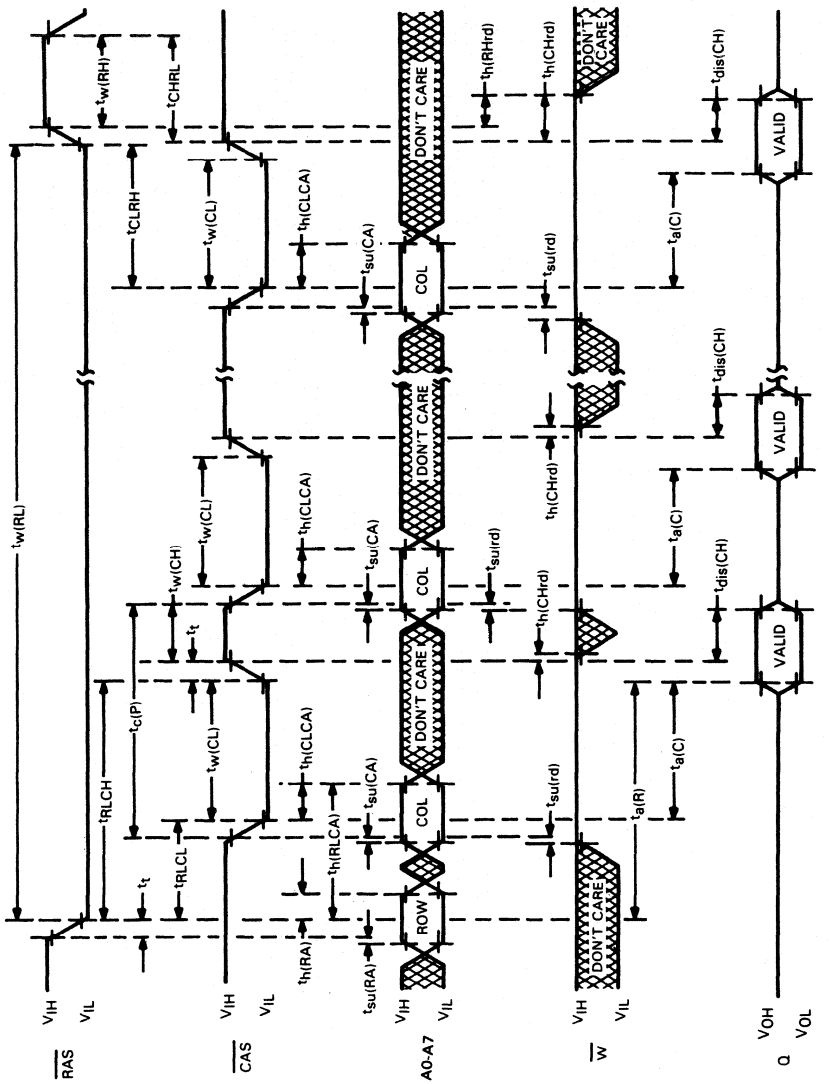


† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

read-write/read-modify-write cycle timing

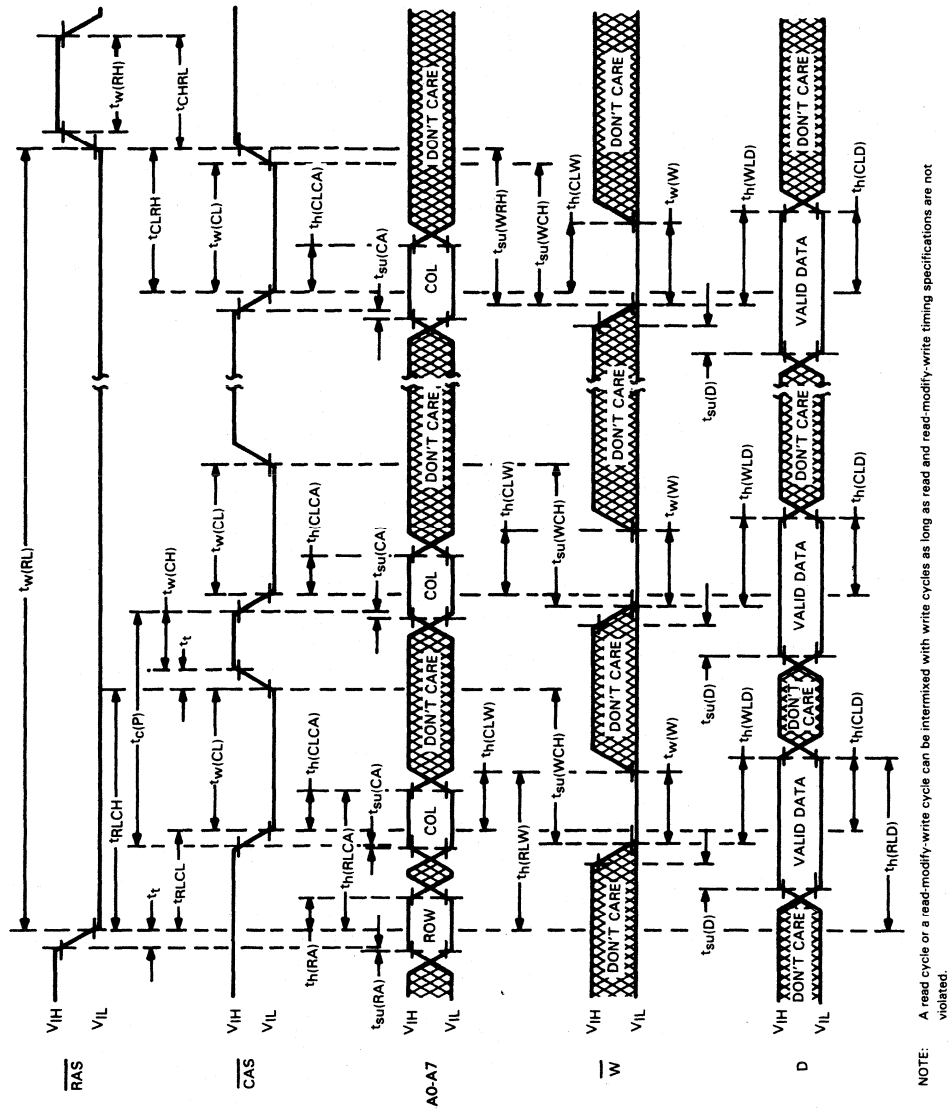


page-mode read cycle timing



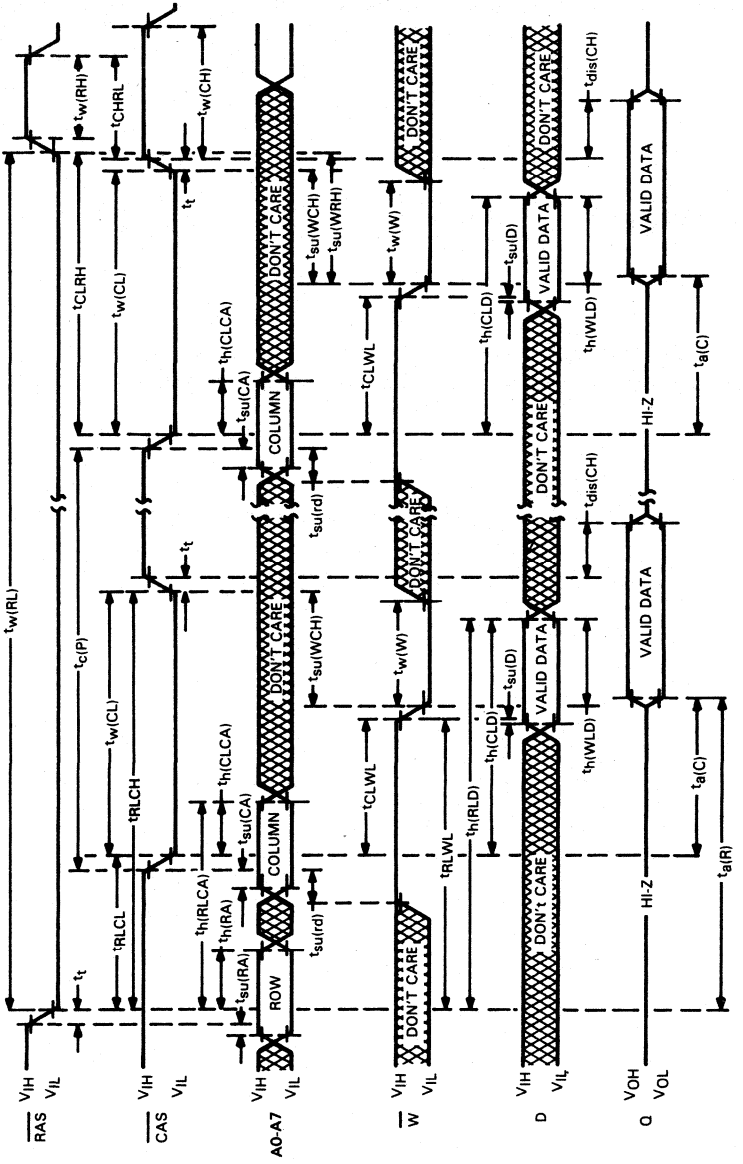
NOTE: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



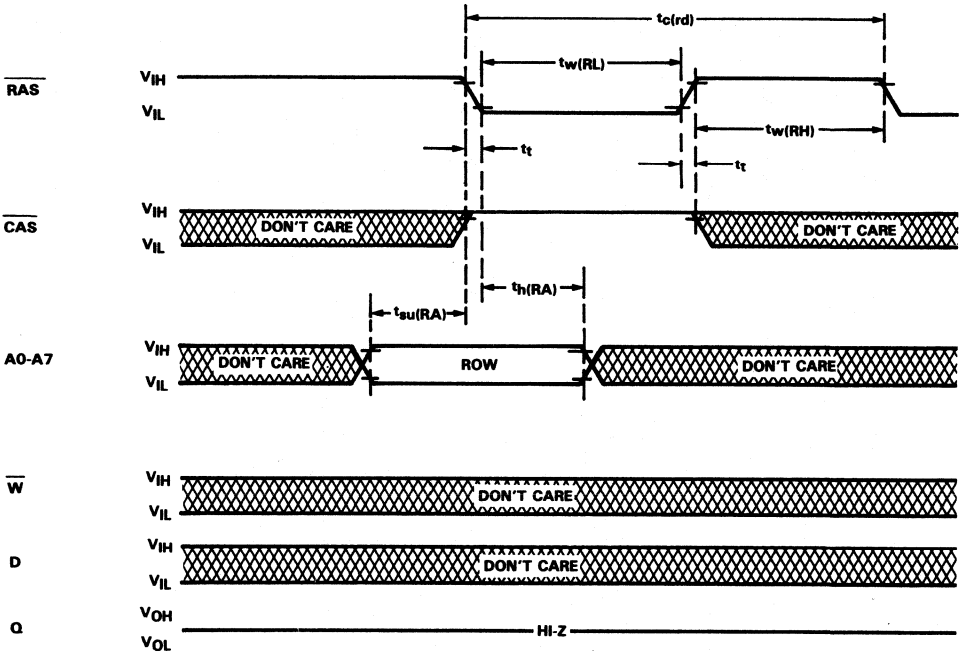
NOTE: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

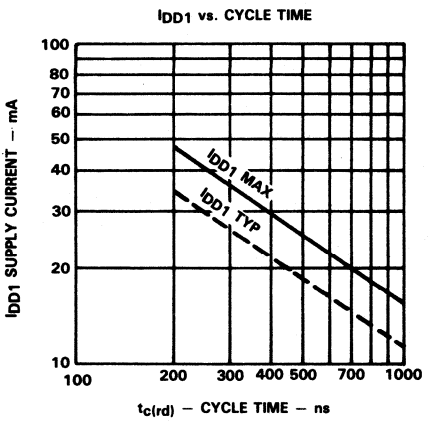
page-mode read-modify-write cycle timing

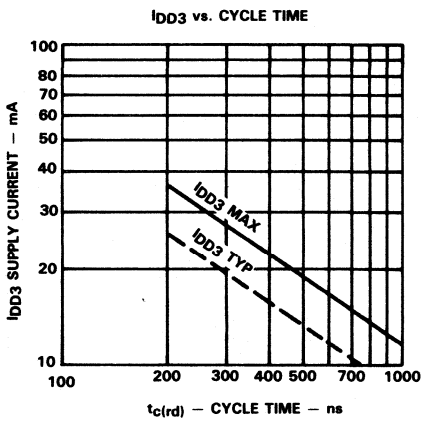


NOTE: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{\text{RAS}}$-only refresh timing







Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

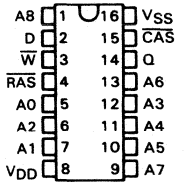
TMS4256, TMS4257
262,144-BIT DYNAMIC RANDOM-ACCESS MEMORIES

MAY 1983 – REVISED JANUARY 1984

- 262,144 X 1 Organization
- Single +5-V Supply (10% Tolerance)
- JEDEC Standardized Pin Out
- Upward Pin Compatible with TMS4164 (64K Dynamic RAM)
- Performance Ranges:

DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-10 TMS4257-10	100 ns	50 ns	200 ns
TMS4256-12 TMS4257-12	120 ns	60 ns	230 ns
TMS4256-15 TMS4257-15	150 ns	75 ns	260 ns
TMS4256-20 TMS4257-20	200 ns	100 ns	330 ns

TMS4256, TMS4257 . . . JL OR NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D	Data-In
Q	Data-Out
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Write Enable
V_{DD}	+5-V Supply
V_{SS}	Ground

- Long Refresh Period . . . 4 ms (MAX)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Common I/O Capability with "Early Write" Feature
- Page ('4256) or Nibble-Mode ('4257) Options for Faster Access Operation
- Power Dissipation As Low As:
  Operating . . . 225 mW (TYP)
  Standby . . . 12.5 mW (TYP)
- $\overline{RAS}$-Only Refresh Mode
- Hidden Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode (Optional)
- Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges in the Future

description

The '4256 and '4257 are high-speed, 262,144-bit dynamic random-access memories, organized as 262,144 words of one bit each. They employ state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

These devices feature maximum $\overline{RAS}$ access times of 100 ns, 120 ns, 150 ns, or 200 ns. Typical power dissipation is as low as 225 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single +5-V supply, reducing system power supply and decoupling

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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requirements, and easing board layout. I_{DD} peaks are 150 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The '4256 and '4257 are offered in a 16-pin dual-in-line ceramic or plastic package and are guaranteed for operation from 0°C to 70°C. These packages are designed for insertion in mounting-hole rows on 300 mil (7,62 mm) centers.

operation

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the nine column-address bits are set up on Pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified pre-charge period, similar to a "$\overline{RAS}$-only" refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh (optional)

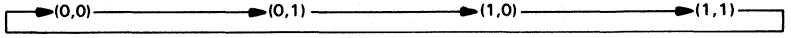
The optional $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. For devices with this option, the external address is also ignored during the hidden refresh cycles.

page-mode (TMS4256)

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{w(RL)}$, the maximum $\overline{RAS}$ low pulse width. For example, with a minimum cycle time ($t_{c(P)}$ = 100 ns) approximately 100 of the 512 columns specified by column A0 to column A8 can be accessed. Row A8 provided in the first page cycle, specifies which group of 512 columns, out of the 1024 internal columns is to be paged.

nibble-mode (TMS4257)

Nibble-mode operation allows high-speed serial read, write, or read-modify-write access of 1 to 4 bits of data. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. The next sequential nibble bits can be read or written by cycling $\overline{CAS}$ while $\overline{RAS}$ remains low. The first bit is determined by the row and column addresses, which need to be supplied only for the first access. Row A8 and column A8 provide the two binary bits for initial selection, with row A8 being the least significant address. Thereafter, the falling edge of $\overline{CAS}$ will access the next bit of the circular 4-bit nibble in the following sequence:

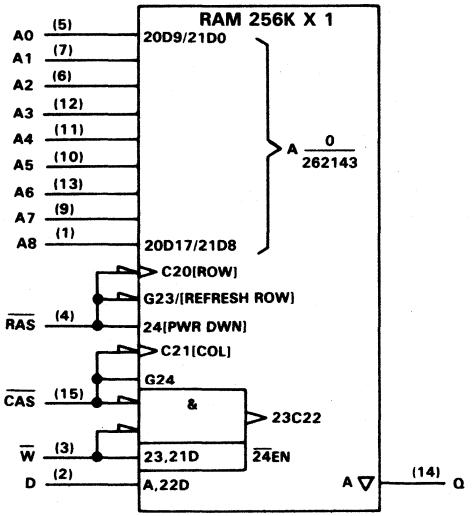


In nibble-mode, all normal memory operations (read, write, or ready-modify-write) may be performed in any desired combination.

power-up

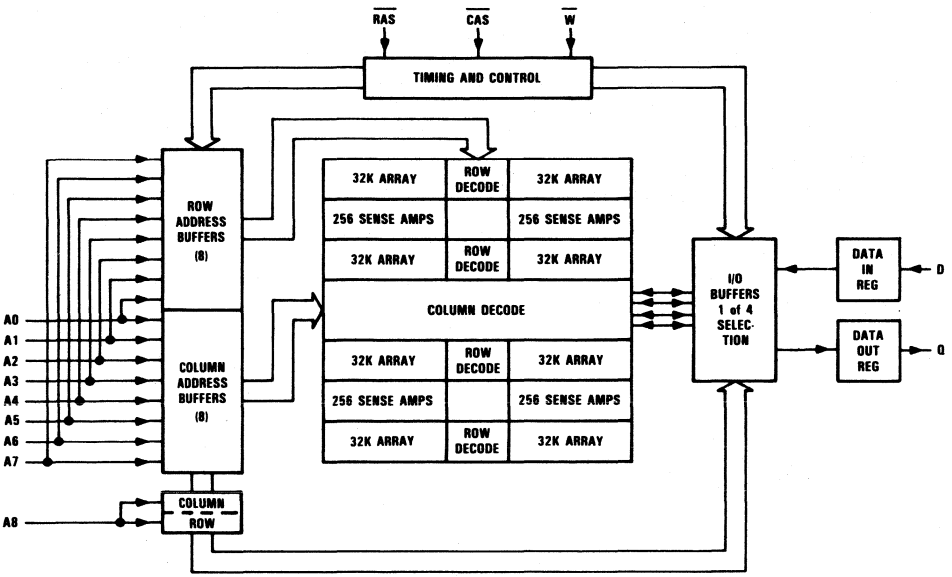
To achieve proper device operation, an initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin including V_{DD} supply (see Note 1)	−1 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.4		$V_{DD}+0.3$	V
Low-level input voltage, V_{IL} (see Note 2)	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4256-10 TMS4257-10			TMS4256-12 TMS4257-12			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=5 V, All other pins = 0 V to 5.8 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle		75	TBD		65	TBD	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2.5	5		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high		60	TBD		50	TBD	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		50	TBD		40	TBD	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45	TBD		35	TBD	mA

† All typical values are at T_A = 25°C and nominal supply voltages.

PARAMETER		TEST CONDITIONS	TMS4256-15 TMS4257-15			TMS4256-20 TMS4257-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=5 V, All other pins = 0 V to 5.8 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle		55	TBD		45	TBD	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2.5	5		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ high		45	TBD		35	TBD	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		35	TBD		25	TBD	mA
I_{DD5}	Average nibble-mode current	$t_{c(N)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		30	TBD		20	TBD	mA

† All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(D)}$	Input capacitance, data input	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	10	pF

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4256-10 TMS4257-10		TMS4256-12 TMS4257-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		50		60	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF Load = 2 Series 74 TTL gates	t_{RAC}		100		120	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4256-15 TMS4257-15		TMS4256-20 TMS4257-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		75		100	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		150		200	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	35	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4256-10 TMS4257-10		TMS4256-12 TMS4257-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	100		120		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	135		165		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	200		230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	200		230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	235		270		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	40		50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	40		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	50	10,000	60	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	90		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	100	10,000	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	35		40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	30		40		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	30		40		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	15		15		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	70		80		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	30		35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	80		95		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		35		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	30		35		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	80		95		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	20		25		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	50		60		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	20		25		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	50		60		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	50	25	60	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	100		120		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

¶ $\overline{CAS}$ before $\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	ALT. SYMBOL	TMS4256-15 TMS4257-15		TMS4256-20 TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time (read or write cycle)	t_{PC}	145		190		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	190		245		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	305		370		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	60		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	75	10,000	100	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	25		45		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	100		145		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	120		155		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	120		155		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	75		100		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{CWD}	70		90		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	75	30	100	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)	t_{RWD}	145		175		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

NOTE: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

† All cycle times assume t_t = 5 ns.

‡ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$). This applies to page-mode read-modify-write also.

§ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).

¶ $\overline{CAS}$ before $\overline{RAS}$ refresh option only.

NIBBLE MODE CYCLE

switching characteristics over recommended supply voltage range and operating free-air temperature range (unless otherwise noted)

PARAMETER		ALT. SYMBOL	TMS4257-10		TMS4257-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble mode access time from $\overline{CAS}$	t_{NCAC}	25		30		ns

PARAMETER		ALT. SYMBOL	TMS4257-15		TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(CN)}$	Nibble mode access time from $\overline{CAS}$	t_{NCAC}	40		50		ns

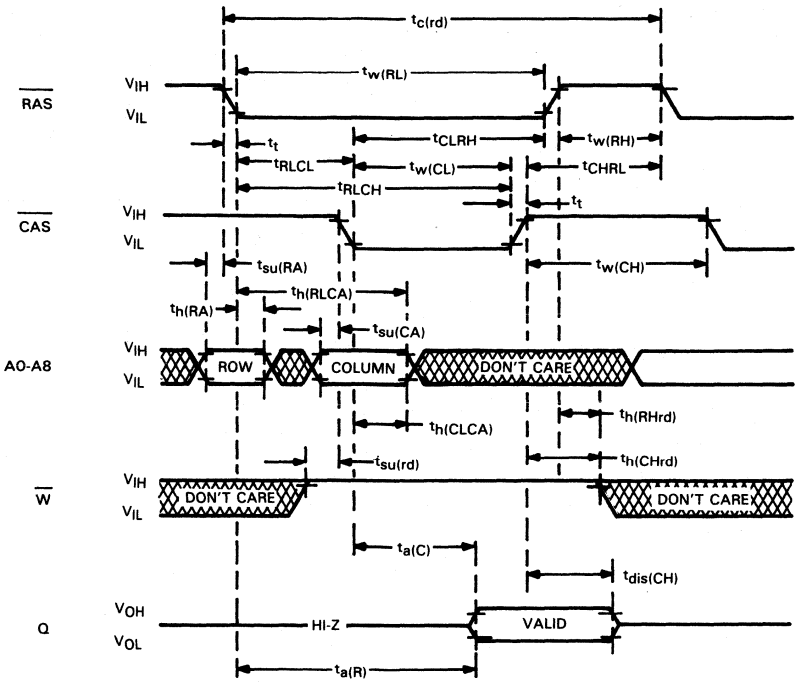
timing requirements over recommended supply voltage range and operating free-air temperature range (unless otherwise noted)

PARAMETER		ALT. SYMBOL	TMS4257-10		TMS4257-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble mode cycle time	t_{NC}	50		60		ns
$t_{c(rdWN)}$	Nibble mode read-modify-write cycle time	t_{NRMW}	70		85		
t_{CLRHN}	Nibble mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	25		30		
t_{CLWLN}	Nibble mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	20		25		
$t_{w(CLN)}$	Nibble mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	25		30		
$t_{w(CHN)}$	Nibble mode pulse duration, $\overline{CAS}$ high	t_{NCP}	15		20		
$t_{su(WCHN)}$	Nibble mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	20		25		

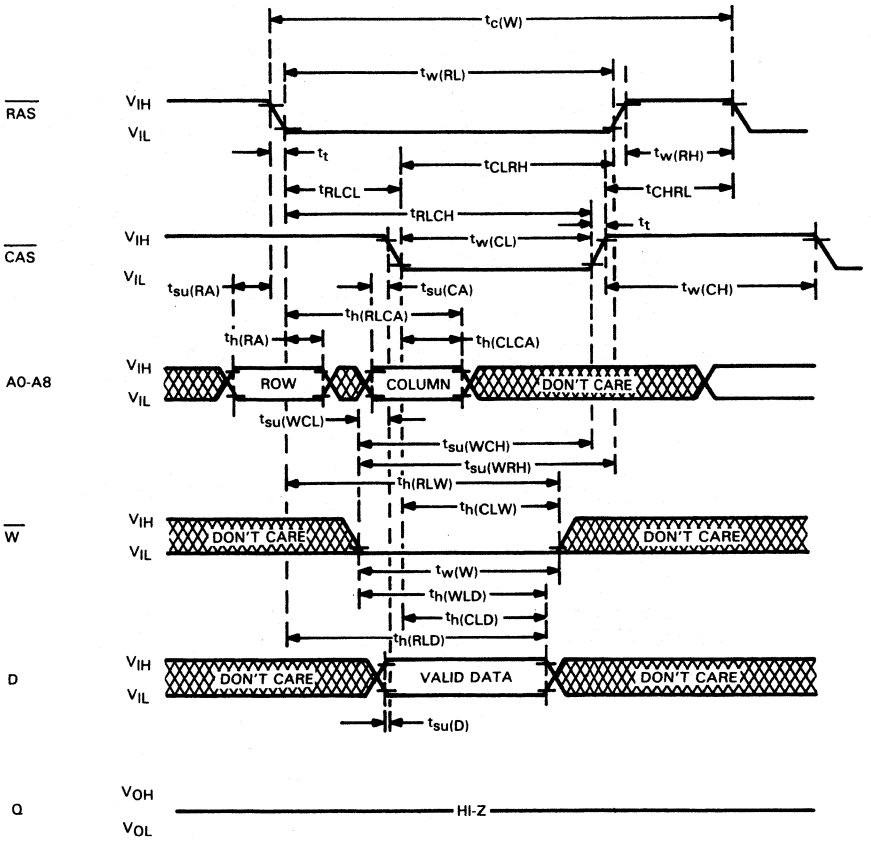
timing requirements over recommended supply voltage range and operating free-air temperature range (unless otherwise noted)

PARAMETER		ALT. SYMBOL	TMS4257-15		TMS4257-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(N)}$	Nibble mode cycle time	t_{NC}	75		90		ns
$t_{c(rdWN)}$	Nibble mode read-modify-write cycle time	t_{NRMW}	105		130		
t_{CLRHN}	Nibble mode delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{NRSH}	40		50		
t_{CLWLN}	Nibble mode delay time, $\overline{CAS}$ to $\overline{W}$ delay	t_{NCWD}	30		40		
$t_{w(CLN)}$	Nibble mode pulse duration, $\overline{CAS}$ low	t_{NCAS}	40		50		
$t_{w(CHN)}$	Nibble mode pulse duration, $\overline{CAS}$ high	t_{NCP}	25		30		
$t_{su(WCHN)}$	Nibble mode write command setup time before $\overline{CAS}$ high	t_{NCWL}	35		45		

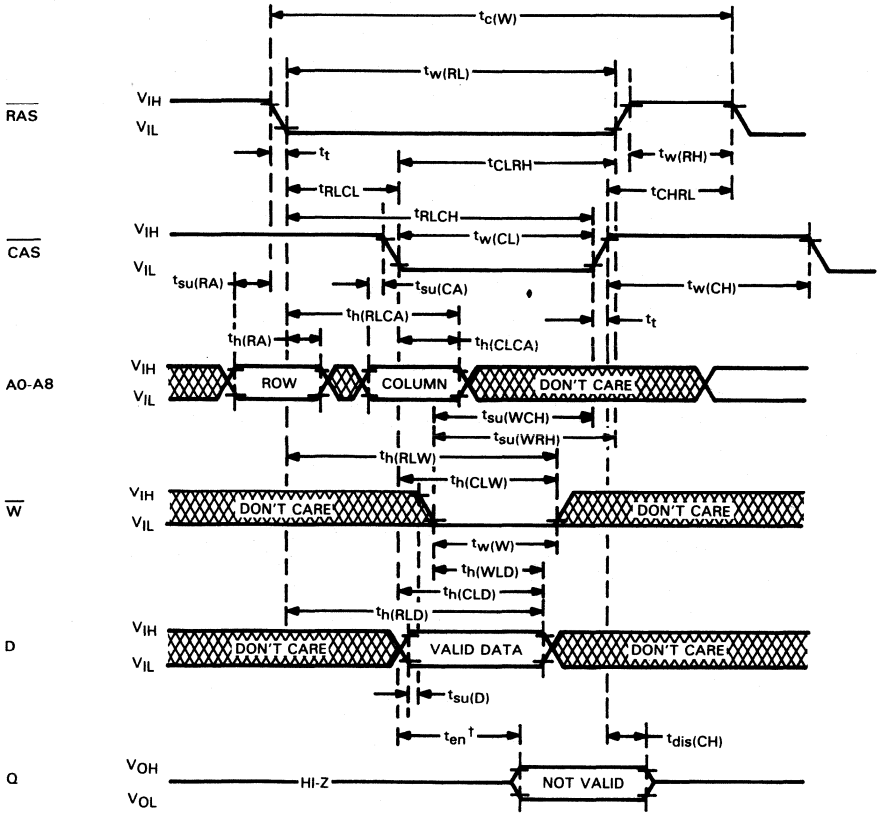
read cycle timing



early write cycle timing

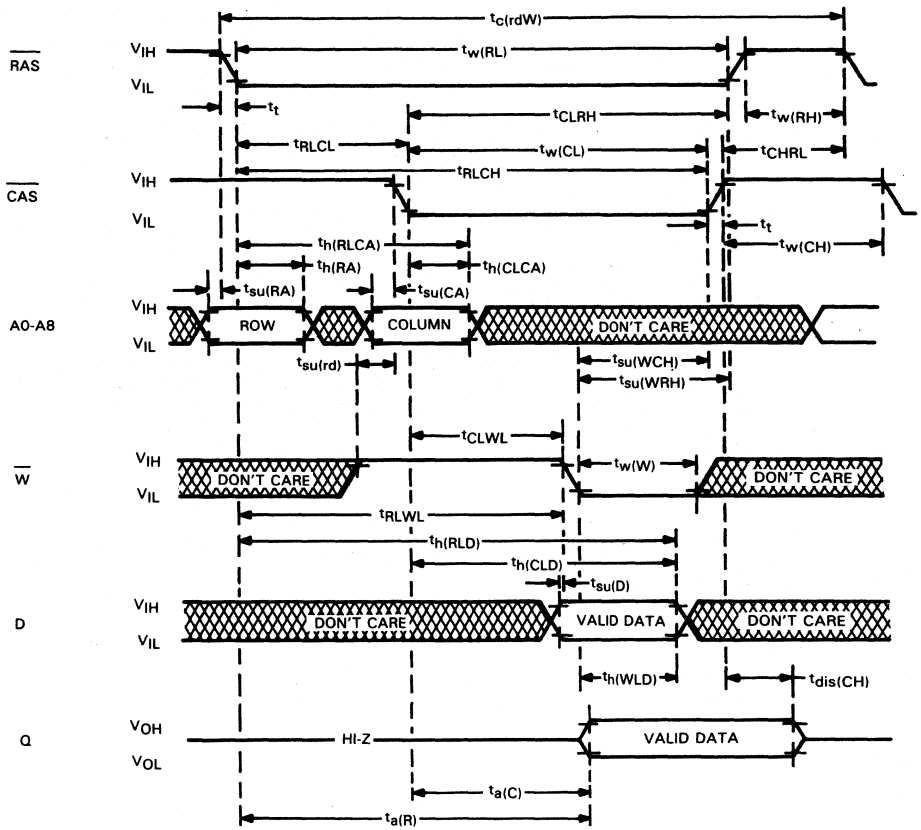


write cycle timing

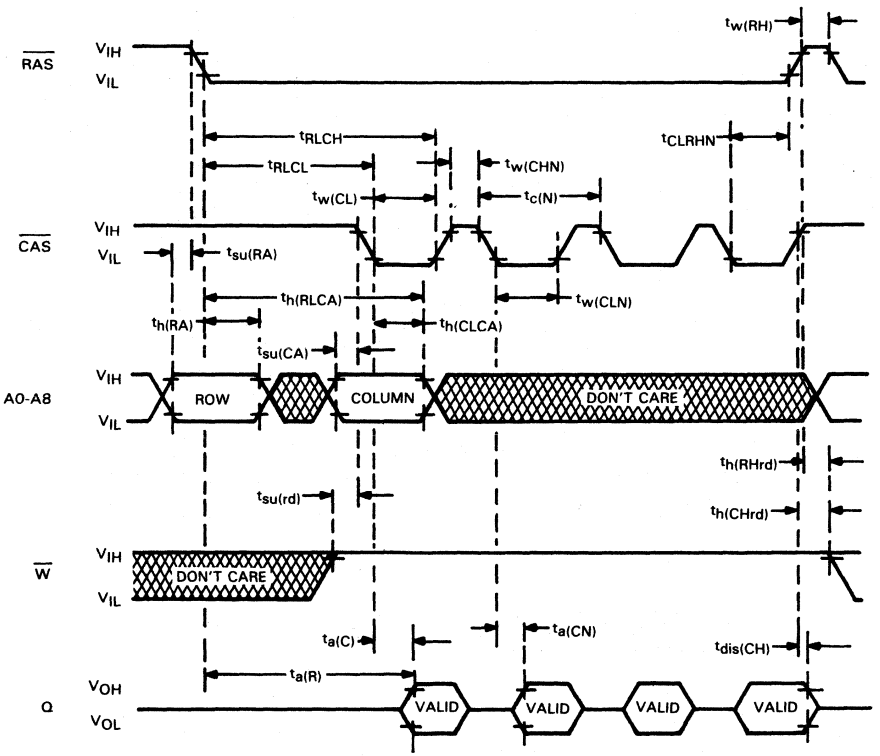


† The enable time (t_{en}) for a write cycle is equal in duration to the access time from $\overline{CAS}$ ($t_{a(C)}$) in a read cycle; but the active levels at the output are invalid.

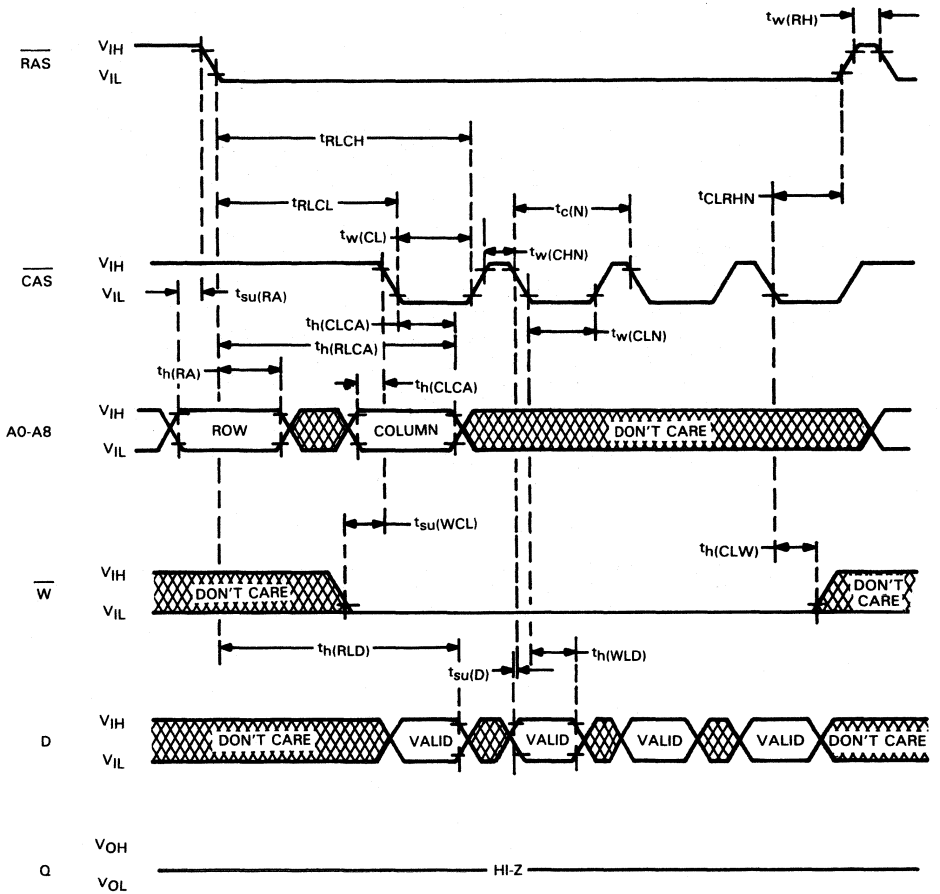
read-write/read-modify-write cycle timing



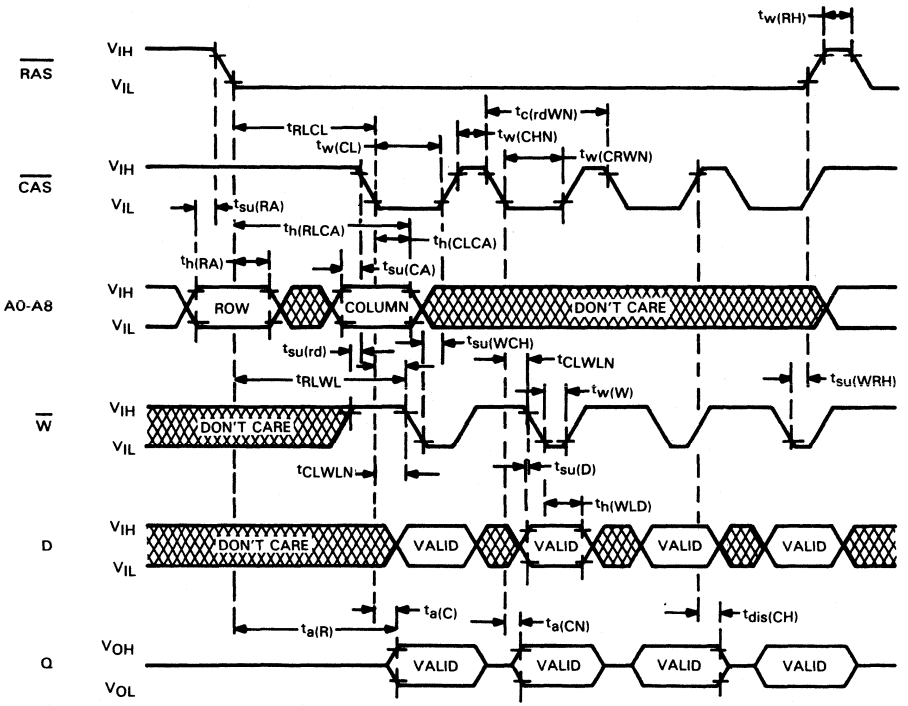
nibble mode read cycle timing



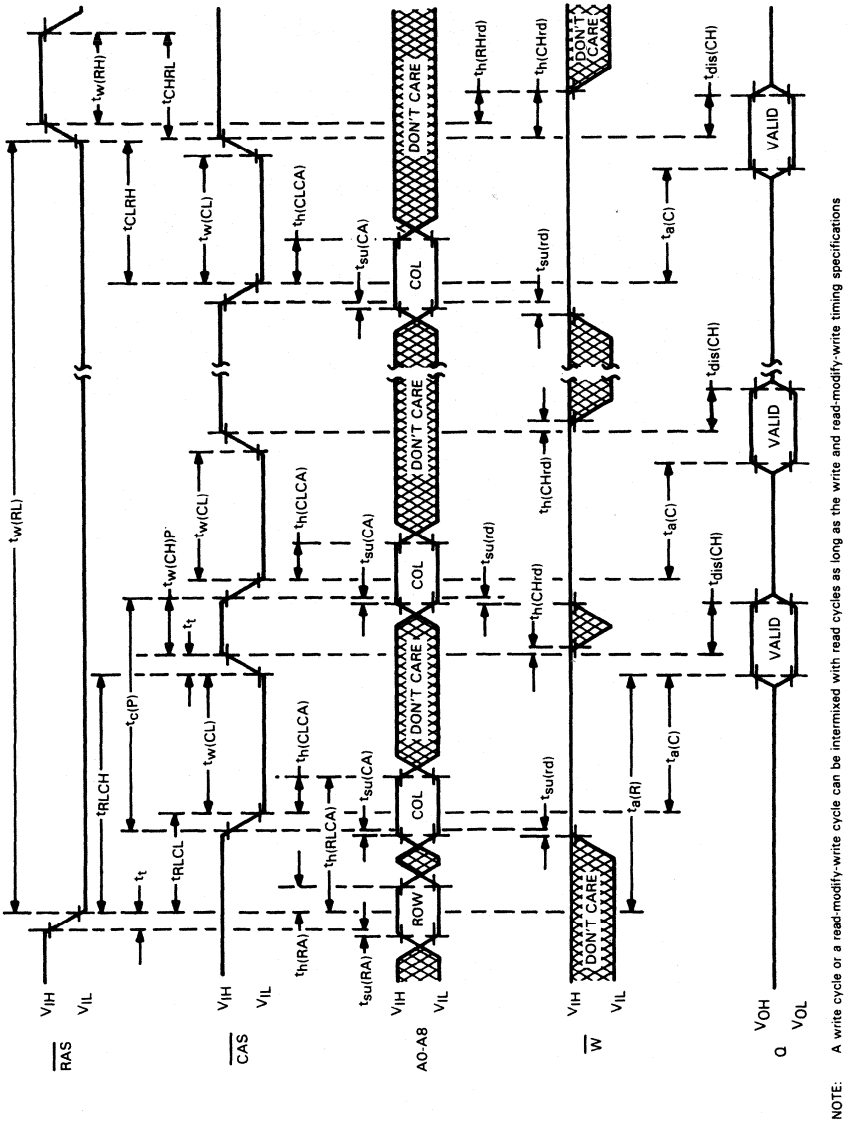
nibble mode write cycle timing



nibble mode read-modify-write-cycle timing

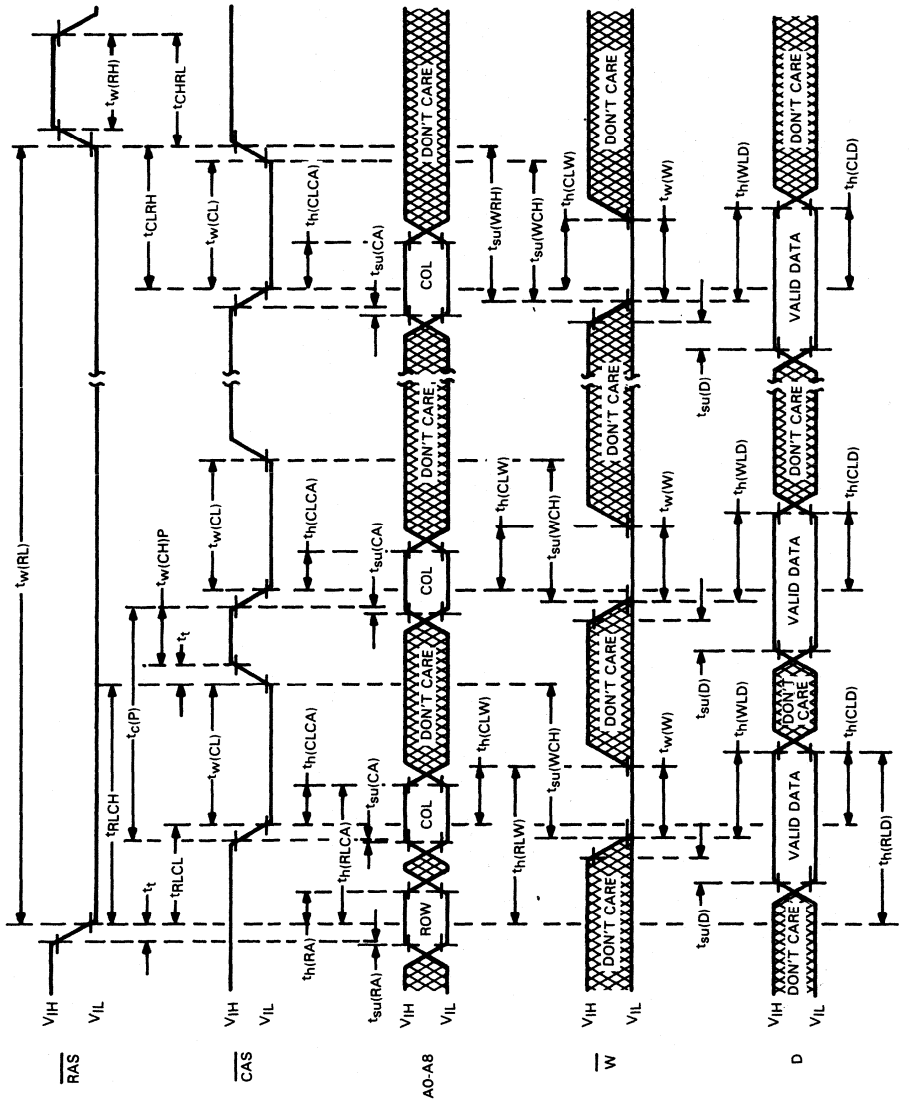


page-mode read cycle timing



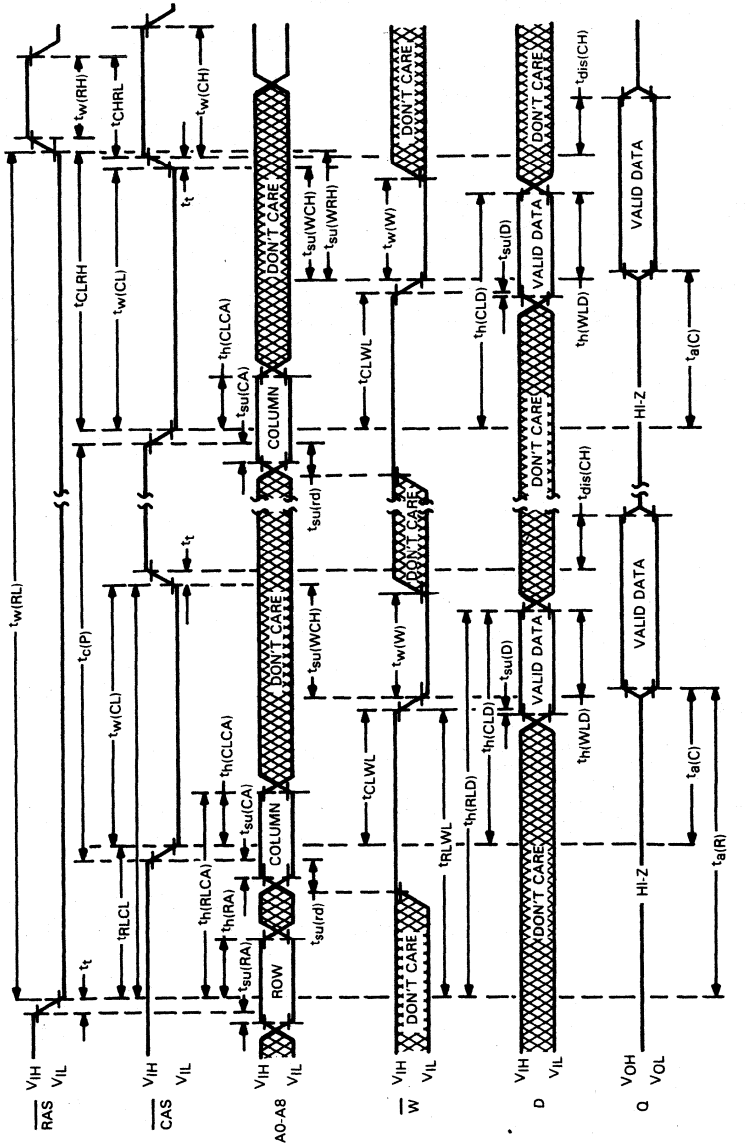
NOTE: A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



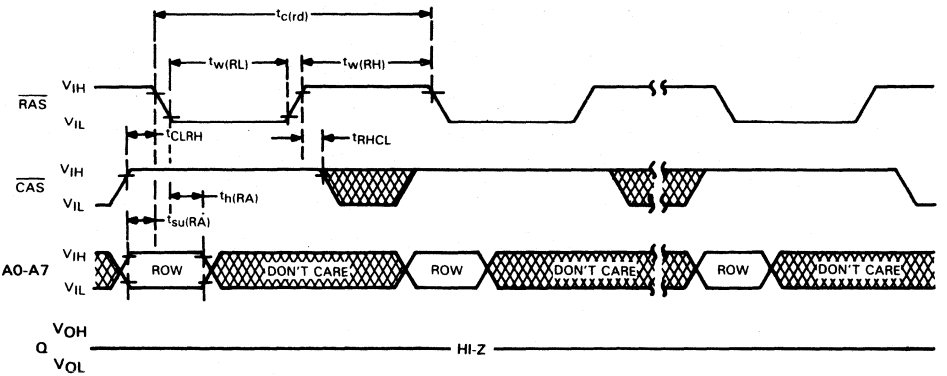
NOTE: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page-mode read-modify-write cycle timing

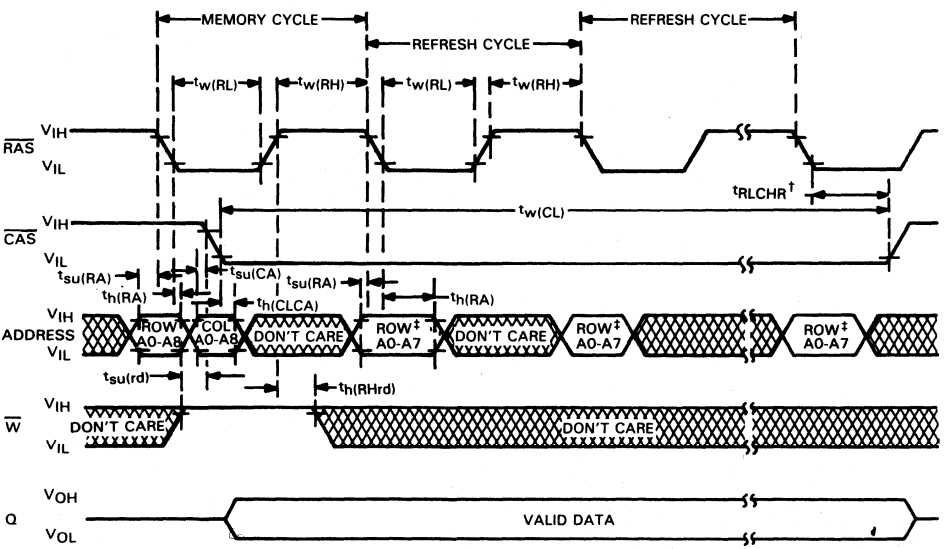


NOTE: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

$\overline{RAS}$-only refresh cycle timing

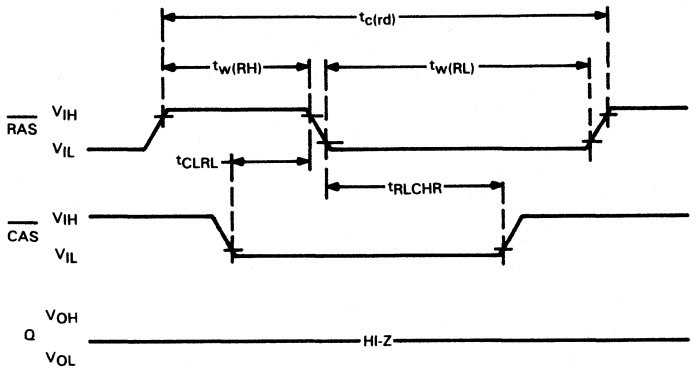


hidden refresh cycle timing



† For devices with $\overline{CAS}$ before $\overline{RAS}$ refresh option only.
‡ Row address is required only for devices without $\overline{CAS}$ before $\overline{RAS}$ refresh option. Row address is "don't care" for devices with the $\overline{CAS}$ before $\overline{RAS}$ refresh option.

automatic ($\overline{CAS}$ before $\overline{RAS}$) refresh cycle timing



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS4416, SMJ4416
16,384-WORD BY 4-BIT DYNAMIC RAM

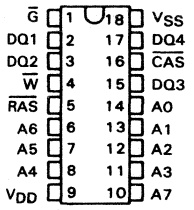
AUGUST 1980 – REVISED JANUARY 1984

- 16,384 X 4 Organization
- Single +5-V Supply (10% Tolerance)
- Performance Ranges:

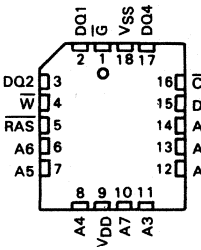
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4416-12	120 ns	70 ns	230 ns	320 ns
'4416-15	150 ns	80 ns	260 ns	330 ns
'4416-20	200 ns	120 ns	330 ns	440 ns

- Available Temperature Ranges*:
  - S . . . −55°C to 100°C
  - E . . . −40°C to 85°C
  - L . . . 0°C to 70°C
- Long Refresh Period . . . 4 milliseconds
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  - Operating . . . 200 mW (TYP)
  - Standby . . . 17.5 mW (TYP)
- New SMOS (Scaled-MOS) N-Channel Technology

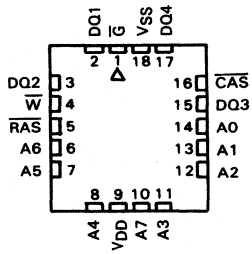
TMS4416 . . . NL PACKAGE
SMJ4416 . . . JD PACKAGE
(TOP VIEW)



TMS4416 . . . FPL PACKAGE
(TOP VIEW)



SMJ4416 . . . FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The '4416 is a high-speed, 65,536-bit, dynamic, random-access memory, organized as 16,384 words of 4 bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The '4416 features $\overline{RAS}$ access times to 120 ns maximum. Power dissipation is 200 mW typical operating, 17.5 mW typical standby.

New SMOS technology permits operation from a single +5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks have been reduced to 60 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations. Input clamp diodes are used to ease system design.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

* M temperature range (−55°C to 125°C) to be available in future.

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.
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The TMS4416 is offered in 18-pin plastic dual-in line and 18-pin plastic chip carrier packages. It is guaranteed for operation from 0°C to 70°C. The SMJ4416 is offered in 18-pin ceramic side-braze dual-in-line and 18-pin ceramic chip carrier packages. It is available in −55°C to 100°C and −40°C to 85°C temperature ranges. Dual-in-line packages are designed for insertion in mounting-hole rows on 300-mil (7,62 mm) centers.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state allowing a write cycle with $\overline{G}$ grounded.

data-in (DQ1 through DQ4)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referrenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data-out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 54/74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(E)}$ are satisified. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will reamin in the low impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

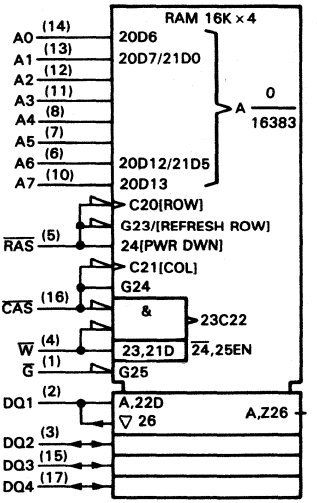
page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 16K × 4 RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power-up

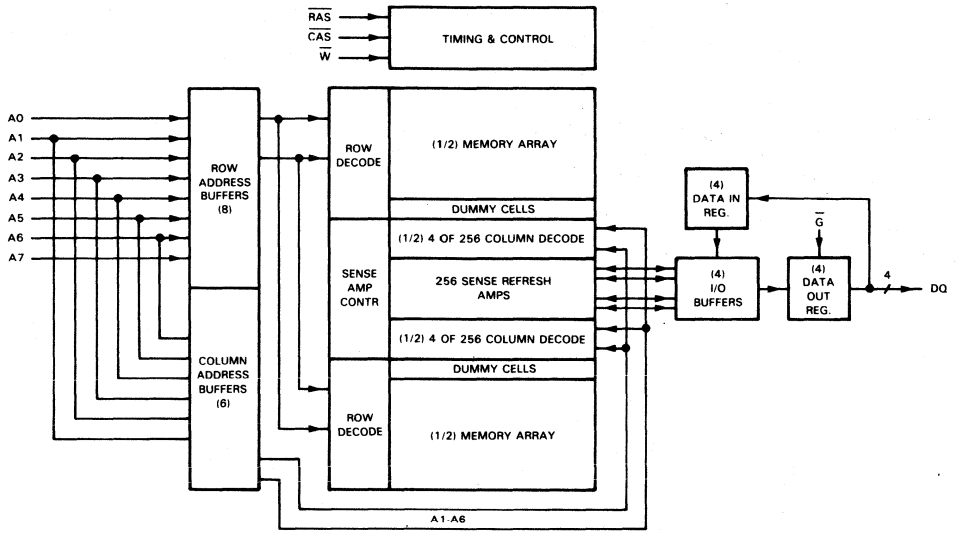
After power-up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . −1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . −1 V to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range: TMS' . . . . . 0°C to 70°C
Operating case temperature range: SMJ' – S version . . . . . −55°C to 100°C
– E version . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

PARAMETER		TMS4416			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{DD}		4.5	5	5.5	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}	V_{DD} = 4.5 V	2.4		4.8	V
	V_{DD} = 5.5 V	2.4		5.8	
Low-level input voltage, V_{IL} (see Note 2)		V_{IK}		0.8	V
Operating free-air temperature, T_A		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4416-12			UNIT
			MIN	TYP†	MAX	
V_{IK}	Input clamp voltage	I_I = −15 mA, see Figure 1			−1.2	V
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	At t_c = minimum cycle			54	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high			46	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling			46	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡V_{IL} ≥ −0.6 V on all inputs.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4416-15			TMS4416-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage	I_I = −15 mA, see Figure 1			−1.2			−1.2	V
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	At t_c = minimum cycle		40	48		35	42	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5		3.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		25	40		21	34	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		25	40		21	34	mA

†All typical values are at T_A = 25°C and nominal supply voltages.
‡$V_{IL} \geq -0.6$ V on all inputs.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TMS4416		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	5	7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
$C_{i/o}$	Input/output capacitance, data ports	8	10	pF

†All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4416-12		UNIT
				MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF Load = 2 Series 74 TTL gates	t_{RAC}		120	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates			30	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates		0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4416-15		TMS4416-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		80		120	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF Load = 2 Series 74 TTL gates	t_{RAC}		150		200	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates			40		50	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	40	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates		0	30	0	40	ns

timing requirements over recommended supply voltage range and operating free-air temperature range

	PARAMETER	ALT. SYMBOL	TMS4416-12 MIN	TMS4416-12 MAX	UNIT
$t_{c(P)}$	Page mode cycle time	t_{PC}	120		ns
$t_{c(rd)}$	Read cycle time*	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	320		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)**	t_{CP}	40		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low†	t_{CAS}	70	10,000	ns
$t_{w(RH)}$	Pulse width $\overline{RAS}$ high (precharge time)	t_{RP}	80		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low‡	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	30		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	50		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	50		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	35		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	85		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	100		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	40		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	100		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	80		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)***	t_{CWD}	120		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)***	t_{RWD}	170		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ		30		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

* Note: All cycle times assume $t_t = 5$ ns.

** Page mode only.

*** Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

† In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.

‡ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4416-15		TMS4416-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	140		210		ns
$t_{c(rd)}$	Read cycle time*	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	360		440		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)**	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low†	t_{CAS}	80	10,000	120	10,000	ns
$t_{w(RH)}$	Pulse width $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low‡	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		50		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	40		50		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	110		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	130		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		50		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	130		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	80		120		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)***	t_{CWD}	120		150		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	70	25	80	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)***	t_{RWD}	190		230		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ		30		40		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

* Note: All cycle times assume t_t = 5 ns.

** Page mode only.

*** Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

† In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.

‡ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.

recommended operating conditions

PARAMETER		SMJ4416 S VERSION MIN	SMJ4416 S VERSION NOM	SMJ4416 S VERSION MAX	SMJ4416 E VERSION MIN	SMJ4416 E VERSION NOM	SMJ4416 E VERSION MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{SS}			0			0		V
High-level input voltage, V_{IH}	V_{DD} = 4.5 V	2.4		4.8	2.4		4.8	V
	V_{DD} = 5.5 V	2.4		5.8	2.4		5.8	
Low-level input voltage, V_{IL} (see Note 2)		V_{IK}		0.8	V_{IK}		0.8	V
Operating case temperature, T_C		−55		100	−40		85	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4416-12 MIN	SMJ4416-12 TYP†	SMJ4416-12 MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −15 mA, see Figure 1			−1.2	V
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10	μA
I_{DD1}	Average operating current during read or write cycle	At t_c = minimum cycle			54	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high			46	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling			46	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡$V_{IL} \geq -0.6$ V on all inputs.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ4416-15			SMJ4416-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp voltage	I_I = −15 mA, see Figure 1			−1.2			−1.2	V
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	At t_c = minimum cycle		40	48		35	42	mA
I_{DD2}‡	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5		3.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		25	40		21	34	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		25	40		21	34	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡V_{IL} ≥ −0.6 V on all inputs.

capacitance over recommended supply voltage range and operating case temperature range, f = 1 MHz

PARAMETER		SMJ4416		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	5	7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
$C_{i/o}$	Input/output capacitance, data ports	8	10	pF

†All typical values are at T_C = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating case temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4416-12 MIN	SMJ4416-12 MAX	UNIT
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF Load = 2 Series 74 TTL gates	t_{RAC}		120	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates			30	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates		0	30	ns

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4416-15 MIN	SMJ4416-15 MAX	SMJ4416-20 MIN	SMJ4416-20 MAX	UNIT
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		80		120	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF Load = 2 Series 74 TTL gates	t_{RAC}		150		200	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates			40		50	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	40	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates		0	30	0	40	ns

timing requirements over recommended supply voltage range and operating case temperature range

PARAMETER		ALT. SYMBOL	SMJ4416-12 MIN	SMJ4416-12 MAX	UNIT
$t_{c(P)}$	Page mode cycle time	t_{PC}	120		ns
$t_{c(rd)}$	Read cycle time*	t_{RC}	230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	320		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)**	t_{CP}	40		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low†	t_{CAS}	70	10,000	ns
$t_{w(RH)}$	Pulse width $\overline{RAS}$ high (precharge time)	t_{RP}	80		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low‡	t_{RAS}	120	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	30		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	50		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	50		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	35		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	15		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	85		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	40		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	100		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	40		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	100		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	80		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)***	t_{CWD}	120		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)***	t_{RWD}	170		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ		30		ns
t_{rf}	Refresh time interval	t_{REF}		4	ms

* Note: All cycle times assume $t_t = 5$ ns.

** Page mode only.

***Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

†In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.

‡In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.

timing requirements over recommended supply voltage range and operating case temperature range

PARAMETER		ALT. SYMBOL	SMJ4416-15		SMJ4416-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	140		210		ns
$t_{c(rd)}$	Read cycle time*	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	360		440		ns
$t_{w(CH)}$	Pulse width, $\overline{CAS}$ high (precharge time)**	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse width, $\overline{CAS}$ low†	t_{CAS}	80	10,000	120	10,000	ns
$t_{w(RH)}$	Pulse width $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse width, $\overline{RAS}$ low‡	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	40		50		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	40		50		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	110		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	60		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	130		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		50		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	60		80		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	130		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	80		120		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)***	t_{CWD}	120		150		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	20	70	25	80	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read, modify-write-cycle only)***	t_{RWD}	190		230		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ		30		40		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

* Note: All cycle times assume t_t = 5 ns.

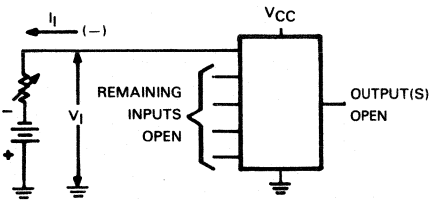
** Page mode only.

*** Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

† In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.

‡ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.

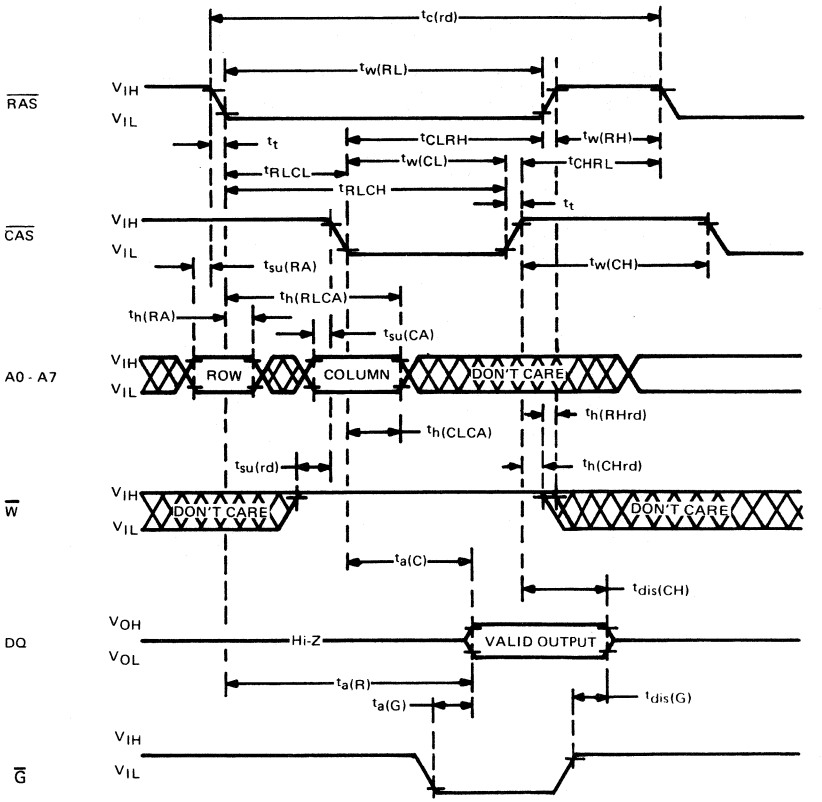
PARAMETER MEASUREMENT INFORMATION



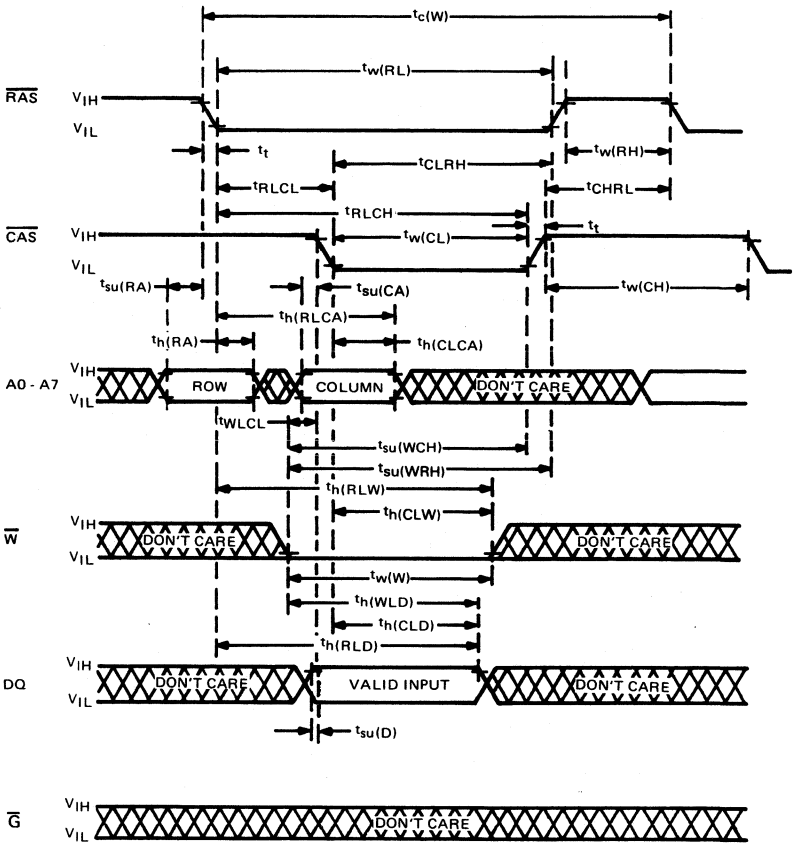
NOTE: Each input is tested separately.

FIGURE 1 — INPUT CLAMP VOLTAGE TEST CIRCUIT

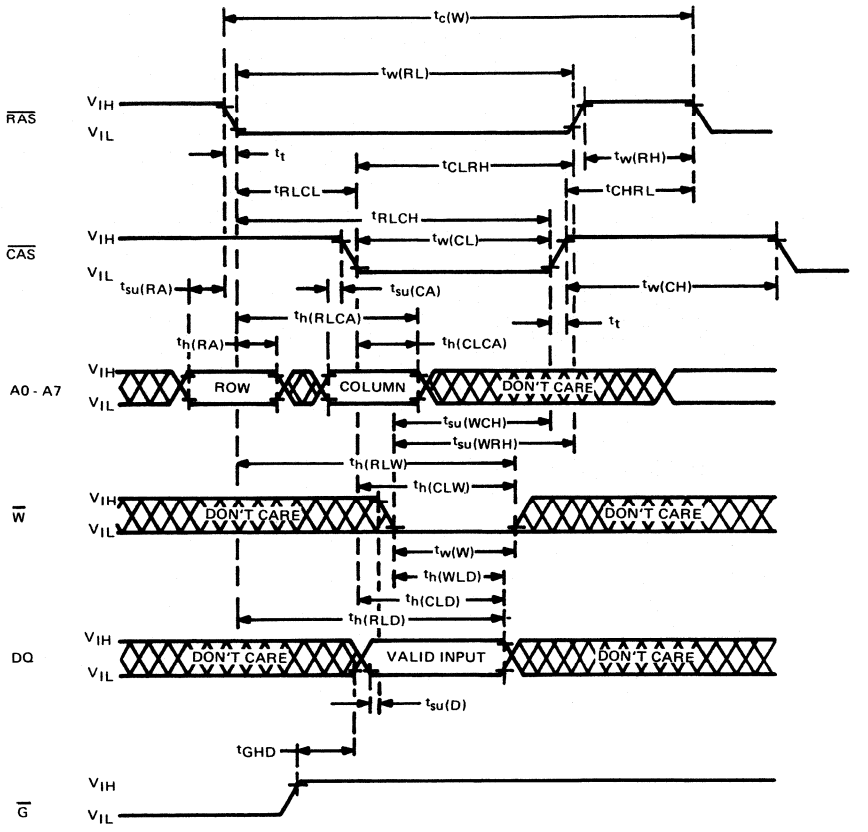
read cycle timing



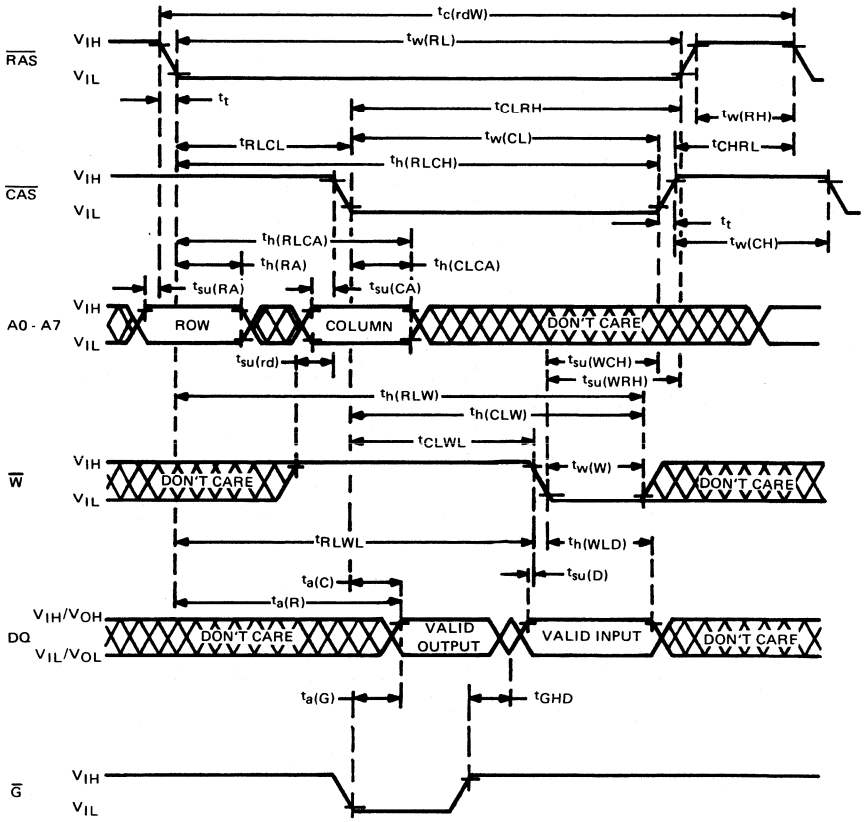
early write cycle timing



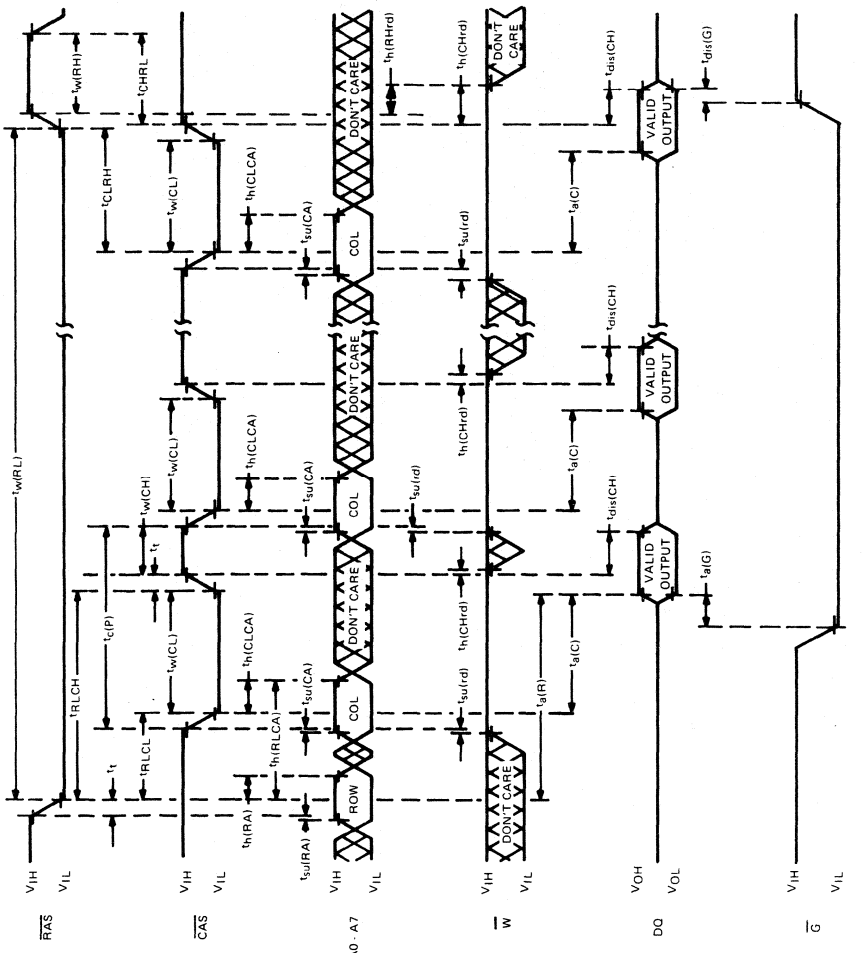
write cycle timing



read-write/read-modify-write cycle timing

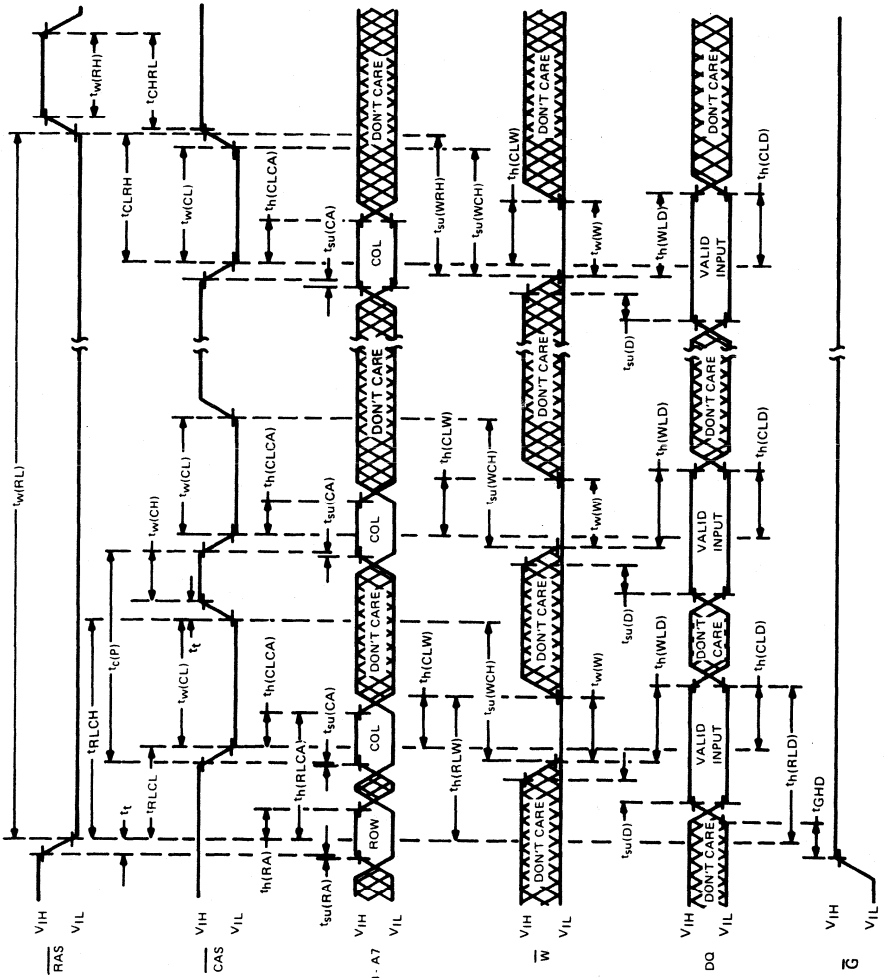


page-mode read cycle timing



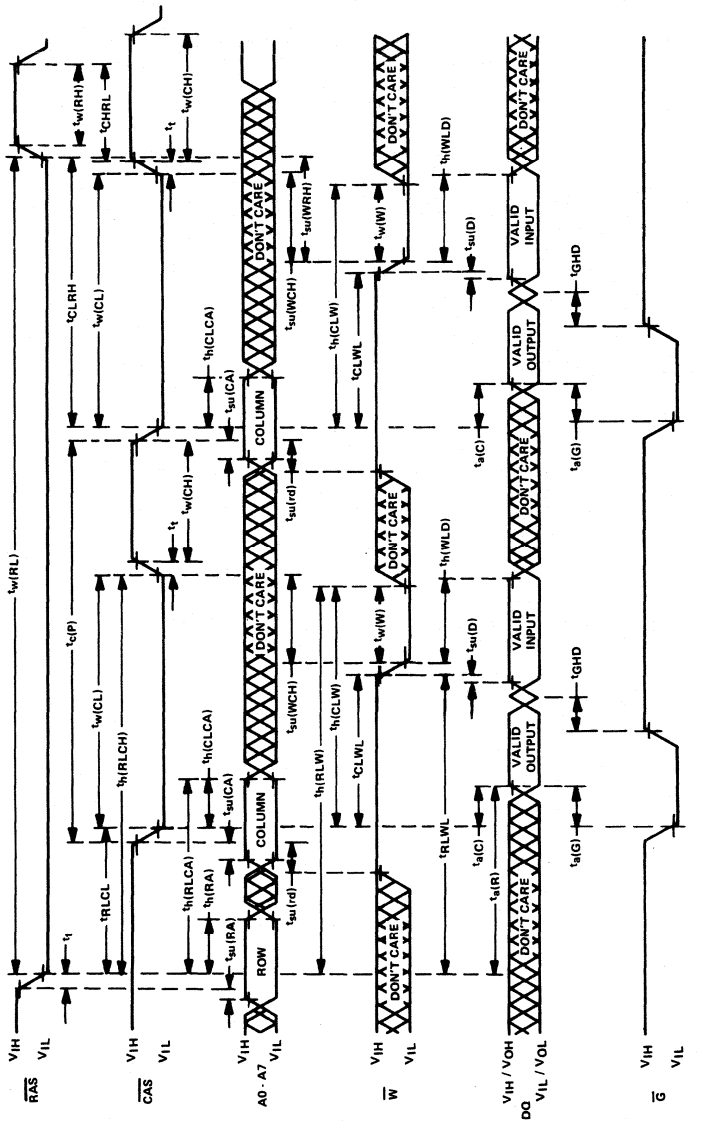
NOTE: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

page-mode write cycle timing



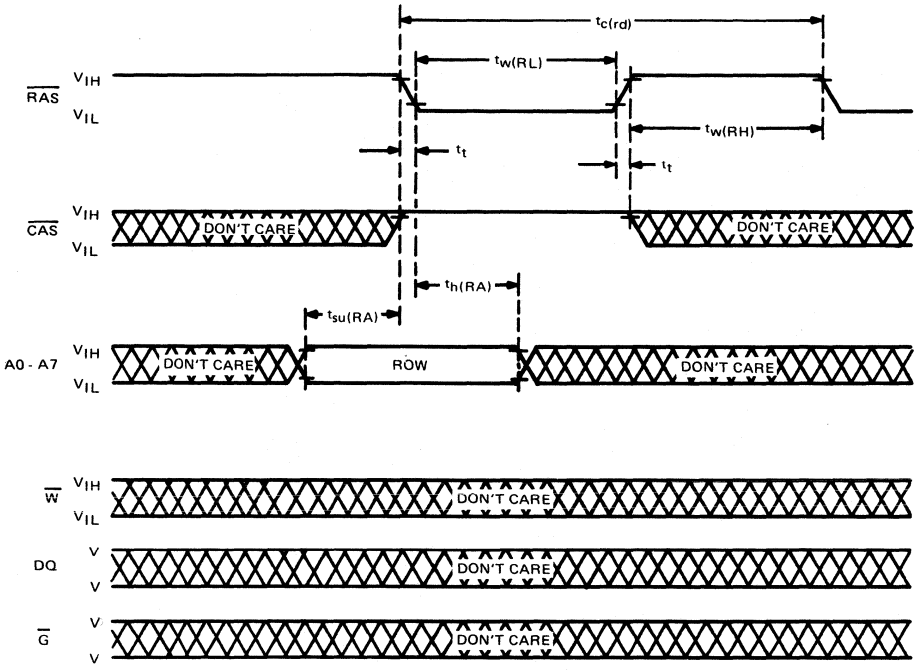
NOTE: A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

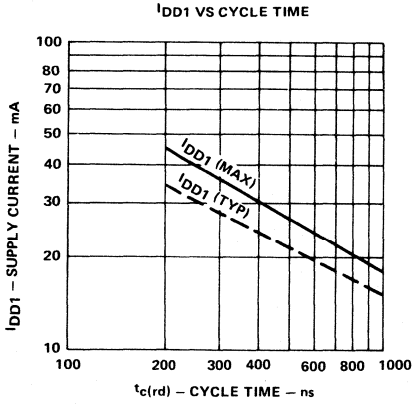
page mode read-modify-write timing

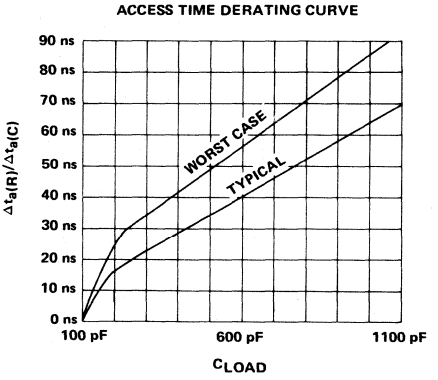


NOTE: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

RAS-only refresh timing







Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS4464
65,536-WORD BY 4-BIT DYNAMIC RAM

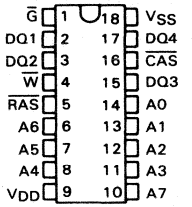
NOVEMBER 1983 — REVISED JANUARY 1984

- 65,536 X 4 Organization
- Single +5-V Supply (10% Tolerance)
- JEDEC Standardized Pin-Out
- Pin-Out Identical to TMS4416 (16K X 4 Dynamic RAM)
- Performance Ranges:

DEVICE	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
TMS4464-10	100 ns	60 ns	200 ns	270 ns
TMS4464-12	120 ns	70 ns	230 ns	310 ns
TMS4464-15	150 ns	85 ns	260 ns	345 ns
TMS4464-20	200 ns	120 ns	330 ns	435 ns

- Long Refresh Period . . . 4 ms (MAX)
- Low Refresh Overhead Time . . . As Low As 1.3% of Total Refresh Period
- On-Chip Substrate Bias Generator
- All Inputs, Outputs, and Clocks Fully TTL Compatible
- 3-State Unlatched Output
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Power Dissipation As Low As:
  - Operating . . . 250 mW (TYP)
  - Standby . . . 12.5 mW (TYP)
- $\overline{RAS}$-Only Refresh Mode
- Hidden Refresh Mode
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Mode (Optional)

TMS4464 . . . JL OR NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data-In/Data-Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4464 is a high-speed, 262,144-bit dynamic random-access memory, organized as 65,536 words of four bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

This device features maximum $\overline{RAS}$ access times of 100 ns, 120 ns, 150 ns, or 200 ns. Typical power dissipation as low as 250 mW operating and 12.5 mW standby.

New SMOS technology permits operation from a single +5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks are 150 mA typical, and a −1-V input voltage undershoot can be tolerated, minimizing system noise considerations.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address and data-in lines are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility.

The TMS4464 is offered in an 18-pin dual-in-line ceramic or plastic package and is guaranteed for operation from 0°C to 70°C. These packages are designed for insertion in mounting-hole rows on 300-mil (7,62 mm) centers.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on Pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (DQ1-DQ4)

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data-out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(G)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state they will remain in the low impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every four milliseconds to retain data. This can be achieved by strobing each of the 256 rows (A0-A7). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified pre-charge period, similar to a "$\overline{RAS}$-only" refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh (optional)

The optional $\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CLRL}) and holding it low after $\overline{RAS}$ falls (see parameter t_{RLCHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. For devices with this option, the external address is also ignored during the hidden refresh cycles.

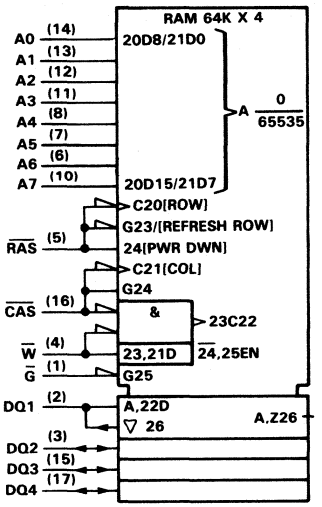
page-mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing random column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. The maximum number of columns that can be addressed is determined by $t_{w(RL)}$, the maximum $\overline{RAS}$ low pulse width. For example, with a minimum cycle time ($t_{c(P)}$ = 110 ns) approximately 90 of the 256 columns can be accessed.

power-up

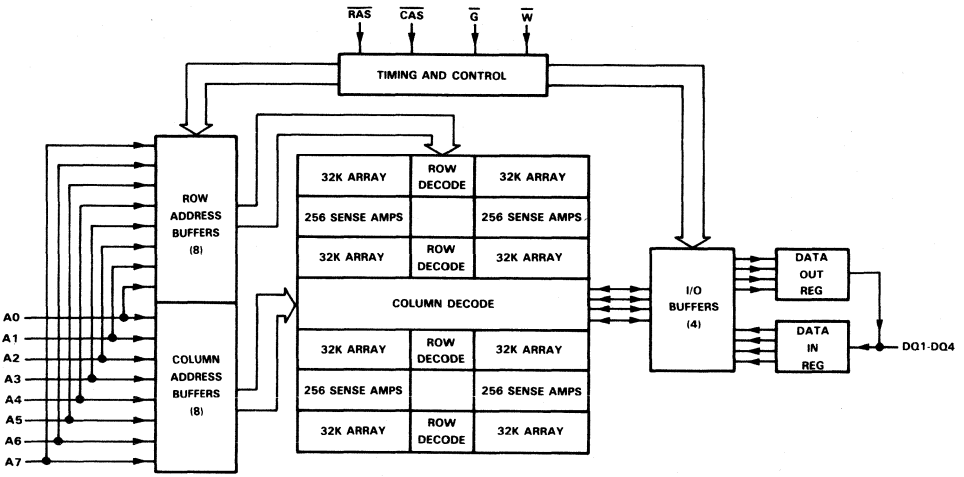
To achieve proper device operation, an initial pause of 200 μs is required after power-up followed by a minimum of eight initialization cycles.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage on any pin including V_{DD} supply (see Note 1)	−1 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.4		$V_{DD}+0.3$	V
Low-level input voltage, V_{IL} (see Note 2)	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as maximum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4464-10			TMS4464-12			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=5 V, All other pins = 0 V to 5.8 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle		80	TBD		70	TBD	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2.5	5		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		65	TBD		55	TBD	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		55	TBD		45	TBD	mA

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS4464-15			TMS4464-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I=0 V to 5.8 V, V_{DD}=5 V All other pins = 0 V to 5.8 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle		60	TBD		50	TBD	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2.5	5		2.5	5	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		50	TBD		40	TBD	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		40	TBD		30	TBD	mA

† All typical values are at T_A = 25°C and nominal supply voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TMS4164		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	4	7	pF
$C_{i(RC)}$	Input capacitance strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
$C_{i/o}$	Output capacitance	8	10	pF

† All typical values are at T_A = 25 °C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4464-10		TMS4464-12		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		60		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		100		120	ns
$t_{a(G)}$‡	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GAC}		30		35	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	30	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GOFF}	0	30	0	30	ns

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS4464-15		TMS4464-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	$t_{RLCL} \geq$ MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		85		120	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		150		200	ns
$t_{a(G)}$‡	Access time after $\overline{G}$ low	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GAC}		45		55	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	30	0	35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{GOFF}	0	30	0	35	ns

‡ $t_{a(C)}$ and $t_{a(R)}$ must be satisfied to guarantee $t_{a(G)}$.

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS4464-10		TMS4464-12		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	110		130		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	180		210		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	200		230		ns
$t_{c(W)}$	Write cycle time	t_{WC}	200		230		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	270		310		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	40		50		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{CPN}	40		50		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	60	10,000	70	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	90		100		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	100	10,000	120	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	35		40		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	30		40		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	30		40		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	20		20		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	15		15		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	60		70		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	30		35		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	70		85		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	30		35		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		10		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	30		35		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	70		85		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	20		25		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	60		70		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	95		105		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	20		25		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	40	25	50	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	135		155		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	30		30		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

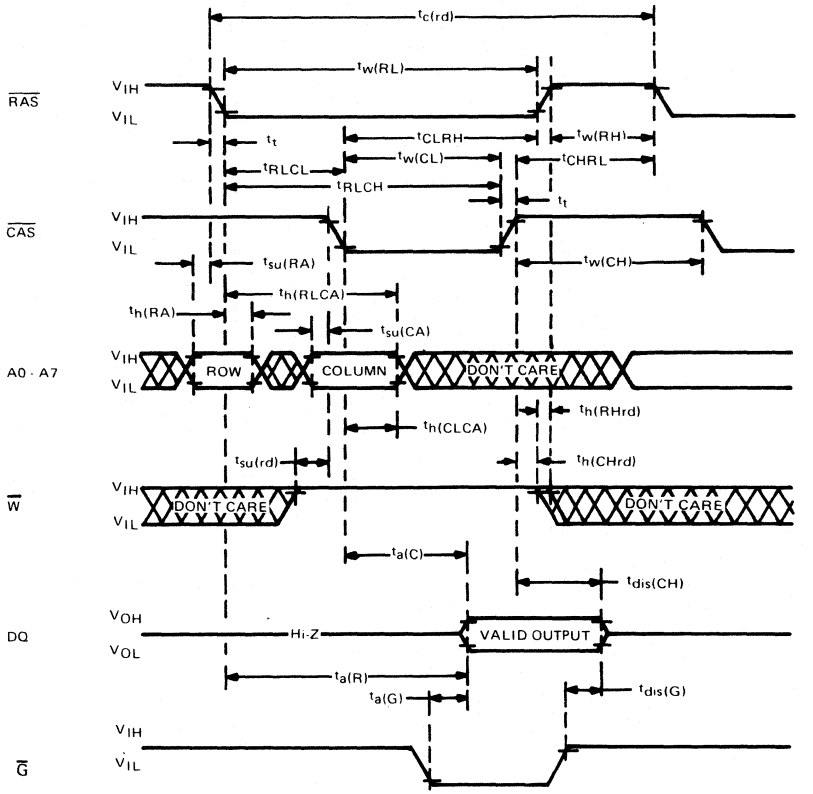
† All cycle times assume t_t = 5 ns.
‡ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
§ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).
¶ $\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.

timing requirements over recommended supply voltage range and operating free-air temperature range

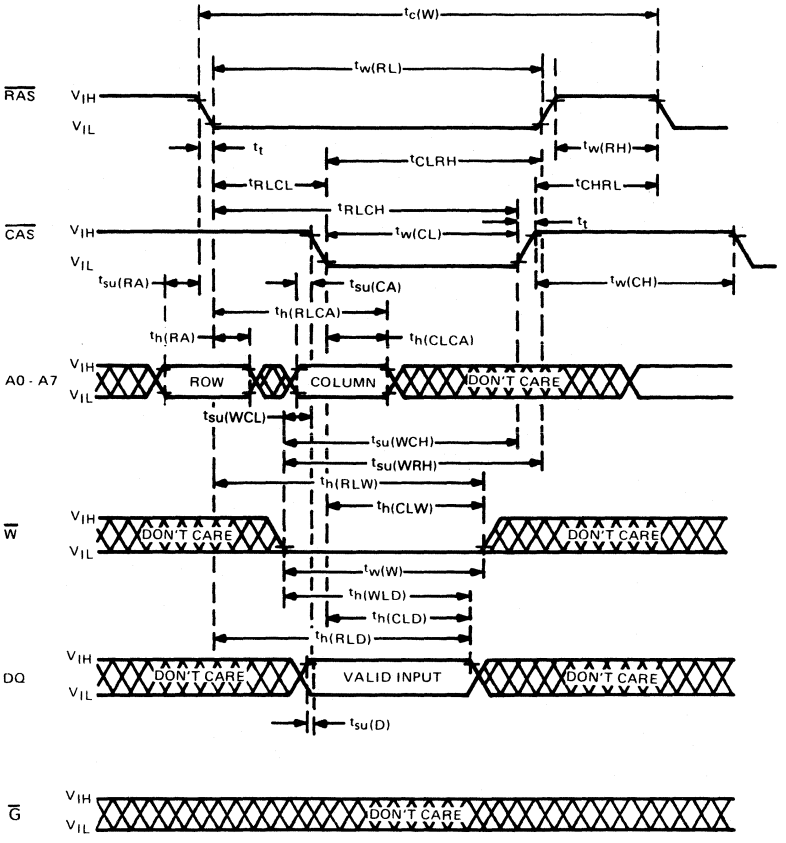
PARAMETER		ALT. SYMBOL	TMS4464-15		TMS4464-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	155		210		ns
$t_{c(PM)}$	Page-mode cycle time (read-modify-write cycle)	t_{PCM}	240		315		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	345		435		ns
$t_{w(CH)P}$	Pulse duration, $\overline{CAS}$ high (page mode)	t_{CP}	60		80		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (non-page mode)	t_{PCN}	60		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low‡	t_{CAS}	85	10,000	120	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low§	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	45		55		ns
t_t	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	50	3	50	ns
$t_{su(CA)}$	Column address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCL)}$	Early write command setup time before $\overline{CAS}$ low	t_{WCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	45		60		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	45		60		ns
$t_{h(CLCA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	25		45		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	15		20		ns
$t_{h(RLCA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	90		125		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	110		135		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		ns
$t_{h(CHrd)}$	Read command hold time after $\overline{CAS}$ high	t_{RCH}	0		0		ns
$t_{h(RHrd)}$	Read command hold time after $\overline{RAS}$ high	t_{RRH}	10		15		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	110		135		ns
t_{RLCHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high¶	t_{CHR}	30		35		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	85		120		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{CWD}	120		160		ns
t_{CLRL}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low¶	t_{CSR}	30		35		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	25	65	30	80	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write cycle only)#	t_{RWD}	185		240		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ	t_{GDD}	30		35		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

† All cycle times assume t_t = 5 ns.
‡ In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time ($t_{w(CL)}$).
§ In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time ($t_{w(RL)}$).
¶ $\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
# $\overline{G}$ must disable the output buffers prior to applying data to the device.

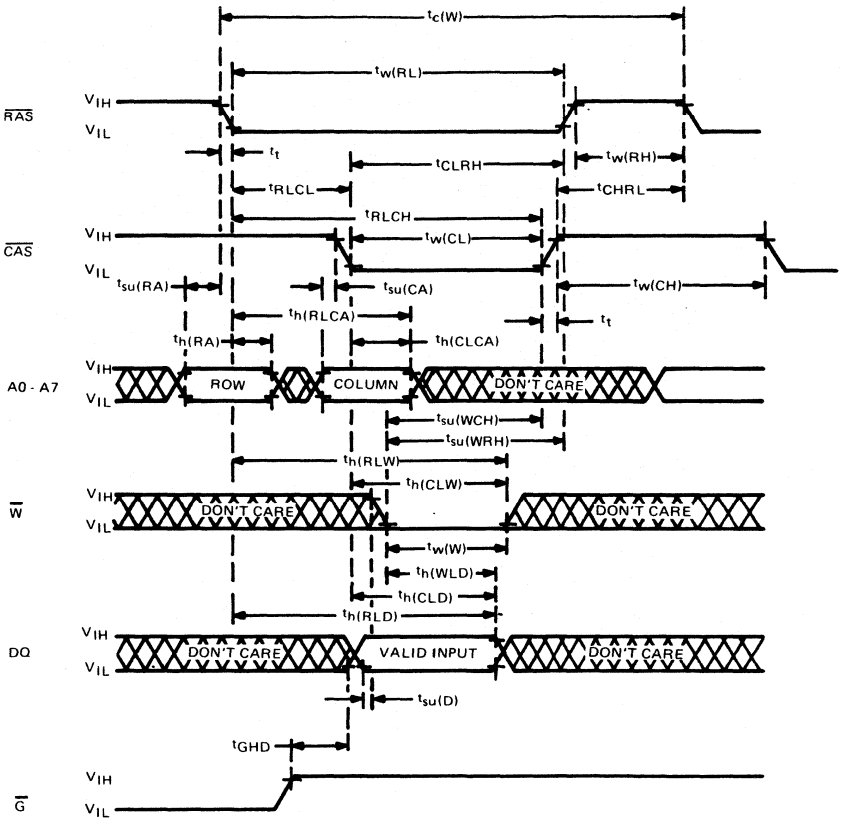
read cycle timing



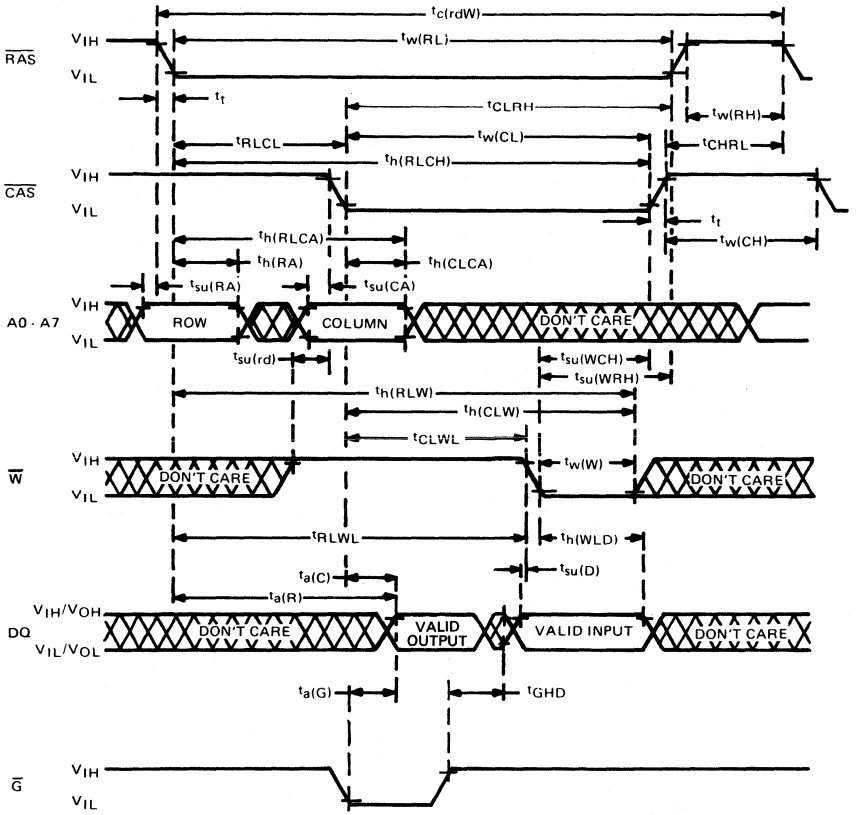
early write cycle timing



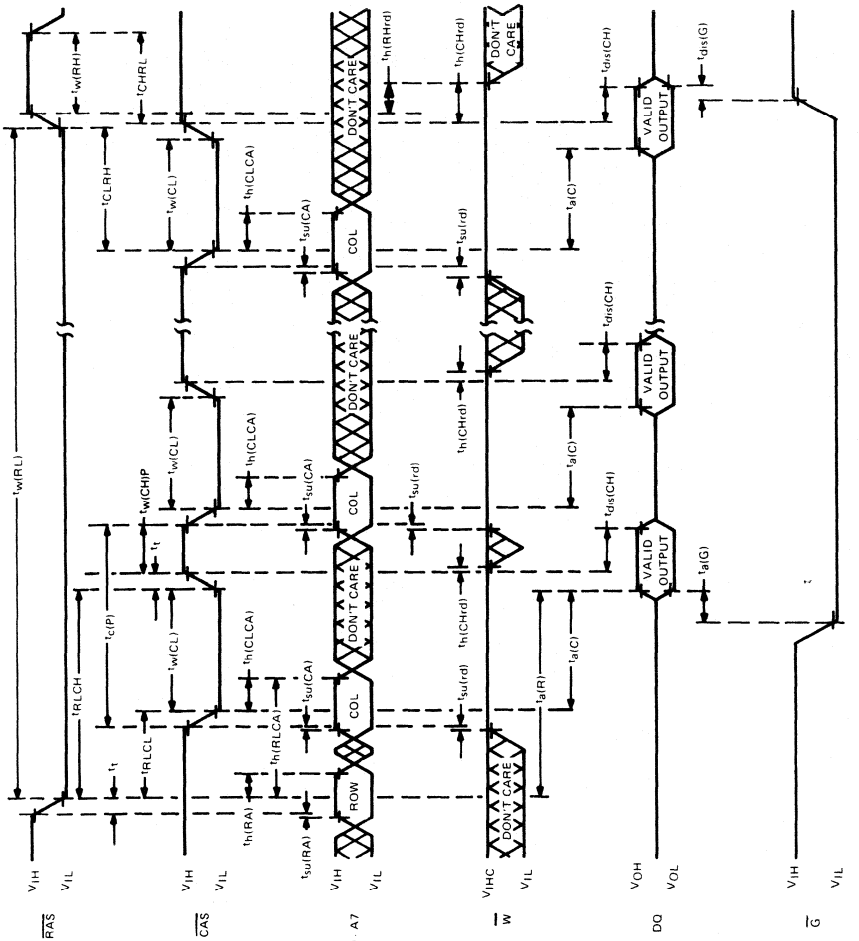
write cycle timing



read-write/read-modify-write cycle timing

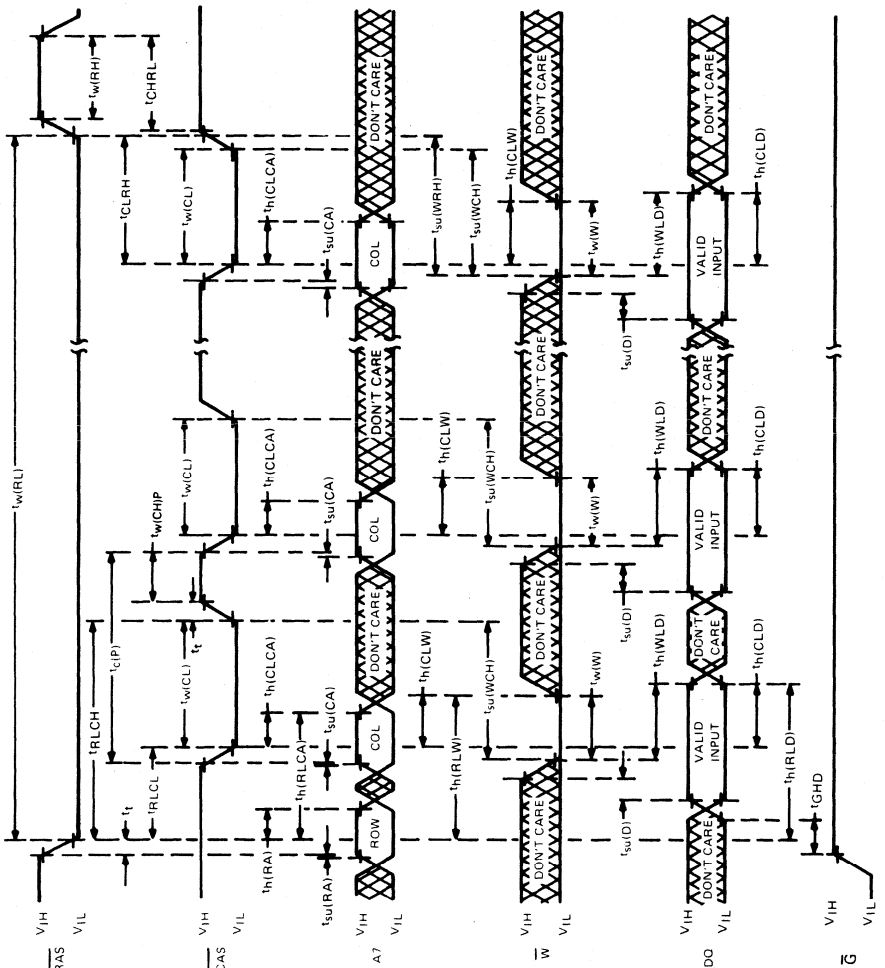


page-mode read cycle timing



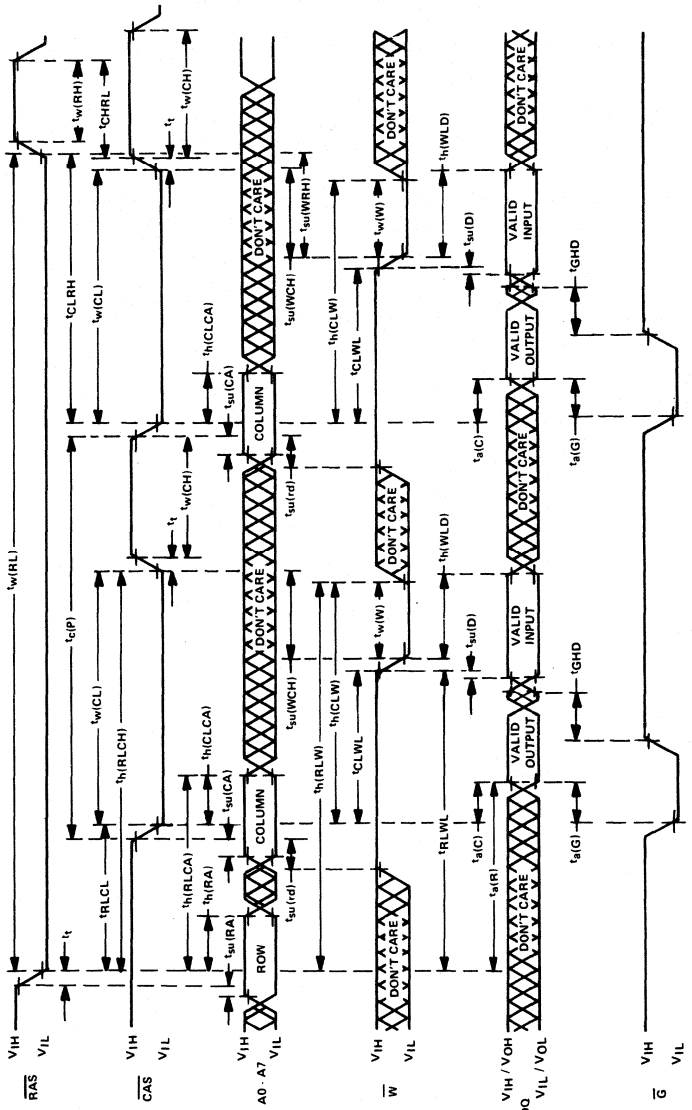
NOTE: A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read modify-write timing specifications are not violated.

page-mode write cycle timing



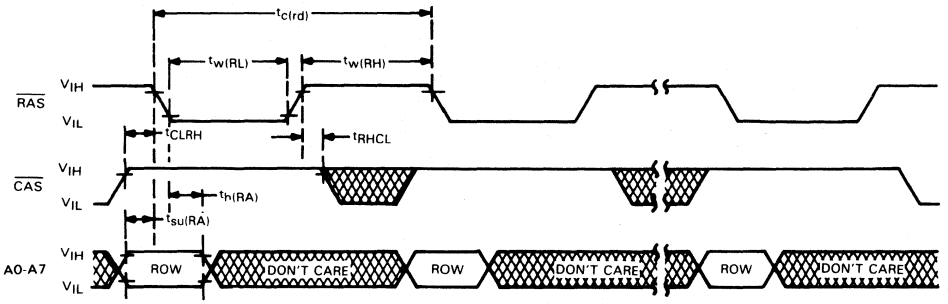
NOTE: A read cycle or a read-modify write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

page mode read-modify-write cycle timing

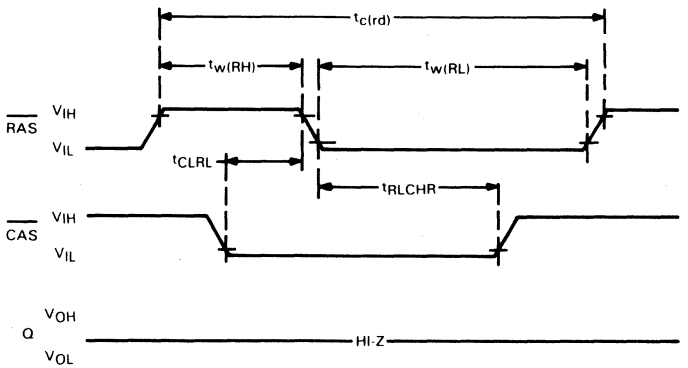


NOTE: A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

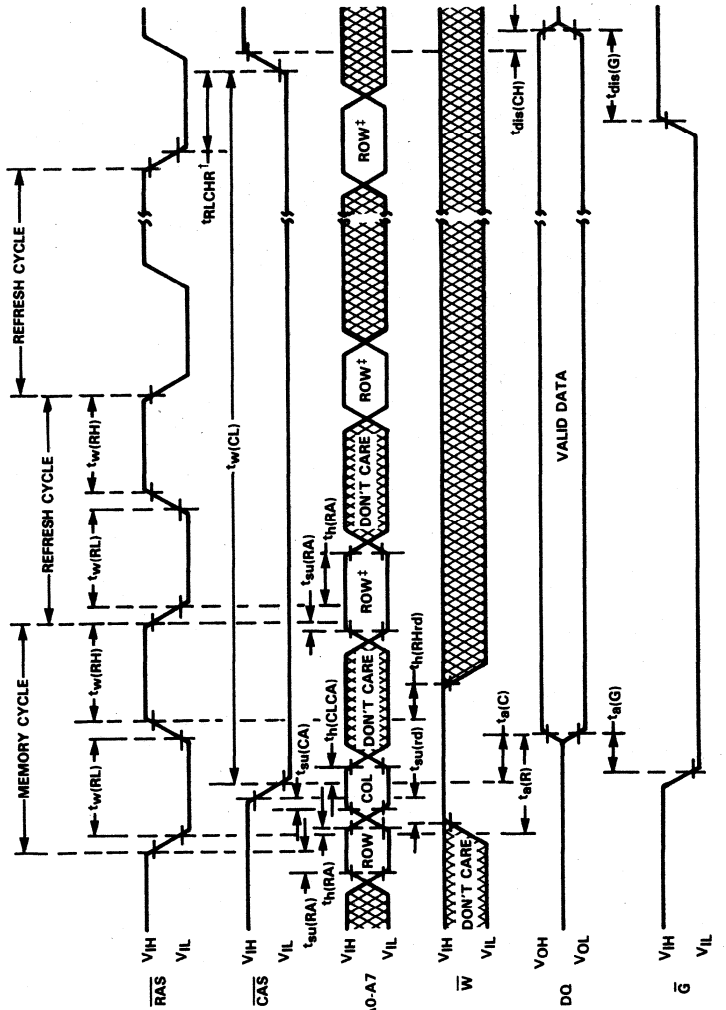
$\overline{RAS}$-only refresh cycle timing



automatic ($\overline{CAS}$ before $\overline{RAS}$) refresh cycle timing



hidden refresh cycle timing



† For devices with $\overline{CAS}$-before-$\overline{RAS}$ refresh option only.
‡ Row address is required only for devices without $\overline{CAS}$-before-$\overline{RAS}$ refresh option. Row address is "don't care" for devices with $\overline{CAS}$-before-$\overline{RAS}$ option.

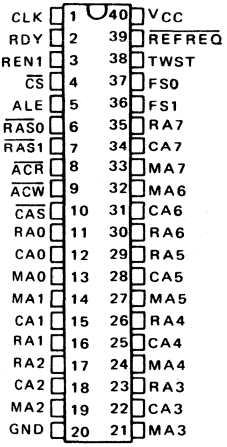
Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS4500A
DYNAMIC RAM CONTROLLER

JANUARY 1982 – REVISED APRIL 1983

- Controls Operation of 8K/16K/32K/64K Dynamic RAMs
- Creates Static RAM Appearance
- One Package Contains Address Multiplexer, Refresh Control, and Timing Control
- Directly Addresses and Drives Up to 256K Bytes of Memory Without External Drivers
- Operates from Microprocessor Clock
  - No Crystals, Delay Lines, or RC Networks
  - Eliminates Arbitration Delays
- Refresh May Be Internally or Externally Initiated
- Versatile
  - Strap-Selected Refresh Rate
  - Synchronous, Predictable Refresh
  - Selection of Distributed, Transparent, and Cycle-Steal Refresh Modes
  - Interfaces Easily to Popular Microprocessors
- Strap-Selected Wait State Generation for Microprocessor/Memory Speed Matching
- Ability to Synchronize or Interleave Controller with the Microprocessor System (Including Multiple Controllers)
- Three-State Outputs Allow Multiport Memory Configuration
- Performance Ranges of 150 ns/200 ns/250 ns

TMS4500A . . . NL PACKAGE
(TOP VIEW)



description

The TMS4500A is a monolithic DRAM system controller designed to provide address multiplexing, timing, control and refresh/access arbitration functions to simplify the interface of dynamic RAMs to microprocessor systems.

The controller contains a 16-bit multiplexer that generates the address lines for the memory device from the 16 system address bits and provides the strobe signals required by the memory to decode the address. An 8-bit refresh counter generates the 256-row addresses required for refresh.

A refresh timer is provided that generates the necessary timing to refresh the dynamic memories and assure data retention.

The TMS4500A also contains refresh/access arbitration circuitry to resolve conflicts between memory access requests and memory refresh cycles. The TMS4500A is offered in a 40-pin, 600-mil dual-in-line plastic package and is guaranteed for operation from 0°C to 70°C.

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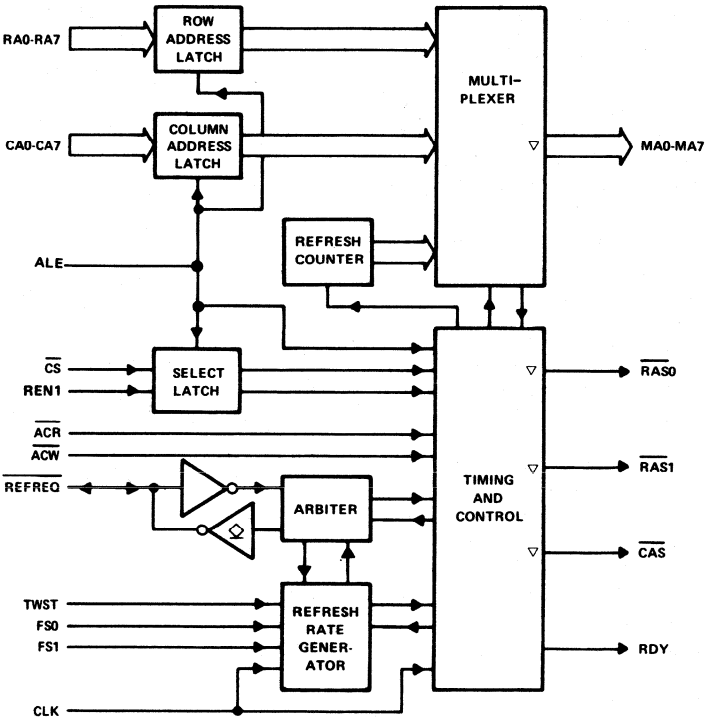
BLOCK DIAGRAM



pin descriptions

RA0 - RA7	Input	Row Address – These address inputs are used to generate the row address for the multiplexer.
CA0 - CA7	Input	Column Address – These address inputs are used to generate the column address for the multiplexer.
MA0 - MA7	Output	Memory Address – These three-state outputs are designed to drive the addresses of the dynamic RAM array.
ALE	Input	Address Latch Enable – This input is used to latch the 16 address inputs, $\overline{CS}$ and REN1. This also initiates an access cycle if chip select is valid. The rising edge (low level to high level) of ALE returns $\overline{RAS}$ to the high level.

pin descriptions (continued)

$\overline{CS}$	Input	Chip Select – A low on this input enables an access cycle. The trailing edge of ALE latches the chip select input.
REN1	INPUT	RAS Enable 1 – This input is used to select one of two banks of RAM via the $\overline{RAS0}$ and $\overline{RAS1}$ outputs when chip select is present. When it is low, $\overline{RAS0}$ is selected; when it is high, $\overline{RAS1}$ is selected.
$\overline{ACR}$, $\overline{ACW}$	Input	Access Control, Read; Access Control, Write – A low on either of these inputs causes the column address to appear on MA0 - MA7 and the column address strobe. The rising edge of $\overline{ACR}$ or $\overline{ACW}$ terminates the cycle by ending $\overline{RAS}$ and $\overline{CAS}$ strobes. When $\overline{ACR}$ and $\overline{ACW}$ are both low, MA0 - MA7, $\overline{RAS0}$, $\overline{RAS1}$, and $\overline{CAS}$ go into a high-impedance (floating) state.
CLK	Input	System Clock – This input provides the master timing to generate refresh cycle timings and refresh rate. Refresh rate is determined by the TWST, FS1, FS0 inputs.
$\overline{REFREQ}$	Input/Output	Refresh Request – (This input should be driven by an open-collector output.) On input, a low-going edge initiates a refresh cycle and will cause the internal refresh timer to be reset on the next falling edge of the CLK. As an output, a low-going edge signals an internal refresh request and that the refresh timer will be reset on the next low-going edge of CLK. $\overline{REFREQ}$ will remain low until the refresh cycle is in progress and the current refresh address is present on MA0-MA7. (Note: $\overline{REFREQ}$ contains an internal pull-up resistor with a nominal resistance of 10 kilohms.)
$\overline{RAS0}$, $\overline{RAS1}$	Output	Row Address Strobe – These three-state outputs are used to latch the row address into the bank of DRAMs selected by REN1. On refresh both signals are driven.
$\overline{CAS}$	Output	Column Address Strobe – This three-state output is used to latch the column address into the DRAM array.
RDY	Output	Ready – This totem-pole output synchronizes memories that are too slow to guarantee microprocessor access time requirements. This output is also used to inhibit access cycles during refresh when in cycle-steal mode.
TWST	Input	Timing/Wait Strap – A high on this input indicates a wait state should be added to each memory cycle. In addition it is used in conjunction with FS0 and FS1 to determine refresh rate and timing.
FS0, FS1	Inputs	Frequency Select 0; Frequency Select 1 – These are strap inputs to select Mode and Frequency of operation as shown in Table 1.

TABLE 1 – STRAP CONFIGURATION

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLK FREQ. (MHz)	REFRESH FREQ. (kHz)	CLOCK CYCLES FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L†	0	EXTERNAL	–	REFREQ	4
L	L	H	0	CLK ÷ 31	1.984	64 - 95‡	3
L	H	L	0	CLK ÷ 46	2.944	64 - 85‡	3
L	H	H	0	CLK ÷ 61	3.904	64 - 82§	4
H	L	L	1	CLK ÷ 46	2.944	64 - 85‡	3
H	L	H	1	CLK ÷ 61	3.904	64 - 80‡	4
H	H	L	1	CLK ÷ 76	4.864	64 - 77‡	4
H	H	H	1	CLK ÷ 91	5.824	64 - 88¶	4

† This strap configuration resets the Refresh Timer circuitry.

‡ Upper figure in refresh frequency is the frequency that is produced if the minimum CLK frequency of the next select state is used.

§ Refresh frequency if CLK frequency is 5 MHz.

¶ Refresh frequency if CLK frequency is 8 MHz.

functional description

TMS4500A consists of six basic blocks; address and select latches, refresh rate generator, refresh counter, the multiplexer, the arbiter, and the timing and control block.

address and select latches

The address and select latches allow the DRAM controller to be used in systems that multiplex address and data on the same lines without external latches. The row address latches are transparent, meaning that while ALE is high, the output at MA0 - MA7 follows the inputs RA0 - RA7.

refresh rate generator

The refresh rate generator is a counter that indicates to the arbiter that it is time for a refresh cycle. The counter divides the clock frequency according to the configuration straps as shown in Table 1. The counter is reset when a refresh cycle is requested or when TWST, FS1 and FS0 are low. The configuration straps allow the matching of memories to the system access time.

Upon Power-Up it is necessary to provide a reset signal by driving all three straps to the controller low to initialize internal counters. A system's low-active, power-on reset ($\overline{\text{RESET}}$) can be used to accomplish this by connecting it to those straps that are desired high during operation. During this reset period, at least four clock cycles should occur.

refresh counter

The refresh counter contains the address of the row to be refreshed. The counter is decremented after each refresh cycle. [A low-to-high transition on TWST sets the refresh counter to FF_{16} (255_{10}).]

multiplexer

The multiplexer provides the DRAM array with row, column, and refresh addresses at the proper times. Its inputs are the address latches and the refresh counter. The outputs provide up to 16 multiplexed addresses on eight lines.

arbiter

The arbiter provides two operational cycles: access and refresh. The arbiter resolves conflicts between cycle requests and cycles in execution, and schedules the inhibited cycle when used in cycle-steal mode.

timing and control block

The timing and control block executes the operational cycle at the request of the arbiter. It provides the DRAM array with $\overline{RAS}$ and $\overline{CAS}$ signals. It provides the CPU with a RDY signal. It controls the multiplexer during all cycles. It resets the refresh rate generator and decrements the refresh counter during refresh cycles.

absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 V to 7 V
Input voltage range (any input) (see Note 1) . . . . . −1.5 V to 7 V
Continuous power dissipation . . . . . 1.2 W
Operating ambient temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2.4		6	V
Low-level input voltage, V_{IL}	−1‡		0.8	V
Operating ambient† temperature, T_A	0		70	°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels only.
NOTE 1: Voltage values are with respect to the ground terminal.

electrical characteristics over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	MA0-MA7, RDY	I_{OH} = −1 mA	V_{CC} = 4.5 V	2.4			V
		$\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS}$			2.7			
		$\overline{REFREQ}$	I_{OH} = 100 μA	V_{CC} = 4.5 V	2.4			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA	V_{CC} = 4.5 V			0.4	V
I_{IH}	High-level input current	$\overline{REFREQ}$	V_I = 5.5 V				100	μA
		All others					10	
I_{IL}	Low-level input current	$\overline{REFREQ}$	V_I = 0 V				−1.25	mA
		All others					−10	μA
I_{OZ}	Off-state output current		V_O = 0 to 4.5 V	V_{CC} = 5.5 V			±50	μA
I_{CC}	Operating supply current		T_A = 0°C			100	140	mA
C_i	Input capacitance		V_I = 0 V,	f = 1 MHz		5		pF
C_o	Output capacitance		V_O = 0 V,	f = 1 MHz		6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C except where otherwise noted.

timing requirements over recommended supply voltage range and operating ambient temperature range

PARAMETER		TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(C)}$	CLK cycle time	100		100		140		ns
$t_{w(CH)}$	CLK high pulse width	20		20		20		
$t_{w(CL)}$	CLK low pulse width	35		35		35		
t_t	Transition time, all inputs		50		50		50	
t_{AEL-CL}	Time delay, ALE low to CLK starting low (see Note 1)	10		10		15		
t_{CL-AEL}	Time delay, CLK low to ALE starting low (see Note 1)	10		10		15		
t_{CL-AEH}	Time delay, CLK low to ALE starting high (see Note 2)	15		20		20		
$t_{w(AEH)}$	Pulse width ALE high	50		60		60		
t_{AV-AEL}	Time delay, address, REN1, $\overline{CS}$ valid to ALE low	5		10		15		
t_{AEL-AX}	Time delay, ALE low to address not valid	10		10		10		
$t_{AEL-ACL}$	Time delay, ALE low to $\overline{ACX}$ low (see Notes 3,4,5, and 6)	$t_{h(RA)}+30$		$t_{h(RA)}+40$		$t_{h(RA)}+50$		
t_{ACH-CL}	Time delay, $\overline{ACX}$ high to CLK low (see Notes 3 and 7)	20		20		20		
t_{ACL-CH}	Time delay, $\overline{ACX}$ low to CLK starting high (to remove RDY)	30		30		30		
t_{RQL-CL}	Time delay, $\overline{REFREQ}$ low to CLK starting low (see Note 8)	20		20		20		
$t_{w(RQL)}$	Pulse width, $\overline{REFREQ}$ low	20		20		20		

NOTES:
1. Coincidence of the trailing edge of CLK and the trailing edge of ALE should be avoided, as the refresh/access occurs on the trailing CLK edge. A trailing edge of CLK should occur during the interval from $\overline{ACX}$ high to ALE low.
2. If ALE rises before $\overline{ACX}$ and a refresh request is present, the falling edge of CLK after t_{CL-AEH} will output the refresh address to MA0-MA7 and initiate a refresh cycle.
3. These specifications relate to system timing and do not directly reflect device performance
4. On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low.
5. For maximum speed access (internal delays on both access and access grant cycles), $\overline{ACX}$ should occur prior to or coincident with ALE.
6. $t_{h(RA)}$ is the dynamic memory row address hold time. $\overline{ACX}$ should follow ALE by $t_{AEL-CEL}$ in systems where the required $t_{h(RA)}$ is greater than $t_{REL-MAX}$ minimum.
7. Minimum of 20 ns is specified to ensure arbitration will occur on falling CLK edge. t_{ACH-CL} also affects precharge time such that the minimum t_{ACH-CL} should be equal or greater than: $t_{w(RH)} - t_{w(CL)} + 30$ ns (for cycle where $\overline{ACX}$ high occurs prior to ALE high) where $t_{w(RH)}$ is the DRAM $\overline{RAS}$ precharge time.
8. This parameter is necessary only if refresh arbitration is to occur on this low-going CLK edge (in systems where refresh is synchronized to external events).

switching characteristics over recommended supply voltage range and operating ambient temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS	TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{AEL-REL}$	Time delay, ALE low to $\overline{RAS}$ starting low	C_L = 160 pF		30		40		50	ns
$t_{t(REL)}$	$\overline{RAS}$ fall time			15		20		25	
$t_{RAV-MAV}$	Time delay, row address valid to memory address valid			40		50		60	
$t_{AEH-MAV}$	Time delay, ALE high to valid memory address			55		70		90	
$t_{AEL-RYL}$	Time delay, ALE to RDY starting low (TWST = 1 or refresh in progress)	C_L = 40 pF		20		25		35	
$t_{AEL-CEL}$	Time delay, ALE low to $\overline{CAS}$ starting low	C_L = 160 pF	60	150	75	200	100	250	
$t_{AEH-REH}$	Time delay, ALE high to $\overline{RAS}$ starting high			25		30		40	
$t_{t(MAV)}$	Address transition time			15		20		25	
$t_{ACL-MAX}$	Row address hold from $\overline{ACX}$ low		15		20		25		
$t_{MAV-CEL}$	Time delay, memory address valid to $\overline{CAS}$ starting low		0		0		0		
$t_{t(CEL)}$	$\overline{CAS}$ fall time	C_L = 320 pF		15		20		25	
$t_{ACL-CEL}$	Time delay, $\overline{ACX}$ low to $\overline{CAS}$ starting low	C_L = 160 pF	50	90	65	130	85	165	
$t_{ACH-REH}$	Time delay, $\overline{ACX}$ to $\overline{RAS}$ starting high			30		40		50	
$t_{t(REH)}$	$\overline{RAS}$ rise time			15		20		25	
$t_{ACH-CEH}$	Time delay, $\overline{ACX}$ high to $\overline{CAS}$ starting high		5	30	10	40	15	50	
$t_{t(CEH)}$	$\overline{CAS}$ rise time	C_L = 320 pF		30		35		45	
$t_{ACH-MAX}$	Column address hold from $\overline{ACX}$ high	C_L = 160 pF	15		20		25		
t_{CH-RYH}	Time delay, CLK high to RDY starting high (after $\overline{ACX}$ low) (see Note 9)	C_L = 40 pF		35		45		60	
$t_{RFL-RFL}$	Time delay, $\overline{REFREQ}$ external till supported by $\overline{REFREQ}$ internal	C_L = 40 pF		25		30		30	
t_{CH-RFL}	Time delay, CLK high till $\overline{REFREQ}$ internal starting low			30		35		45	
t_{CL-MAV}	Time delay, CLK low till refresh address valid	C_L = 160 pF		75		100		125	
t_{CH-RRL}	Time delay, CLK high till refresh $\overline{RAS}$ starting low		10	50	15	60	20	80	
$t_{MAV-RRL}$	Time delay, refresh address valid till refresh $\overline{RAS}$ low		5		5		5		
t_{CL-RFH}	Time delay, CLK low to $\overline{REFREQ}$ starting high (3 cycle refresh)			45		55		75	
t_{CH-RFH}	Time delay, CLK high to $\overline{REFREQ}$ starting high (4 cycle refresh)			45		55		75	
t_{CH-RRH}	Time delay, CLK high to refresh $\overline{RAS}$ starting high		5	35	10	45	10	60	
t_{CH-MAX}	Time delay, refresh address hold after CLK high		15		20		25		

NOTE 9: RDY returns high on the rising edge of CLK. If TWST = 0, then on an access grant cycle RDY goes high on the same edge that causes access $\overline{RAS}$ low. If TWST = 1, then RDY goes to the high level on the first rising CLK edge after $\overline{ACX}$ goes low on access cycles and on the next rising edge after the edge that causes access $\overline{RAS}$ low on access grant cycles (assuming $\overline{ACX}$ low).

switching characteristics over recommended supply voltage range and operating ambient temperature range (see Figure 1) (continued)

PARAMETER		TEST CONDITIONS	TMS4500A-15		TMS4500A-20		TMS4500A-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{CH-REL}	Time delay, CLK high till access $\overline{RAS}$ starting low	C_L = 160 pF		60		70		95	ns
t_{CL-CEL}	Time delay, CLK low to access $\overline{CAS}$ starting low (see Note 4)			125		140		185	
t_{CL-MAX}	Row address hold after CLK low		25		30		40		
$t_{w(ACL)}$	$\overline{ACX}$ low width		25		30		40		
$t_{REL-MAX}$	Row address hold from $\overline{RAS}$ low		25		30		35		
$t_{t(RYL)}$	RDY fall time	C_L = 40 pF		10		15		20	
$t_{t(RYH)}$	RDY rise time			20		25		35	
t_{dis}	Output disable time (3-state outputs)	C_L = 160 pF	45	100	55	125	75	165	
$t_{AEH-MAX}$	Column address hold from ALE high		10		15		20		
t_{en}	Output enable time (3-state outputs)		0	65	0	80	0	105	
$t_{CAV-CEL}$	Column address setup to $\overline{CAS}$ after refresh		0		0		0		
t_{CH-CEL}	Time delay, CLK high to access $\overline{CAS}$ starting low (see Note 4)			140		180		235	
t_{ACL-CL}	$\overline{ACX}$ low to CLK starting low	C_L = 40 pF	25		35		45		
$t_{ACL-RYH}$	$\overline{ACX}$ low to RDY starting high	C_L = 40 pF		40		50		60	
t_{CL-ACL}	CLK low to $\overline{ACX}$ starting low	C_L = 40 pF	0		0		0		

NOTE 4: On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ is timed from the CLK high transition that causes $\overline{RAS}$ low. If $\overline{ACX}$ occurs 20 ns or more after ALE then $\overline{CAS}$ is timed from the CLK low transition following the CLK high transition causing $\overline{RAS}$ low.

PARAMETER MEASUREMENT INFORMATION

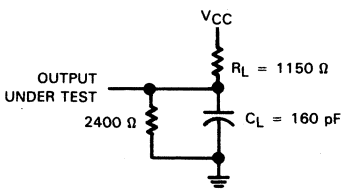
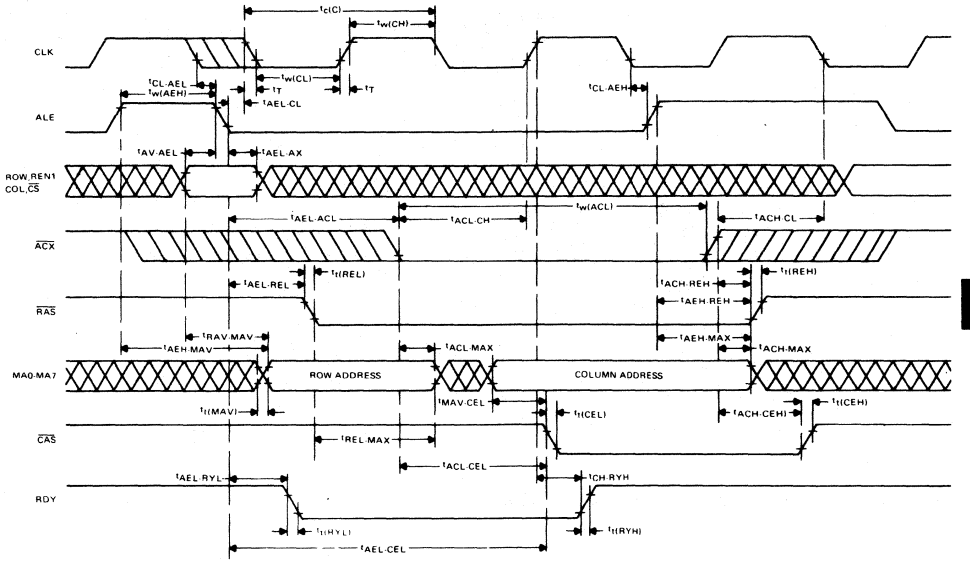
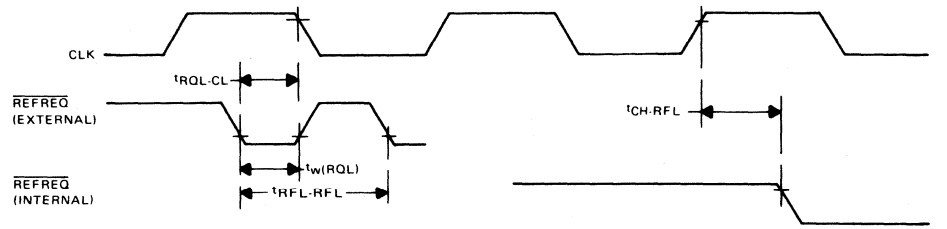


FIGURE 1 – LOAD CIRCUIT

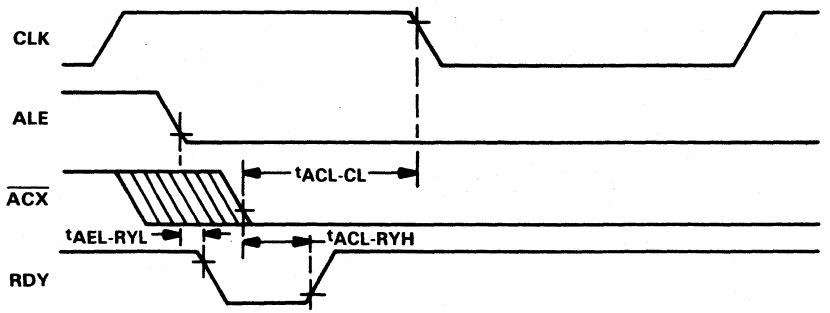
access cycle timing



refresh request timing



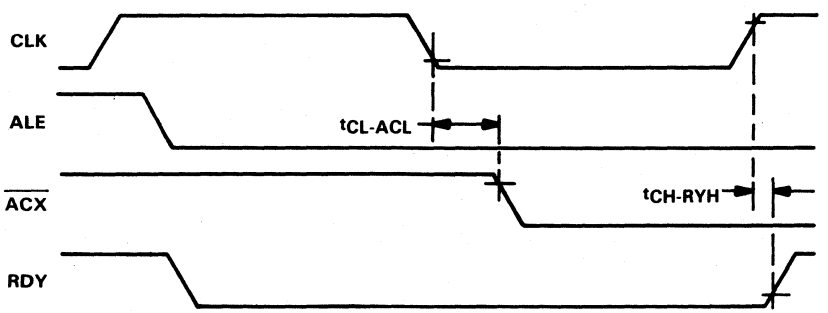
ready timing ($\overline{ACX}$ during CLK high) (see notes 10 thru 13)



RDY starting high is timed from $\overline{ACX}$ low ($t_{ACL-RYH}$) for the condition $\overline{ACX}$ going low while CLK high.

NOTES: 10. For RDY high transition (during normal access) to be timed from the rising edge of CLK, $\overline{ACX}$ must occur t_{CL-ACL} after the falling edge of CLK.
11. For $\overline{ACX}$ prior to the falling edge of CLK by t_{ACL-CL}, the RDY high transition will be $t_{ACL-RYH}$.
12. t_{ACL-CL} is a limiting parameter for control of RDY to be dependent upon $\overline{ACX}$ low.
13. During the interval for t_{ACL-CL} < MINIMUM to t_{CL-ACL} > MINIMUM, the control of RDY may vary between the rising clock edge or falling edge of $\overline{ACX}$.

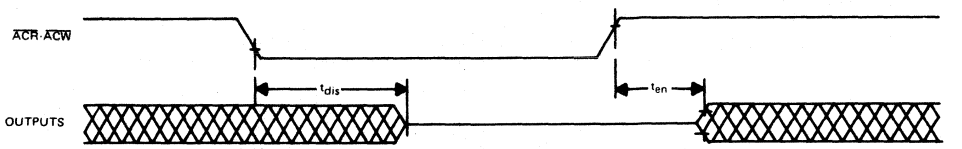
ready timing ($\overline{ACX}$ during CLK low) (see notes 10 thru 13)



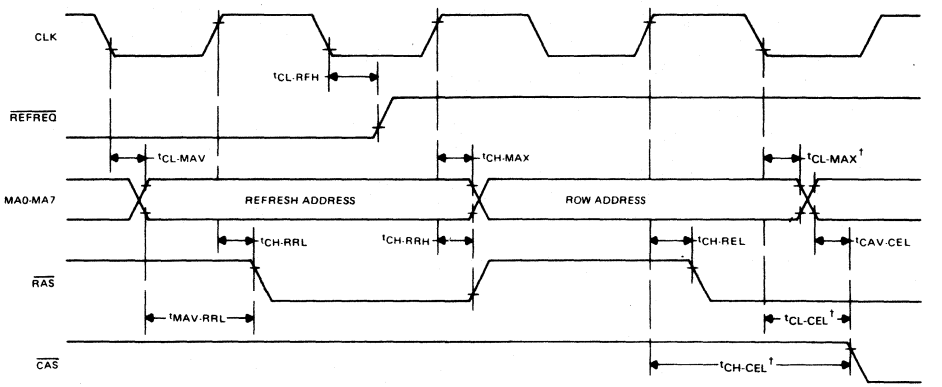
RDY starting high is timed from CLK high (t_{CH-RYH}) for the condition $\overline{ACX}$ going low while CLK low.

NOTES: 10. For RDY high transition (during normal access) to be timed from the rising edge of CLK, $\overline{ACX}$ must occur t_{CL-ACL} after the falling edge of CLK.
11. For $\overline{ACX}$ prior to the falling edge of CLK by t_{ACL-CL}, the RDY high transition will be $t_{ACL-RYH}$.
12. t_{ACL-CL} is a limiting parameter for control of RDY to be dependent upon $\overline{ACX}$ low.
13. During the interval for t_{ACL-CL} < MINIMUM to t_{CL-ACL} > MINIMUM, the control of RDY may vary between the rising clock edge or falling edge of $\overline{ACX}$.

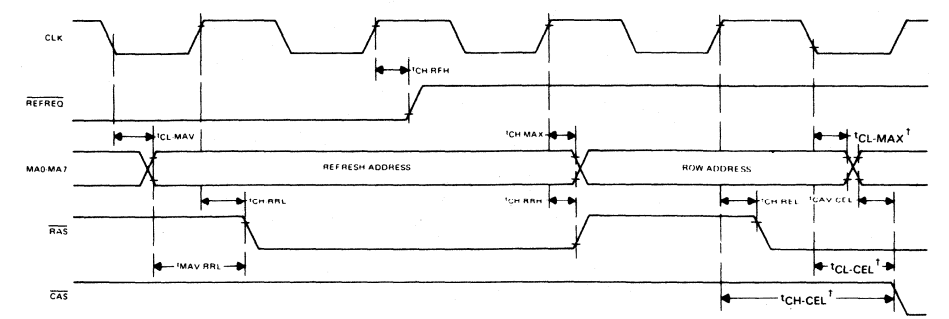
output tristate timing



refresh cycle timing (three cycle)

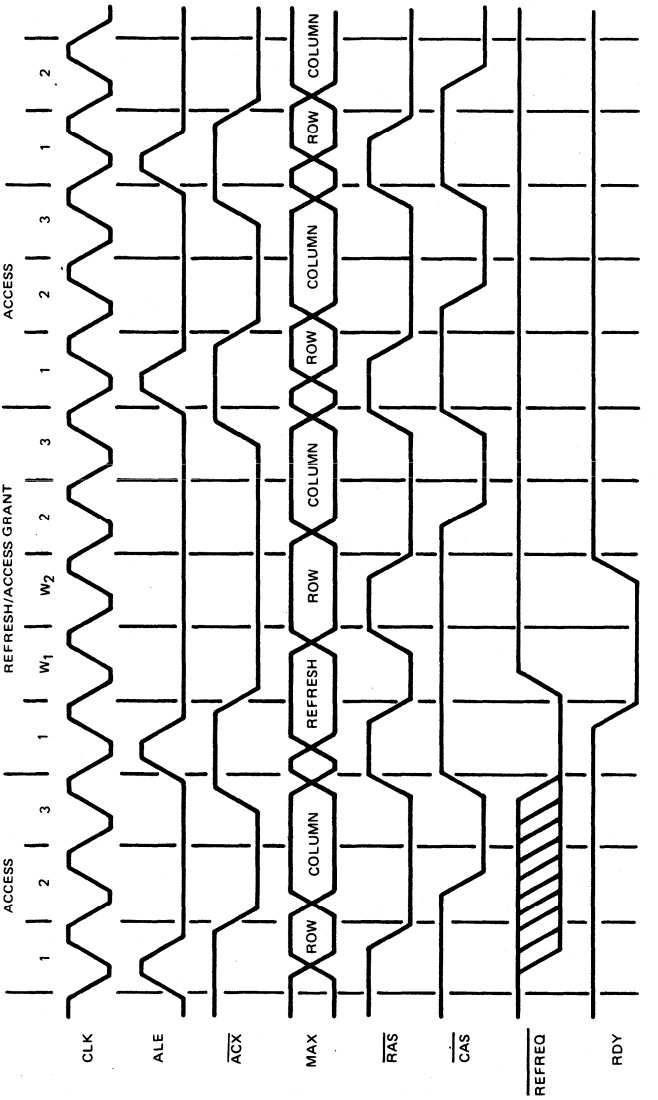


refresh cycle timing (four cycle)

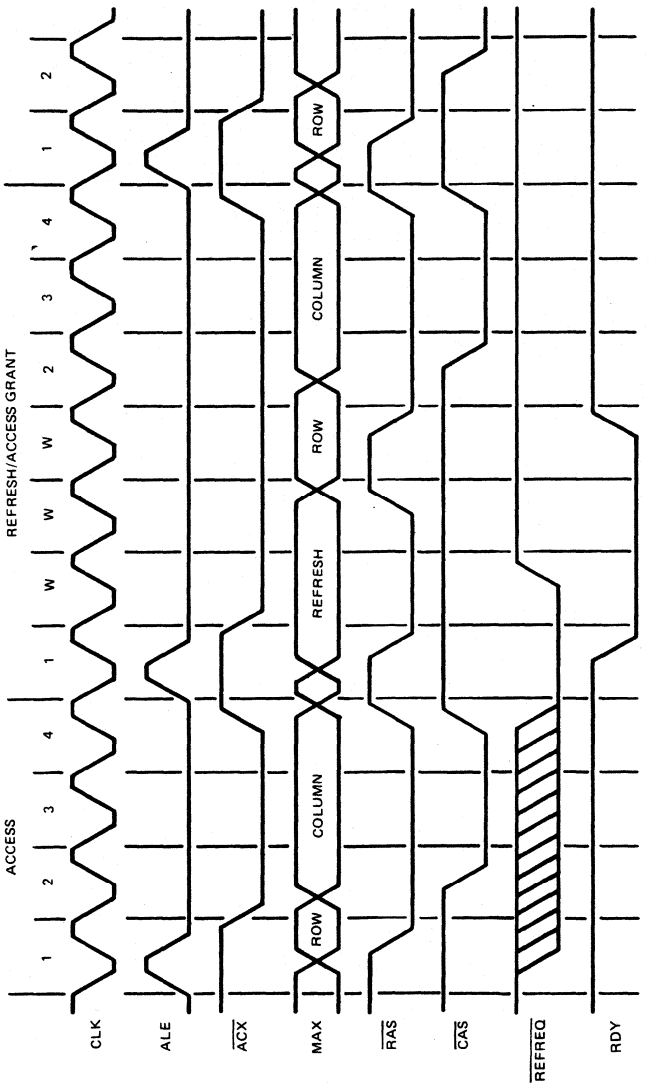


† On the access grant cycle following refresh, the occurrence of $\overline{CAS}$ low depends on the relative occurrence of ALE low to $\overline{ACX}$ low. If $\overline{ACX}$ occurs prior to or coincident with ALE then $\overline{CAS}$ and address multiplexing are timed from the CLK high transition with $t_{REL\text{-}MAX}$ delay from $\overline{RAS}$ low to address not valid. If $\overline{ACX}$ occurs 20 ns or more after ALE, then $\overline{CAS}$ and address multiplexing are timed from the CLK low transition.

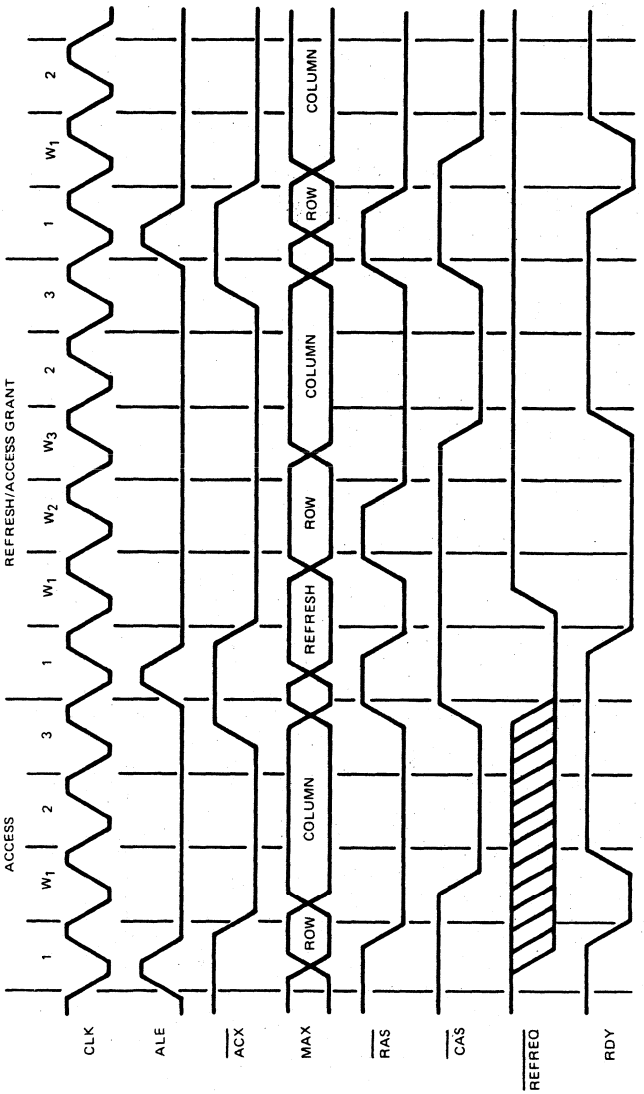
typical access/refresh/access cycle
(three cycle, TWST = 0)



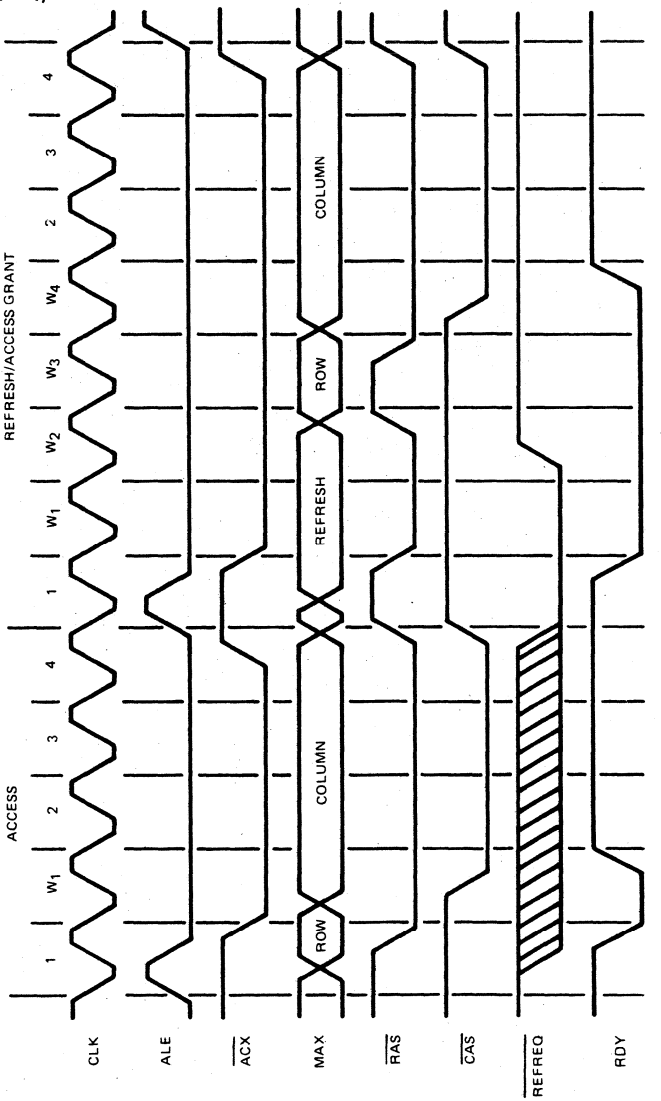
typical access/refresh/access cycle
(four cycle, TWST = 0)



typical access/refresh/access cycle
(three cycle, TWST = 1)



typical access/refresh/access cycle
(four cycle, TWST = 1)



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is available from Texas Instruments in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

Please contact

Texas Instruments
P.O. Box 401560
Dallas, Texas 75240

to obtain this brochure.

TM4416ET16, TM4416EJ16
16,384 BY 16-BIT DYNAMIC RAM MODULE

NOVEMBER 1983 - REVISED APRIL 1984

- 16,384 X 16 Organization
- Single +5 V Supply (10% Tolerance)
- 30-Pin Single-In-Line Package (SIP)
- Utilizes Four 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period ... 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

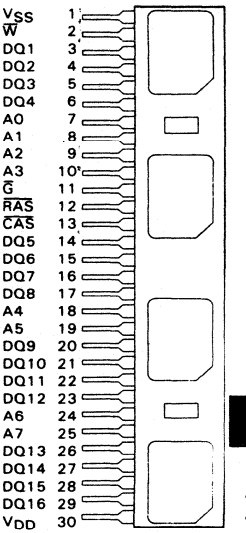
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS4416-15	150 ns	80 ns	260 ns	360 ns
TMS4416-20	200 ns	120 ns	330 ns	460 ns

- Common CAS Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4416E 16-15	800 mW	70 mW
TM4416E 16-20	700 mW	70 mW

- Operating Free-Air Temperature ... 0 °C to 70 °C

30-PIN
SINGLE-IN-LINE PACKAGE
(TOP VIEW)



This drawing shown for pin assignments only. Chip carrier orientation, number of capacitors and location vary with package used (see Mechanical Data).

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ16	Data In/Data Out
$\overline{G}$	Output Enable
NC	No Connection
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4416E 16 is a 256K, dynamic random-access memory module organized as 16,384 × 16 bits in a 30-pin single-in-line package comprising four TMS4416FPL, 16,384 × 4 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate. Two 0.1 uF decoupling capacitors are mounted on bottom of the substrate for TM4416EJ16 and two 0.1 uF decoupling capacitors are mounted on top of the substrate for TM4416ET16. Each TMS4416FPL is described in the TMS4416 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as ammended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed. The TM4416E 16 series is rated for operation from 0 °C to 70 °C.

operation

The TM4416E 16 operates as four TMS4416s connected as shown in the functional block diagram. Refer to the TMS4416 data sheet for details of its operation.

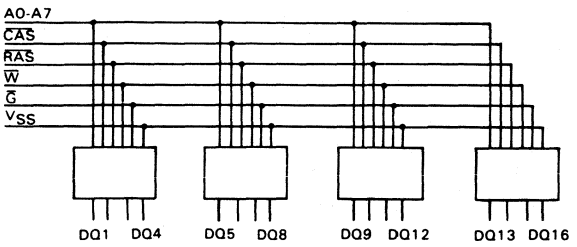
specifications

For TMS4416 electrical specifications, refer to the TMS4416 data sheet.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) MIN thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin over nickel plate

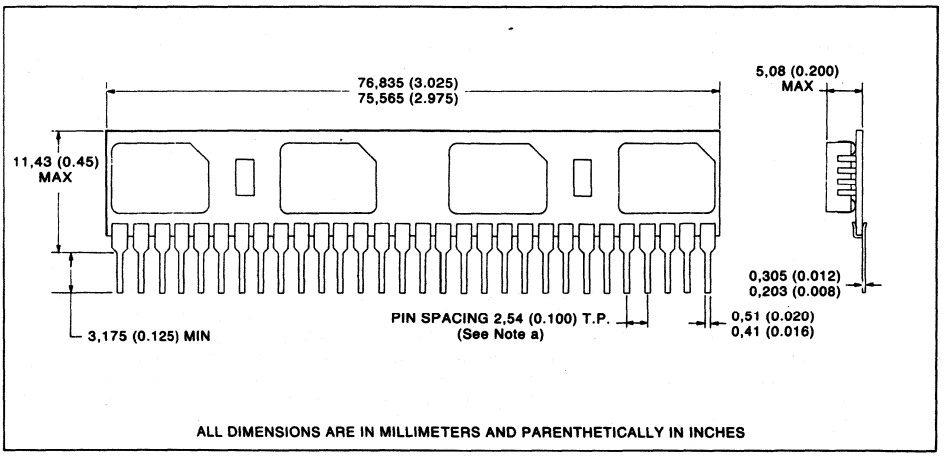
block diagram



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Write Enable Input
V_{DD}	+ 5V Supply
V_{SS}	Ground
DQ1-DQ16	Data in/Data out
G	Output Enable

MECHANICAL DATA

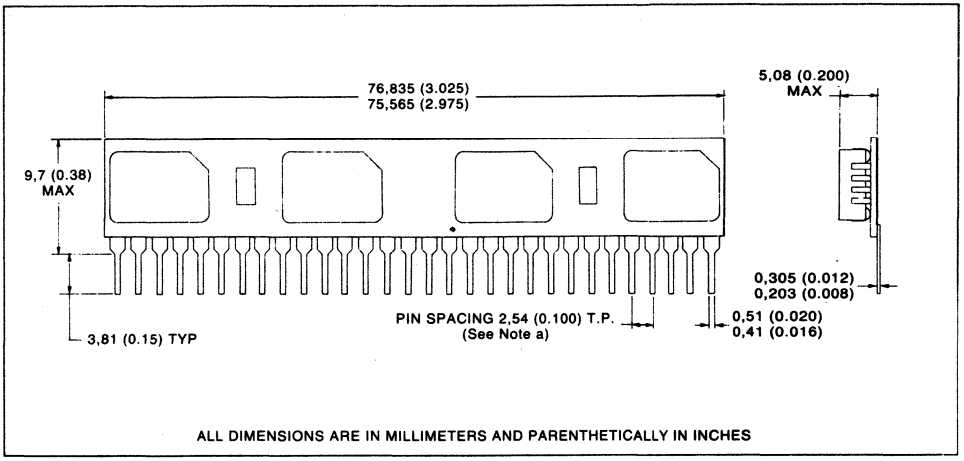
30 - Pin single-in-line packages
TM4416ET16



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

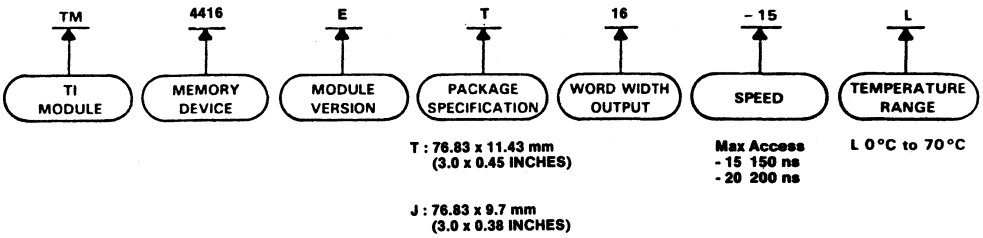
Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TM4416EJ16



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TI single-in-line package nomenclature



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TM4416EE8, TM4416EF8
32,768 BY 8-BIT DYNAMIC RAM MODULE

NOVEMBER 1983 - REVISED APRIL 1984

- 32,768 X 8 Organization
- Single +5 V Supply (10% Tolerance)
- 24-Pin Single-In-Line Package (SIP)
- Utilizes Four 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period ... 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

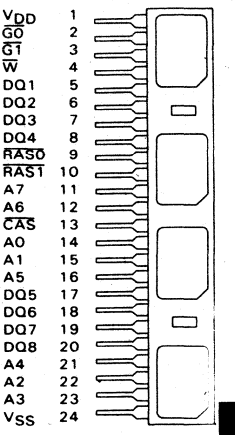
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS4416-15	150 ns	80 ns	260 ns	360 ns
TMS4416-20	200 ns	120 ns	330 ns	460 ns

- Common CAS Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4416E8-15	800 mW	70 mW
TM4416E8-20	700 mW	70 mW

- Operating Free-Air Temperature ... 0 °C to 70 °C

24-PIN
SINGLE-IN-LINE PACKAGE
(TOP VIEW)



This drawing shown for pin assignments only. Chip carrier orientation, number of capacitors and location vary with package used (see Mechanical Data).

PIN NOMENCLATURE	
A0-A7	Address Inputs
CAS	Column Address Strobe
DQ1-DQ8	Data In/Data Out
G0-G1	Output Enable
RAS0-RAS1	Row Address Strobe
VDD	+5-V Supply
VSS	Ground
W	Write Enable

5 Dynamic RAM Modules

description

The TM4416E 8 are 256K, dynamic random-access memory module organized as 32,768 × 8 bits in a 24-pin single-in-line package comprising four TMS4416FPL, 16,384 x 4 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate with two 0.1 uF decoupling capacitors mounted on top. Each TMS4416FPL is described in the TMS4416 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as ammended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed. The TM4416E 8 series is rated for operation from 0 °C to 70 °C.

operation

The TM4416E8 operates as four TMS4416s connected as shown in the functional block diagram. Refer to the TMS4416 data sheet for details of its operation.

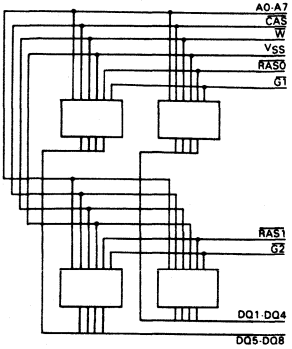
specifications

For TMS4416 electrical specifications, refer to the TMS4416 data sheet.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) MIN thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin over nickel plate.

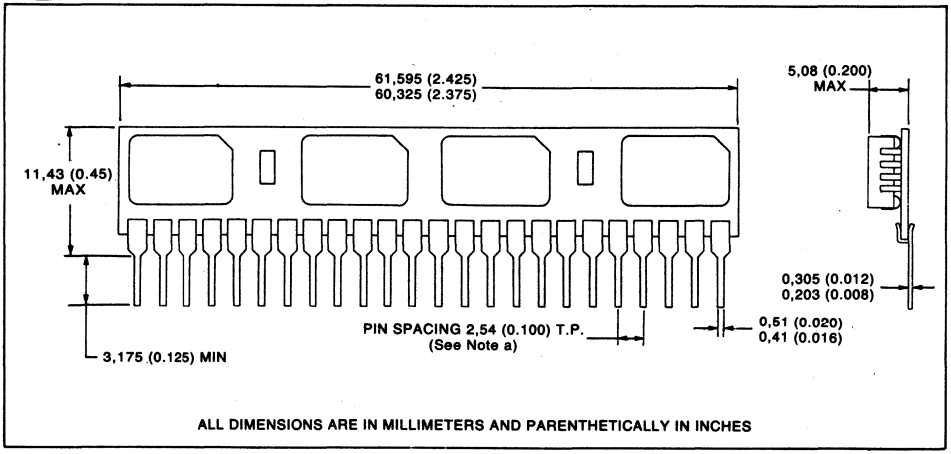
block diagram



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS0}$-1	Row Address Strobe
$\overline{W}$	Write Enable Input
DQ1-DQ8	Data In/Data Out
$\overline{G0}$-$\overline{G1}$	Output Enable
V_{DD}	+ 5V Supply
V_{SS}	Ground

MECHANICAL DATA

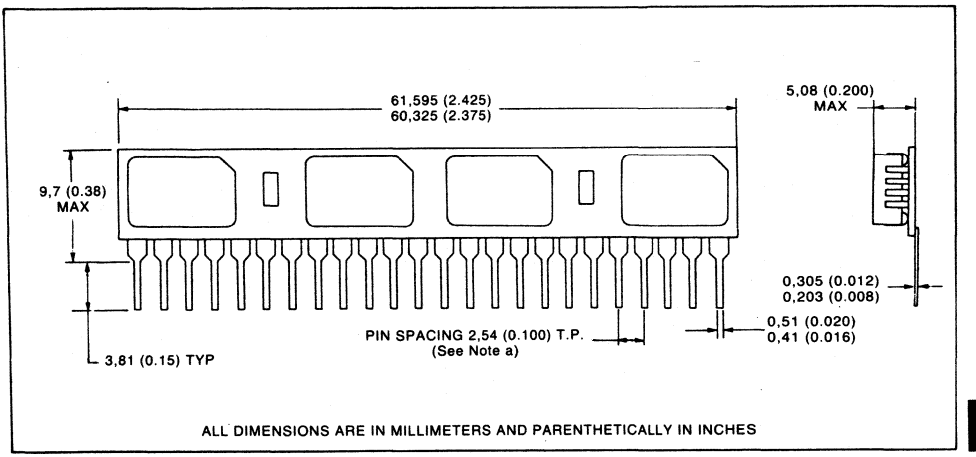
24 - Pin single-in-line packages
TM4416EE8



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TM4416EF8



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TI single-in-line package nomenclature

TM	4416	E	E	8	- 15	L
TI MODULE	MEMORY DEVICE	MODULE VERSION	PACKAGE SPECIFICATION	WORD WIDTH OUTPUT	SPEED	TEMPERATURE RANGE
			E : 61.59 x 11.43 mm (2.4 x 0.38 INCHES) **F : 61.59 x 9.7 mm (2.4 x 0.45 INCHES)**		**Max Access** **- 15 150 ns** **- 20 200 ns**	L 0°C to 70°C

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TM4164EA4, TM4164EC4, TM4164ED4
65,536 BY 4-BIT DYNAMIC RAM MODULES

DECEMBER 1983 - REVISED APRIL 1984

- 65,536 X 4 Organization
- Single +5-V Supply (10% Tolerance)
- 22-Pin Single-In-Line Package (SIP)
- Utilizes Four 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

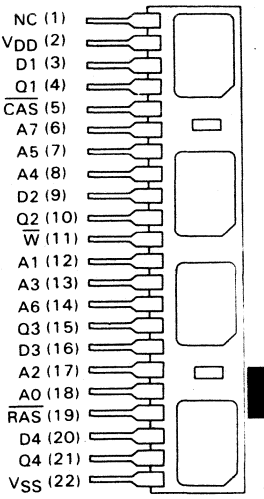
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS4164-12	120 ns	70 ns	230 ns	260 ns
TMS4164-15	150 ns	85 ns	260 ns	285 ns
TMS4164-20	200 ns	135 ns	330 ns	345 ns

- Common $\overline{CAS}$ Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164E 4-12	800 mW	70 mW
TM4164E 4-15	700 mW	70 mW
TM4164E 4-20	540 mW	70 mW

- Operating Free-Air Temperature . . . 0°C to 70°C
- Upward Compatible with 256K X 4 Single-In-Line Package

22-PIN
SINGLE-IN-LINE PACKAGE
(TOP VIEW)



This drawing shown for pin assignments only. Chip carrier orientation, number of capacitors and location vary with package used (see Mechanical Data).

PIN NOMENCLATURE	
A0 A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D1 D4	Data Inputs
NC	No Connection
Q1 Q4	Data Outputs
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4164E 4 series are 256K, dynamic random-access memory modules organized as 65,536 × 4 bits in a 22-pin single-in-line package comprising four TMS4164FPL, 65,536 × 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate. Two 0.1 μF decoupling capacitors are mounted on top of the substrate for TM4164EA4 and TM4164EC4 versions; four 0.1 μF decoupling capacitors are mounted on the bottom of the substrate for the TM4164ED4. Each TMS4164FPL is described in the TMS4164 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as ammended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed. The TM4164E 4 series is rated for operation from 0°C to 70°C.

upward compatibility

Future 256K × 4 memory modules in single-in-line packages will have identical pin functions and spacing, but will be 5,1 mm (0.2 inches) longer than the TM4164E 4 series; the length of the 256K × 4 (TM4256EE4) will be

PRELIMINARY DATA SHEET:
Supplementary data may be published at a late date.

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61,0 ± 0,6 mm MAX (2.400 ± 0.025 inches MAX). To ensure compatibility between the two devices, enough clearance should be allowed on the PC board design to accomodate the increased length of the TM4256EE4. Pin 1 of the TM4256EE4 module will be memory address A8.

operation

The TM4164E 4 series operates as four TMS4164s connected as shown in the functional block diagram. Refer to the TMS4164 data sheet for details of its operation.

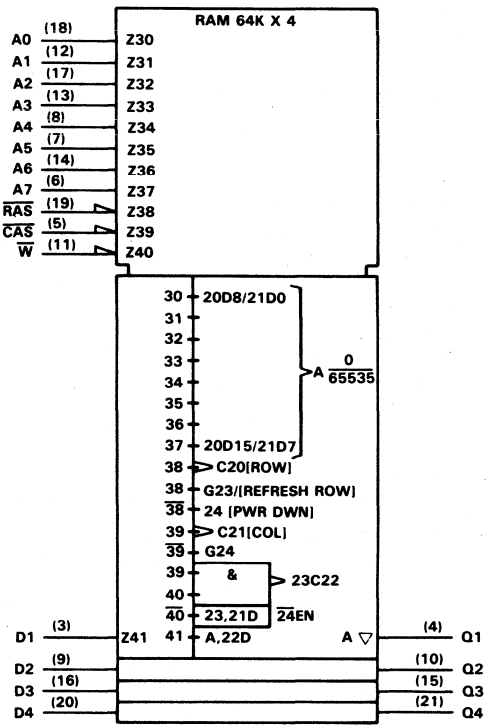
specifications

For TMS4164 electrical specifications, refer to the TMS4164 data sheet.

single-in-line package and components

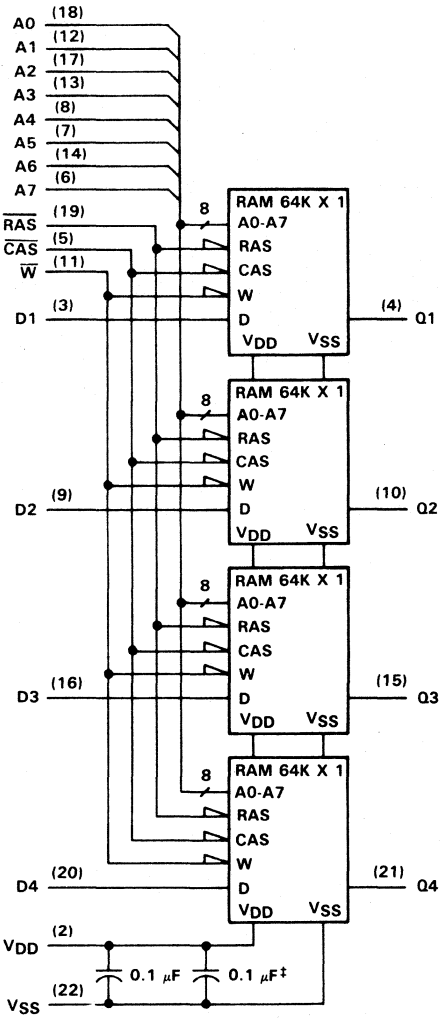
PC substrate: 0,79 mm (0.031 inch) minimum thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin over brass

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC.

functional block diagram

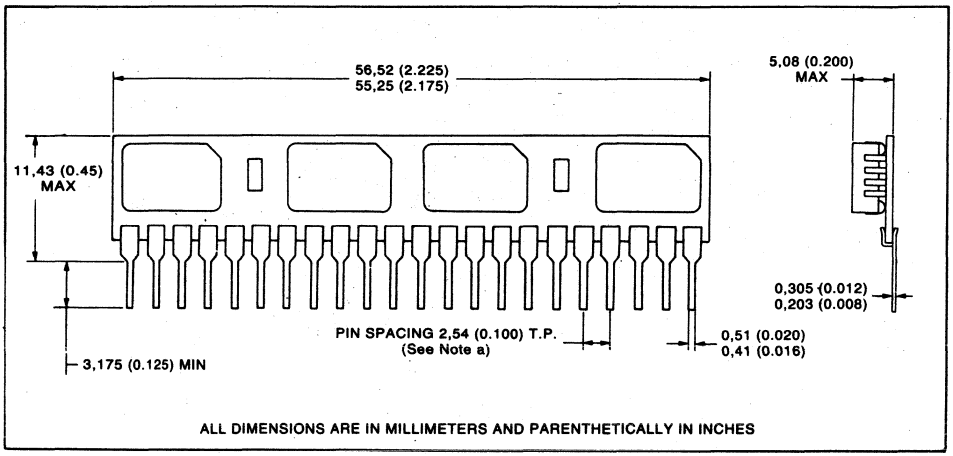


‡The TM4164EA4 and TM4164EC4 use two decoupling capacitors as shown; the TM4164ED4 uses four decoupling capacitors connected in parallel.

MECHANICAL DATA

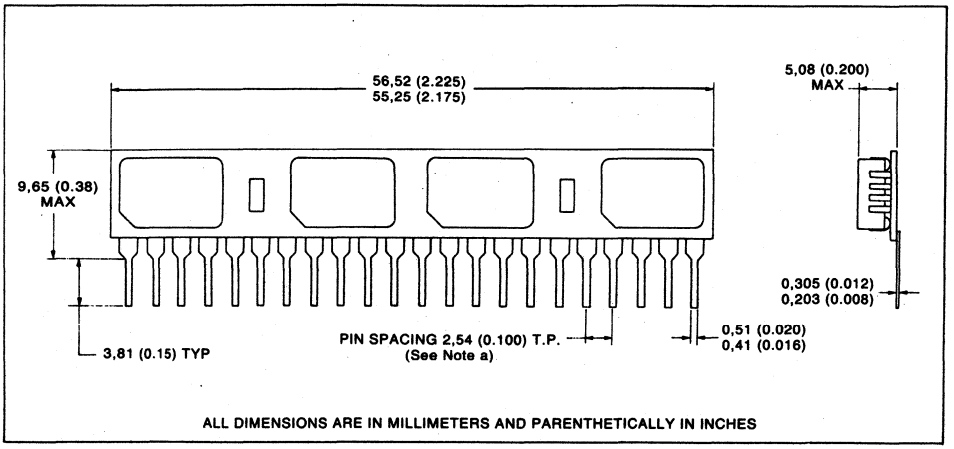
22-Pin single-in-line packages

TM4164EC4



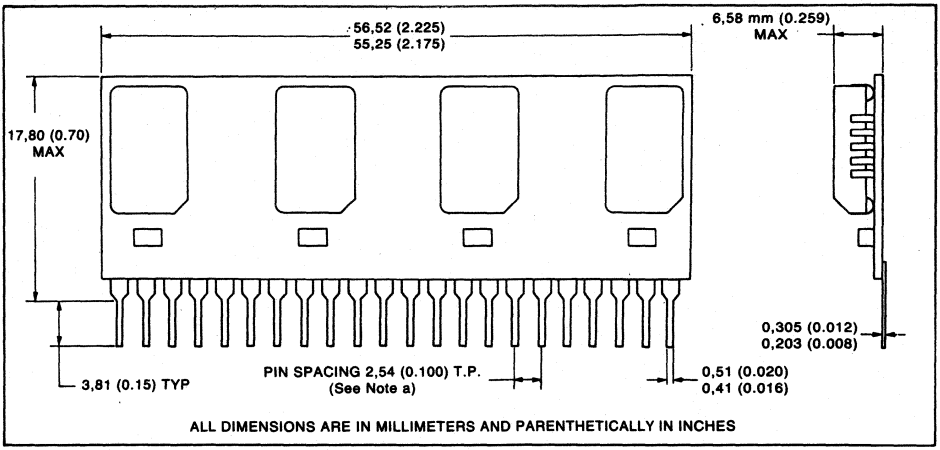
NOTE a. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.

TM4164EA4



NOTE a. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.

TM4164ED4



NOTE a: Each pin centerline is located within 0.25 (0.010) of its true longitudinal position

TI single-in-line package nomenclature

TM	4164	E	A	4	-15	L
TI MODULE	MEMORY DEVICE	MODULE VERSION	PACKAGE SPECIFICATION	WORD WIDTH OUTPUT	SPEED	TEMPERATURE RANGE

A: 55,88 x 9,65 mm (2.2 x 0.38 inches)
C: 55,88 x 11,43 mm (2.2 x 0.45 inches)
D: 55,88 x 17,80 mm (2.2 x 0.70 inches)

Max Access
-12 120 ns
-15 150 ns
-20 200 ns

L 0°C to 70°C

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TM4164EG5, TM4164EH5, TM4164EQ5
65,536 BY 5-BIT DYNAMIC RAM MODULE

NOVEMBER 1983 - REVISED APRIL 1984

- 65,536 X 5 Organization
- Single +5-V Supply (10% Tolerance)
- 24-Pin Single-In-Line Package (SIP)
- Utilizes Five 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

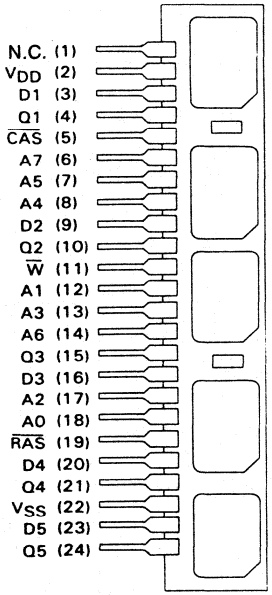
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS4164-12	120 ns	70 ns	230 ns	260 ns
TMS4164-15	150 ns	85 ns	260 ns	285 ns
TMS4164-20	200 ns	135 ns	330 ns	345 ns

- Common $\overline{CAS}$ Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164E 5-12	1000 mW	87.5 mW
TM4164E 5-15	875 mW	87.5 mW
TM4164E 5-20	675 mW	87.5 mW

- Decoupling Capacitors Ready Mounted on Substrate
- Operating Free-Air Temperature . . . 0°C to 70°C

24-PIN
SINGLE-IN-LINE PACKAGE†
(TOP VIEW)



This drawing shown for pin assignments only. Chip carrier orientation, number of capacitors and location vary with package used (see Mechanical Data).

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D1-D5	Data Inputs
NC	No Connection
Q1-Q5	Data Outputs
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4164E 5 series are 320K, dynamic random-access memory modules organized as 65,536 × 5 bits in a 24-pin single-in-line package comprising five TMS4164FPL, 65,536 × 1 bit dynamic RAMs in 18-lead plastic chip carriers mounted on top of a substrate. Two 0.1 μF decoupling capacitors are mounted on top of the substrate for TM4164EH5 and TM4164EQ5 versions: five 0.1 μF decoupling capacitors are mounted on the bottom of the substrate for the TM4164EG5. Each chip carrier meets the full specifications given in the TMS4164 data sheet. The TM4164E 5 series of modules are rated for operation from 0°C to 70°C.

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PRELIMINARY DATA SHEET:
Supplementary data may be published at a late date.

TEXAS INSTRUMENTS

operation

The TM4164E 5 series operates as five TMS4164s connected as shown in the functional block diagram. Refer to the TMS4164 data sheet for details of its operation.

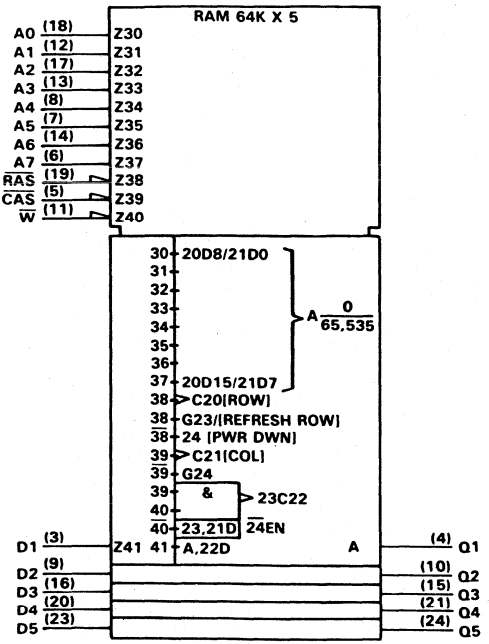
specifications

For TMS4164 electrical specifications, refer to the TMS4164 data sheet.

single-in-line packages

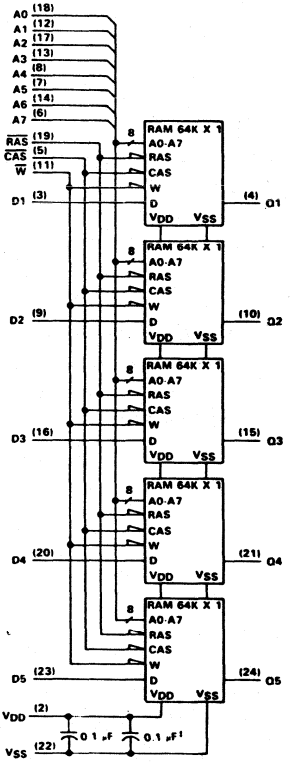
Three single-in-line packages are available for the TM4164E 5 (see mechanical data). All of the packages use tin over nickel plated leads.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32-14 and recent decisions by IEEE and IEC.

functional block diagram

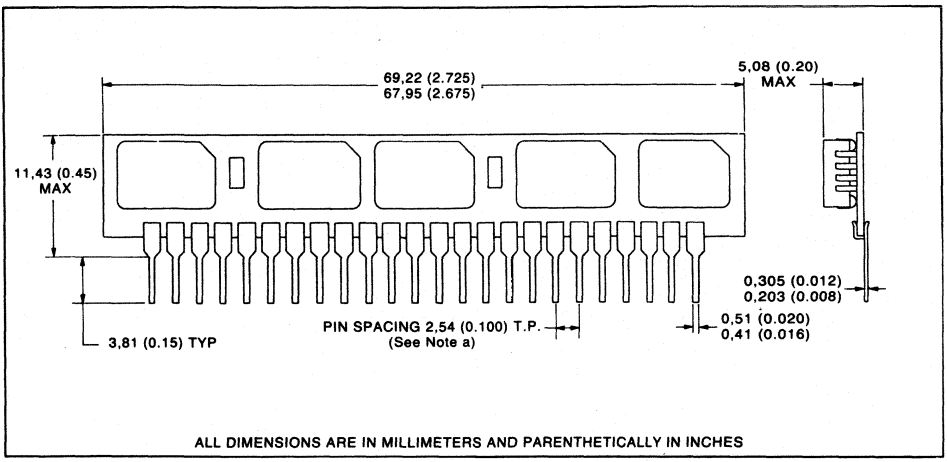


The TM4164EH5 and TM4164EQ5 use two decoupling capacitors as shown: the TM416EG5 uses five decoupling capacitors connected in parallel.

MECHANICAL DATA

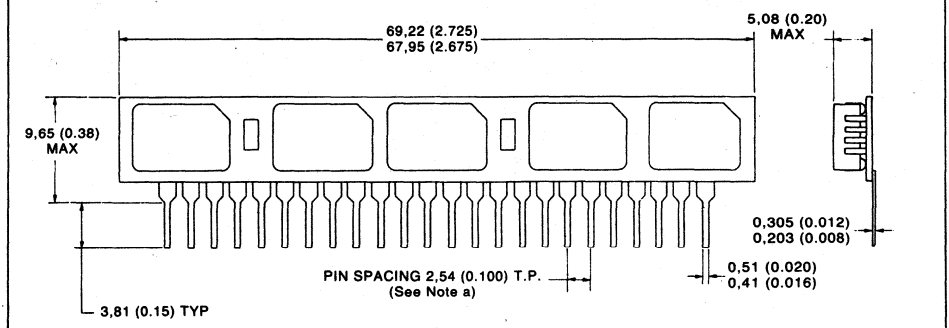
24 - Pin single-in-line packages

TM4164EQ5



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

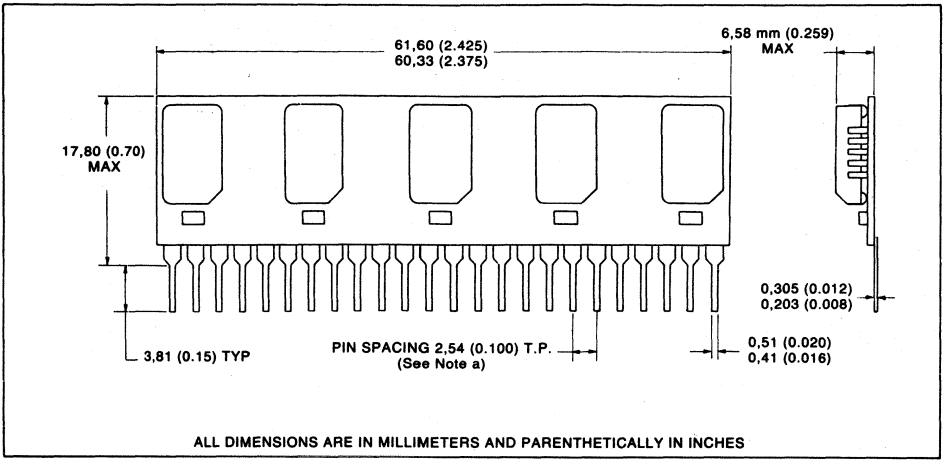
TM4164EH5



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TM4164EG5



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TI single-in-line package nomenclature

TM	4164	E	G	5	-15	L
TI MODULE	MEMORY DEVICE	MODULE VERSION	PACKAGE SPECIFICATION	WORD WIDTH OUTPUT	SPEED	TEMPERATURE RANGE

G: 60,96 x 17,80 mm (2.4 x 0.70 inches)
H: 68,58 x 9,65 mm (2.7 x 0.38 inches)
Q: 68,58 x 11,43 mm (2.7 x 0.45 inches)

Max Access	
-12	120 ns
-15	150 ns
-20	200 ns

L 0°C to 70°C

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TEXAS INSTRUMENTS

TM4164EK8
65,536 BY 8-BIT DYNAMIC RAM MODULE

NOVEMBER 1983 - REVISED APRIL 1984

- 65,536 X 8 Organization
- Single +5 V Supply (10% Tolerance)
- 30-Pin Single-In-Line Package (SIP)
- Utilizes Eight 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period ... 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

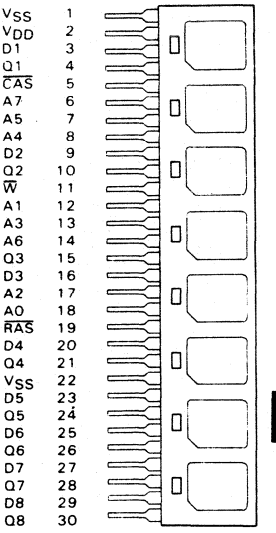
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS4164-12	120 ns	**70 ns**	230 ns	260 ns
TMS4164-15	150 ns	**85 ns**	260 ns	285 ns
TMS4164-20	200 ns	**135 ns**	330 ns	345 ns

- Common CAS Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164EK8-12	1600 mW	140 mW
TM4164EK8-15	1400 mW	140 mW
TM4164EK8-20	1080 mW	140 mW

- Operating Free-Air Temperature ... 0 °C to 70 °C

30-PIN
SINGLE-IN-LINE PACKAGE
(TOP VIEW)



This drawing shown for pin assignments only. Chip carrier orientation, number of capacitors and location vary with package used (see Mechanical Data).

PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
D1-D8	Data Inputs
NC	No Connection
Q1-Q8	Data Outputs
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4164EK8 is a 512K, dynamic random-access memory module organized as 65,536 x 8 bits in a 30-pin single-in-line package comprising eight TMS4164FPL, 65,536 x 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate with eight 0.1 uF decoupling capacitors mounted on the bottom. Each TMS4164FPL is described in the TMS4164 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as ammended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed. The TM4164EK8 is rated for operation from 0 °C to 70 °C.

operation

The TM4164EK8 operates as eight TMS4164s connected as shown in the functional block diagram. Refer to the TMS4164 data sheet for details of its operation.

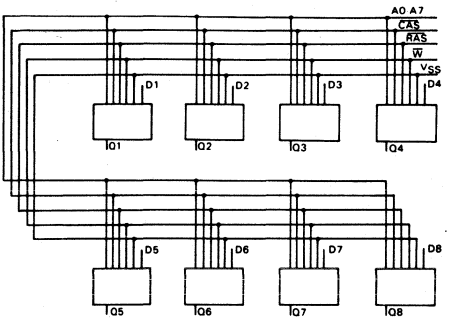
specifications

For TMS4164 electrical specifications, refer to the TMS4164 data sheet.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) MIN thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin over nickel plate.

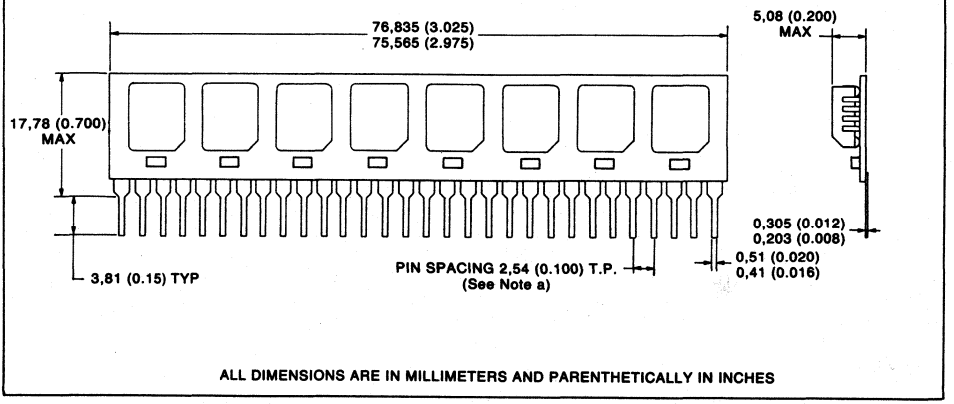
block diagram



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
D1-D8	Data Inputs
Q1-Q8	Data Outputs
$\overline{W}$	Write Enable Input
V_{DD}	+5V Supply
V_{SS}	Ground

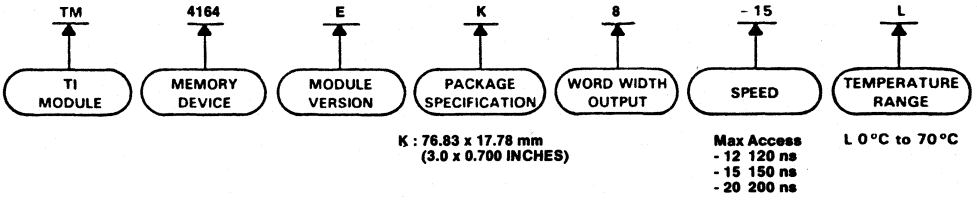
MECHANICAL DATA

30-pin single-in-line package



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TI single-in-line package nomenclature



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TM4164FN9
65,536 BY 9-BIT DYNAMIC RAM MODULE

NOVEMBER 1983 - REVISED APRIL 1984

- 65,536 X 9 Organization
- Single +5 V Supply (10% Tolerance)
- 32-Pin Single-In-Line Package (SIP)
- Utilizes Nine 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period ... 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

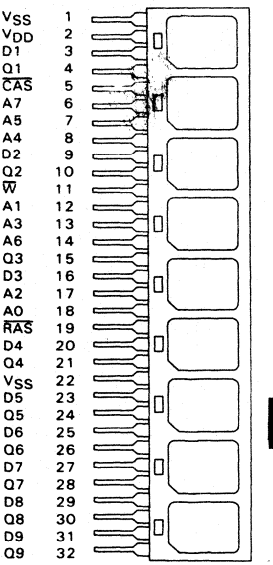
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS4164-12	120 ns	70 ns	230 ns	260 ns
TMS4164-15	150 ns	85 ns	260 ns	285 ns
TMS4164-20	200 ns	135 ns	330 ns	345 ns

- Common CAS Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164FN9-12	1800 mW	157,5 mW
TM4164FN9-15	1575 mW	157,5 mW
TM4164FN9-20	1215 mW	157,5 mW

- Operating Free-Air Temperature ... 0 °C to 70 °C

32-PIN
SINGLE-IN-LINE PACKAGE
(TOP VIEW)



This drawing shown for pin assignments only. Chip carrier orientation, number of capacitors and location vary with package used (see Mechanical Data).

PIN NOMENCLATURE	
A0-A7	Address Inputs
CAS	Column Address Strobe
D1-D9	Data Inputs
NC	No Connection
Q1-Q9	Data Outputs
RAS	Row Address Strobe
VDD	+5-V Supply
VSS	Ground
W	Write Enable

description

The TM4164FN9 is a 576K, dynamic random-access memory module organized as 65,536 x 9 bits in a 32-pin single-in-line package comprising nine TMS4164FPL, 65,536 x 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate with nine 0.1 uF decoupling capacitors mounted on the bottom. Each TMS4164FPL is described in the TMS4164 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as ammended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed. The TM4164FN9 is rated for operation from 0 °C to 70 °C.

operation

The TM4164FN9 operates as nine TMS4164s connected as shown in the functional block diagram. Refer to the TMS4164 data sheet for details of its operation.

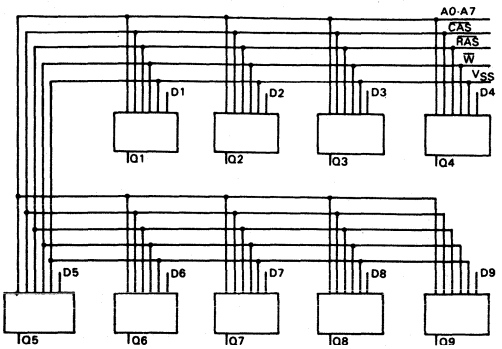
specifications

For TMS4164 electrical specifications, refer to the TMS4164 data sheet.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) MIN thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin over nickel plate.

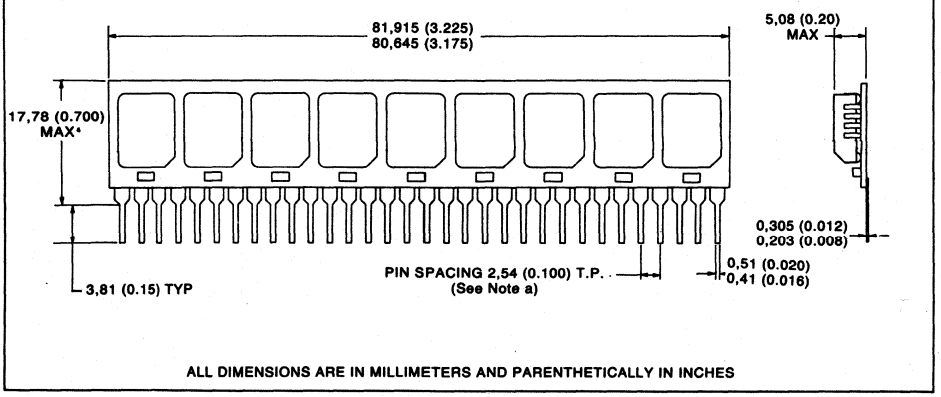
block diagram



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
D1-D9	Data Inputs
Q1-Q9	Data Outputs
$\overline{W}$	Write Enable Input
V_{DD}	+5V Supply
V_{SS}	Ground

MECHANICAL DATA

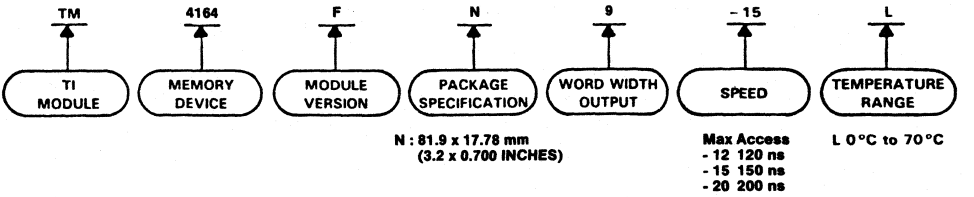
32 - Pin single-in-line packages



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TI single-in-line package nomenclature



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TM4164FC1, TM4164FA1
262,144 BY 1-BIT DYNAMIC RAM MODULE

NOVEMBER 1983 - REVISED APRIL 1984

- 262,144 X 1 Organization
- Single +5 V Supply (10% Tolerance)
- 22-Pin Single-In-Line Package (SIP)
- Utilizes Four 64K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period ... 4 ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs:

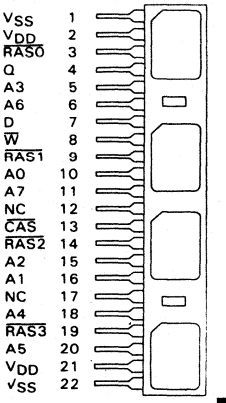
	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY, WRITE CYCLE (MIN)
TMS4164-12	120 ns	70 ns	230 ns	260 ns
TMS4164-15	150 ns	85 ns	260 ns	285 ns
TMS4164-20	200 ns	135 ns	330 ns	345 ns

- Common CAS Control with Separate Data-In and Data-Out Lines
- Low Power Dissipation:

	OPERATING (TYP)	STANDBY (TYP)
TM4164F 1-12	800 mW	70 mW
TM4164F 1-15	700 mW	70 mW
TM4164F 1-20	540 mW	70 mW

- Operating Free-Air Temperature ... 0 °C to 70 °C

22-PIN
SINGLE-IN-LINE PACKAGE
(TOP VIEW)



This drawing shown for pin assignments only. Chip carrier orientation, number of capacitors and location vary with package used (see Mechanical Data).

PIN NOMENCLATURE	
A0-A7	Address Inputs
CAS	Column Address Strobe
D	Data Input
NC	No Connection
Q	Data Output
RAS0-RAS3	Row Address Strobe
VDD	+5-V Supply
VSS	Ground
W	Write Enable

description

The TM416F 1 are 256K, dynamic random-access memory module organized as 262,144 x 1 bits in a 22-pin single-in-line package comprising four TMS4164FPL, 65,536 x 1 bit dynamic RAM's in 18-lead plastic chip carriers mounted on top of a substrate with two 0.1 uF decoupling capacitors mounted on the bottom. Each TMS4164FPL is described in the TMS4164 data sheet and is fully electrically tested and processed according to TI's MIL-STD-883B (as ammended for commercial applications) flows prior to assembly. After assembly onto the substrate, a further set of electrical tests is performed. The TM4164F 1 is rated for opetion from 0 °C to 70 °C.

operation

The TM4164F 1 operates as nine TMS4164s connected as shown in the functional block diagram. Refer to the TMS4164 data sheet for details of its operation.

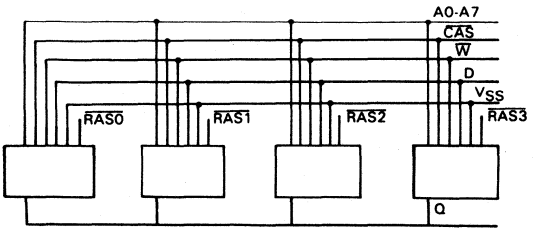
specifications

For TMS4164 electrical specifications, refer to the TMS4164 data sheet.

single-in-line package and components

PC substrate: 0,79 mm (0.031 inch) MIN thickness
Bypass capacitors: Multilayer ceramic
Leads: Tin over nickel plate.

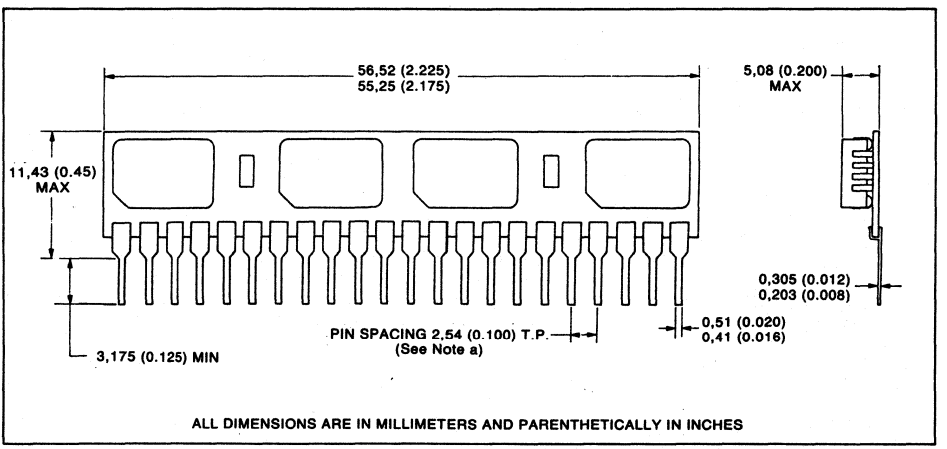
block diagram



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Write Enable Input
D	Data Input
Q	Data Output
V_{DD}	+5V Supply
V_{SS}	Ground

MECHANICAL DATA

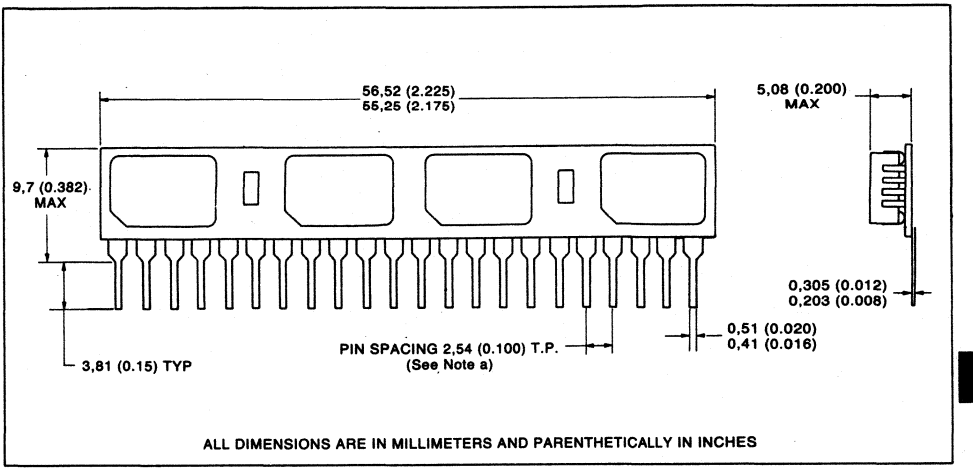
TM4164FC1



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

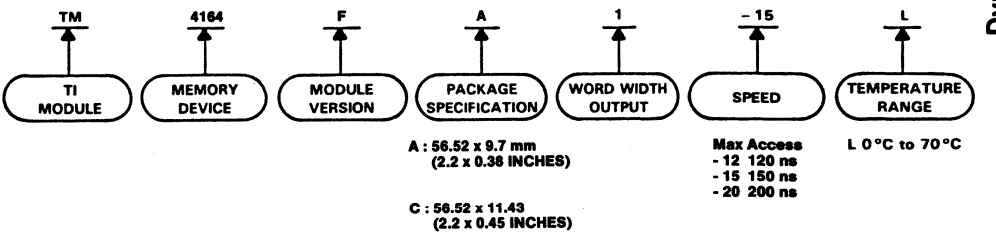
Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

22 - Pin single-in-line packages
TM4164FA1



NOTE: a. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TI single-in-line package nomenclature



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TI EPROMS INCORPORATE FAST PROGRAMMING CAPABILITY

The TMS2764 64K EPROM and TMS27128 128K EPROM (industry standard JEDEC approved pin outs) may be programmed with the fast programming algorithm reducing programming time by a factor of 5 to 10X.

The TMS2516 16K EPROM, TMS2532 32K EPROM, TMS2564 64K EPROM and TMS2732A 32K EPROM (JEDEC approved pin out) may be programmed with either the standard 50-millisecond pulse or a fast 10-millisecond pulse.

To take advantage of fast programming on TI EPROMs commercial programmers require the revision shown below.

PROGRAMMERS	TI EPROMs	
	TMS2516 TMS2532 TMS2564 TMS2732A	TMS2764 TMS27128
DATA I/O		
Model 120A/121	Revision G/V07*	Revision D*
Unipak	Revision V07*	Revision V04*
Unipak 2	Revision V05*	Revision V03*
PROLOG		
M980/M910A Control Unit PM9080 Personality Module PA28/80B Pin Out Adapter	Update PROM UDP4	No Update PROM is required

* Subsequent revisions are also valid

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is available from Texas Instruments in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

Please contact

Texas Instruments
P.O. Box 401560
Dallas, Texas 75240

to obtain this brochure.

TMS2516, SMJ2516
16,384-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

DECEMBER 1979 – REVISED AUGUST 1983

- Organization . . . 2048 X 8
- Single +5-V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (16K, 32K, and 64K)
- JEDEC Standard Pinout
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time:

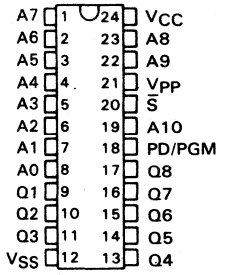
  '2516-35 350 ns
  '2516-45 450 ns

- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Low Power Dissipation:

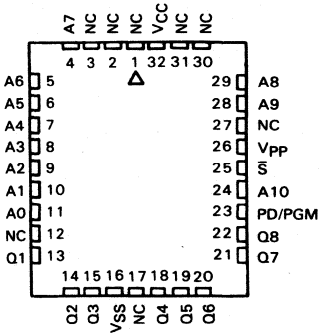
  Active . . . 285 mW Typical
  Standby . . . 100 mW Typical

- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Available in Full Military Temperature Range Version (SMJ2516)

TMS2516 . . . JL PACKAGE
SMJ2516 . . . J PACKAGE
(TOP VIEW)



SMJ2516 . . . FG PACKAGE
(TOP VIEW)



description

The '2516 series are 16,384-bit, ultraviolet-light erasable, electrically-programmable read-only memories. These devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54/74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 54/74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The '2516 is plug-in compatible with the '4016 16K static RAM.

PIN NOMENCLATURE	
A(N)	Address Inputs
NC	No Internal Connection
PD/PGM	Power Down/Program
Q(N)	Data Outputs
$\overline{S}$	Chip Select
V_{CC}	+5-V Power Supply
V_{PP}	+25-V Power Supply
V_{SS}	0-V Ground

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The TMS2516s are offered in a dual-in-line cerpak package (JL suffix), rated for operation form 0°C to 70°C. The SMJ' devices are offered in a 24-pin dual-in-line ceramic package (J) and in a 32-pad leadless ceramic chip carrier (FG). The J package is designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers, whereas the FG package is intended for surface mounting on solder pads on 0.050-inch (1,27 mm) centers. The FG package offers a three layer rectangular chip carrier with dimensions 0.450 × 0.550 × 0.100 (11,42 × 13,97 × 2,54).

Since these EPROMs operate from a single +5 V supply (in the read mode), they are ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 10-ms pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 20 seconds.

operation

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down	Start Programming	Inhibit Programming	Program Verification
PD/PGM (18)	V_{IL}	Don't Care	V_{IH}	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IL}
$\overline{S}$ (20)	V_{IL}	V_{IH}	Don't Care	V_{IH}	V_{IH}	V_{IL}
V_{PP} (21)	+5 V	+5 V	+5 V	+25 V	+25 V	+25 V (or +5 V)
V_{CC} (24)	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
Q (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	HI-Z	Q

read/output disable

When the outputs of two or more '2516s are connected to the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. The device whose output is to be read should have a low-level TTL signal applied to the $\overline{S}$ and PD/PGM pins. All other devices in the circuit should have their outputs disabled by applying high-level signals to these same pins. PD/PGM can be left low, but it may be advantageous to power down the device during output disable. Output data is accessed at pins Q1 through Q8. On the '2516-45, data can be accessed in 450 ns and access time from $\overline{S}$ is 150 ns. On the '2516-35, data can be accessed in 350 ns and access time from $\overline{S}$ is 120 ns. These access times assume that the addresses are stable.

power down

Active power dissipation can be cut by 64% by applying a high TTL signal to the PD/PGM pins. in this mode all outputs are in a high-impedance state.

erasure

Before programming, the '2516 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light having a wavelength of 253.7 nm (2537 angstroms). The recommended minimum exposure dose (UV intensity times exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12-milliwatt per-square-centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are in the "1" state (assuming a high-level output corresponds to logic "1"). It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the '2516, the window should be covered with an opaque lid.

start programming

After erasure (all bits in logic "1" state), logic "0's" are programmed into the desired locations. A "0" can be erased only by ultraviolet light. The programming mode is achieved when V_{PP} is 25 V and $\overline{S}$ is at V_{IH}. Data is presented

in parallel (8 bits) on pins Q1 through Q8. Once addresses and data are stable, a 10-millisecond TTL high-level pulse should be applied to the PGM pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. Several '2516s can be programmed simultaneously when the devices are connected in parallel.

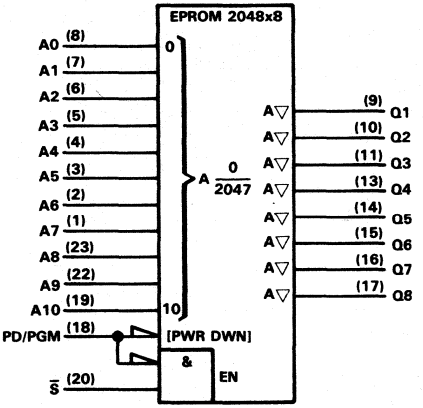
inhibit programming

When two or more devices are connected in parallel, data can be programmed into all devices or only chosen devices. '2516s not intended to be programmed (i.e., inhibited) should have a low level applied to the PD/PGM pin and a high-level applied to the $\overline{S}$ pin.

program verification

A verification is done to see if the device was programmed correctly. A verification can be done at any time. It can be done on each location immediately after that location is programmed. To do a verification, V_{PP} may be kept at +25 V.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions in IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 7 V
Supply voltage, V_{PP} (see Note 1)	−0.3 V to 28 V
All input voltages (see Note 1)	−0.3 V to 7 V
Output voltage (operating, with respect to V_{SS})	−0.3 V to 7 V
Operating free-air temperature range: TMS'	0°C to 70°C
Operating case temperature range: SMJ'	−55°C to 125°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: 1. Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{SS} (substrate).

recommended operating conditions

PARAMETER	TMS2516-35			TMS2516-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.1		0.8	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$	350			450			ns
Operating free-air temperature, T_A	0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (±1 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS2516			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V			±10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V, PD/PGM = V_{IL}			6	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/PGM = V_{IH}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/PGM = V_{IH}		20	30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{S}$ = PD/PGM = V_{IL}		57	100	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage and operating free-air temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TMS2516		UNIT
			TYP‡	MAX	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	TMS2516-35			TMS2516-45			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leq 20$ ns, $t_f \leq 20$ ns		250	350		280	450	ns
$t_{a(S)}$	Access time from chip select				120			150	ns
$t_{a(PR)}$	Access time from PD/PGM			250	350		280	450	ns
$t_{v(A)}$	Output data valid after address change		0			0			ns
$t_{dis(S)}$	Output disable time from chip select during read only‡		0		100	0		100	ns
$t_{dis(S)}$	Output disable time from chip select during program and program verify‡				120			120	ns
$t_{dis(PR)}$	Output disable time from PD/PGM‡		0		100			100	ns

† All typical values are at T_A = 25°C and nominal voltages.
‡ Value calculated from 0.5 volt delta to measured output level.

recommended timing requirements for programming T_A = 25°C (see Note 4)

PARAMETER		TMS2516			UNIT
		MIN	TYP†	MAX	
$t_{w(PR)}$	Pulse duration, program pulse	9		55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(S)}$	Chip-select setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(S)}$	Chip-select hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs

† Typical values are at nominal voltages.
NOTES: 4. Timing measurement reference levels: inputs 0.8 V and 2 V, outputs 0.65 V and 2.2 V.
5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$, $t_{a(S)}$, and t_{dis}, PD/PGM = $\overline{S}$ = V_{IL}.

recommended operating conditions

PARAMETER	SMJ2516-35			SMJ2516-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.1		0.8	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$	350			450			ns
Operating case temperature, T_C	−55		125	−55		125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 25 V (±1 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	SMJ2516			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V			±10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V, PD/PGM = V_{IL}			6	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/PGM = V_{IH}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/PGM = V_{IH}		20	30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{S}$ = PD/PGM = V_{IL}		57	100	mA

† Typical values are at T_C = 25°C and nominal voltages.

capacitance over recommended supply voltage and operating case temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	SMJ2516		UNIT
			TYP‡	MAX	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_C = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	SMJ2516-35			SMJ2516-45			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 54 TTL load, $t_r \leq 20$ ns, $t_f \leq 20$ ns		250	350		280	450	ns
$t_{a(S)}$	Access time from chip select				120			150	ns
$t_{a(PR)}$	Access time from PD/PGM			250	350		280	450	ns
$t_{v(A)}$	Output data valid after address change		0			0			ns
$t_{dis(S)}$	Output disable time from chip select during read only‡		0		100	0		100	ns
$t_{dis(S)}$	Output disable time from chip select during program and program verify‡				120			120	ns
$t_{dis(PR)}$	Output disable time from PD/PGM‡		0		100			100	ns

† All typical values are at T_C = 25°C and nominal voltages.
‡ Value calculated from 0.5 volt delta to measured output

recommended timing requirements for programming T_C = 25°C (see Note 4)

PARAMETER		SMJ2516			UNIT
		MIN	TYP†	MAX	
$t_{w(PR)}$	Pulse duration, program pulse	9		55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(S)}$	Chip-select setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from Vpp	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(S)}$	Chip-select hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs

† Typical values are at nominal voltages.
NOTES: 4. Timing measurement reference levels: inputs 0.8 V and 2 V, outputs 0.65 V and 2.2 V.
5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$, $t_{a(S)}$, and t_{dis}, PD/PGM = $\overline{S}$ = V_{IL}.

PARAMETER MEASUREMENT INFORMATION

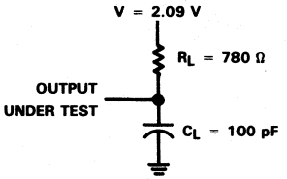
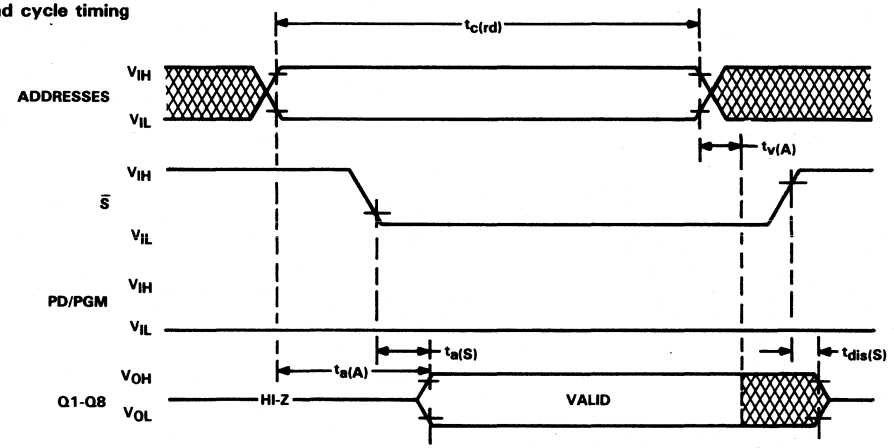
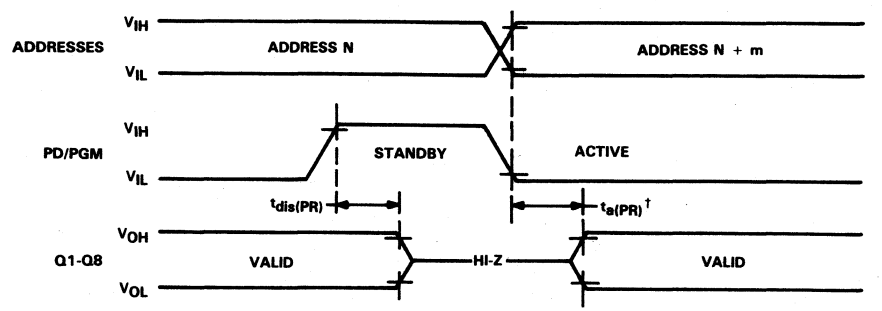


FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing

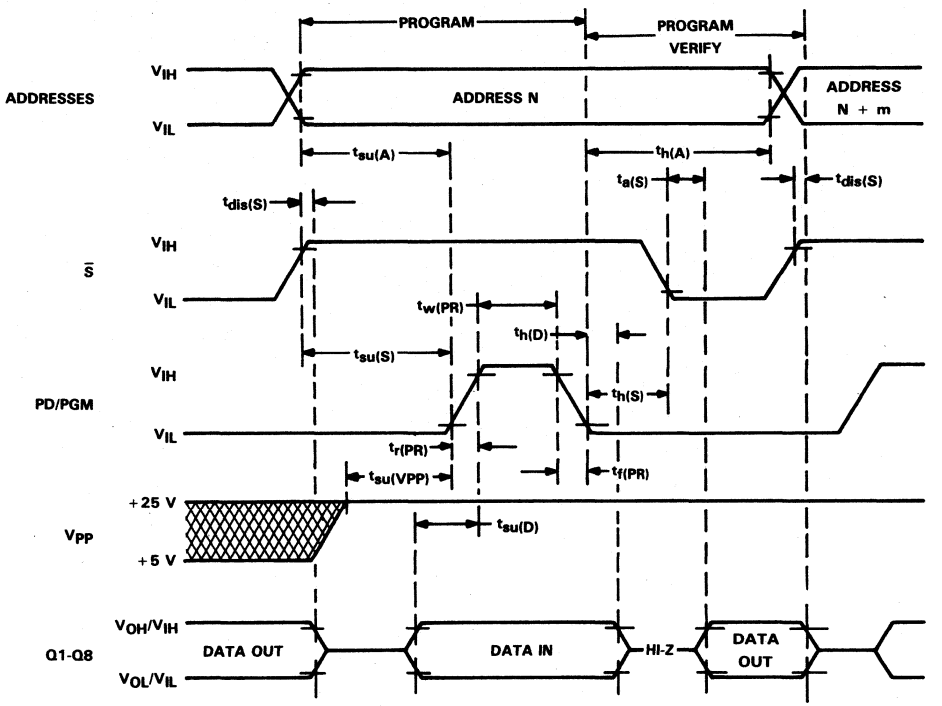


standby mode



NOTE: $\overline{S}$ must be in low state during Active Mode, "Don't Care" otherwise.
† $t_{a(PR)}$ referenced to PD/PGM or the address, whichever occurs last.

program cycle timing



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS2532, SMJ2532
32,768-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

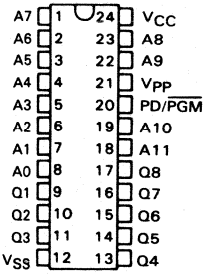
DECEMBER 1979 – REVISED SEPTEMBER 1983

- Organization . . . 4096 X 8
- Single +5-V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)
- JEDEC Standard Pinout
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time:

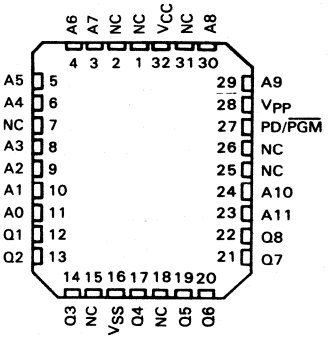
'2532-30	300 ns
'2532-35	350 ns
'2532-45	450 ns

- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Low Power Dissipation:
  - Active . . . 400 mW Typical
  - Standby . . . 100 mW Standby
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Available in Full Military Temperature Range Version (SMJ2532)

TMS2532 . . . JL PACKAGE
SMJ2532 . . . J PACKAGE
(TOP VIEW)



SMJ2532 . . . FE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address Inputs
NC	No Internal Connection
PD/$\overline{PGM}$	Power Down/Program
Q(N)	Data Outputs
V_{CC}	+5-V Power Supply
V_{PP}	+25-V Supply
V_{SS}	0-V Ground

description

The '2532 series are 32,768-bit, ultraviolet-light-erasable, electrically-programmable read-only memories. These devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54/74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 54/74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS2532 series are plug-in compatible with the TMS4732 32K ROM.

The TMS2532's are offered in a dual-in-line ceramic package (JL suffix), rated for operation from 0°C to 70°C. The SMJ' devices are offered in a 24-pin dual-in-line ceramic package (J) and in a 32-pad leadless ceramic chip carrier (FE). The J package is designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers, whereas the FE package is intended for surface mounting on solder pads on 0.050-inch (1,27 mm) centers. The FE package offers a three-layer rectangular chip carrier with dimensions 0.450 × 0.550 × 0.100 (11,43 × 13,97 × 2,54 mm).

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Since these EPROMs operate from a single +5 V supply (in the read mode), they are ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 10 ms pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 41 seconds.

operation

FUNCTION (PINS)	MODE				
	Read	Output Disable	Power Down	Start Programming	Inhibit Programming
PD/$\overline{PGM}$ (20)	V_{IL}	V_{IH}	V_{IH}	Pulsed V_{IH} to V_{IL}	V_{IH}
V_{PP} (21)	+5 V	+5 V	+5 V	+25 V	+25 V
V_{CC} (24)	+5 V	+5 V	+5 V	+5 V	+5 V
Q (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	HI-Z

read/out disable

When the outputs of two or more '2532s are connected on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. The device whose output is to be read should have a low-level TTL signal applied to the PD/$\overline{PGM}$ pin. All other devices in the circuit should have their outputs disabled by applying a high-level signal to this pin. Output data is accessed at pins Q1 through Q8.

power down

Active power dissipation can be cut by over 70% by applying a high TTL signal to the PD/$\overline{PGM}$ pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the '2532 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light having a wavelength of 253.7 nm (2537 angstroms). The recommended minimum exposure dose (UV intensity times exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are in the "1" state (assuming high-level output corresponds to logic "1"). It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore when using the '2532, the window should be covered with an opaque label.

start programming

After erasure (all bits in logic "1" state), logic "0's" are programmed into the desired locations. A "0" can be erased only by ultraviolet light. The programming mode is achieved when V_{PP} is 25 V. Data is presented in parallel (8 bits) on pins Q1 through Q8. Once addresses and data are stable, a 10-millisecond TTL low-level pulse should be applied to the $\overline{PGM}$ pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. Several '2532s can be programmed simultaneously when the devices are connected in parallel.

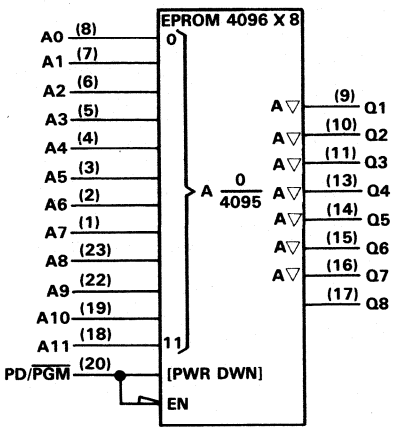
inhibit programming

When two or more devices are connected in parallel, data can be programmed into all devices or only chosen devices. Any '2532s not intended to be programmed should have a high level applied to PD/$\overline{PGM}$.

program verification

The '2532 program verification is simply the read operation, which can be performed as soon as V_{PP} returns to +5 V ending the program cycle.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} (see Note 1)	−0.3 V to 7 V
Supply voltage, V_{PP} (see Note 1)	−0.3 V to 28 V
All input voltages (see Note 1)	−0.3 V to 7 V
Output voltage (operating, with respect to V_{SS})	−0.3 V to 7 V
Operating free-air temperature range: TMS2532	0°C to 70°C
Operating case temperature range: SMJ2532	−55°C to 125°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{SS} (substrate).

recommended operating conditions

PARAMETER	TMS2532-30			TMS2532-35			TMS2532-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}			V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0			0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	2		$V_{CC}+1$	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.1		0.8	−0.1		0.8	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$	300			350			450			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (± 1 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS2532			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V			±10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V, PD/$\overline{PGM}$ = V_{IL}			12	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/$\overline{PGM}$ = V_{IL}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/$\overline{PGM}$ = V_{IH}		20	30	mA
I_{CC2}	V_{CC} supply current (active)	PD/$\overline{PGM}$ = V_{IL}		80	160	mA

capacitance over recommended voltage and operating free-air temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TMS2532		UNIT
			TYP‡	MAX	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (See Notes 4 & 5)	TMS2532-30			TMS2532-35			TMS2532-45			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \le 20$ ns, $t_f \le 20$ ns, See Figure 1.			300			350		280	450	ns
$t_{a(PR)}$	Access time from PD/$\overline{PGM}$				300			350		280	450	ns
$t_{v(A)}$	Output data valid after address change		0			0			0			ns
t_{dis}	Output disable time from PD/$\overline{PGM}$‡				100			100			100	ns

† All typical values are at T_A = 25°C and nominal voltages.
‡ Value calculated from 0.5 volt delta to measured output level.

recommended timing requirements for programming T_A = 25°C (see Note 4)

PARAMETER		TMS2532			UNIT
		MIN	TYP†	MAX	
$t_{w(PR)}$	Pulse duration, program pulse	9		55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(PR)}$	Program pulse hold time	0			ns
$t_{h(VPP)}$	V_{PP} hold time	2			μs

† Typical values are at nominal voltages.

NOTES: 4. Timing measurement reference levels: inputs 0.8 V and 2 V, outputs 0.65 V and 2.2 V.

5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$ and t_{dis}, PD/$\overline{PGM}$ = V_{IL}.

recommended operating conditions

PARAMETER	SMJ2532-35			SMJ2532-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.5	5	5.5	4.5	5	5.5	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.1		0.8	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$	350			450			ns
Operating case temperature, T_C	−55		125	−55		125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} is applied.
3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 25 V (± 1 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	SMJ2532			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V			±10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.5 V, PD/$\overline{PGM}$ = V_{IL}			12	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/$\overline{PGM}$ = V_{IL}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/$\overline{PGM}$ = V_{IH}		20	30	mA
I_{CC2}	V_{CC} supply current (active)	PD/$\overline{PGM}$ = V_{IL}		80	160	mA

capacitance over recommended voltage and operating case temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	SMJ2532		UNIT
			TYP‡	MAX	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_C = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (See Notes 4 & 5)	SMJ2532-35			SMJ2532-45			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 54 TTL Load, t_r ≤20 ns, t_f ≤20 ns, See Figure 1.			350		280	450	ns
$t_{a(PR)}$	Access time from PD/$\overline{PGM}$				350		280	450	ns
$t_{v(A)}$	Output data valid after address change		0			0			ns
t_{dis}	Output disable time from PD/$\overline{PGM}$‡				100			100	ns

† All typical values are T_C = 25°C and nominal voltages.
‡ Value calculated from 0.5 volt delta to measured output level.

NOTES: 4. Timing measurement reference levels: inputs 0.8 V and 2 V, outputs 0.65 V and 2.2 V.
5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$ and t_{dis}, PD/$\overline{PGM}$ = V_{IL}.

recommended timing requirements for programming T_C = 25°C (see Note 4)

PARAMETER		SMJ2532			UNIT
		MIN	TYP†	MAX	
$t_{w(PR)}$	Pulse duration, program pulse	9		55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(PR)}$	Program pulse hold time	0			ns
$t_{h(VPP)}$	V_{PP} hold time	2			μs

† Typical values are at nominal voltages.

NOTES: 4. Timing measurement reference levels: inputs 0.8 V and 2 V, outputs 0.65 V and 2.2 V.

5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$ and t_{dis}, $\overline{PD/PGM} = V_{IL}$.

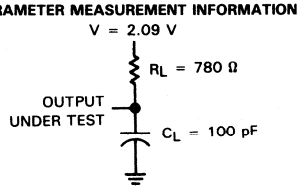
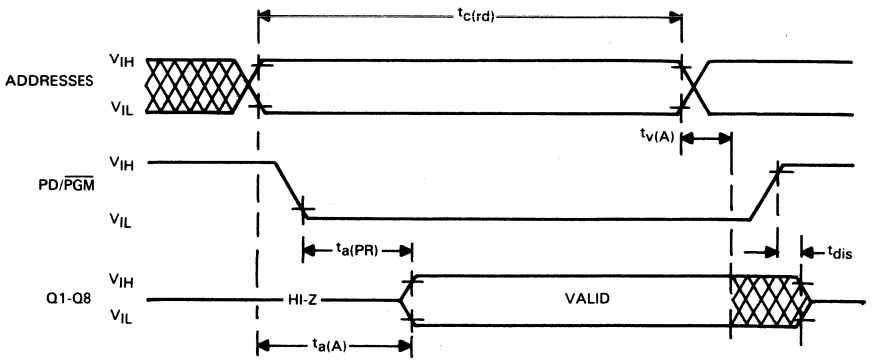


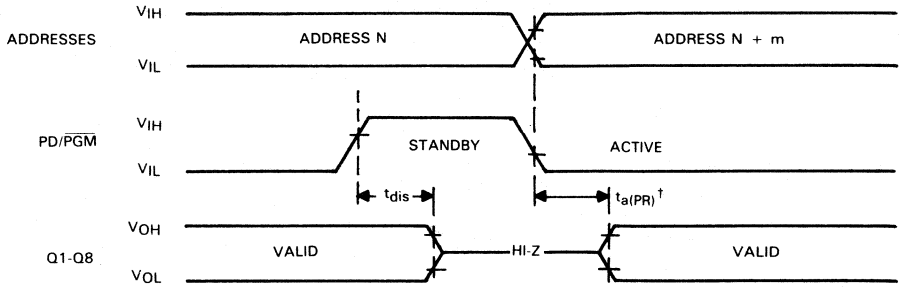
FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



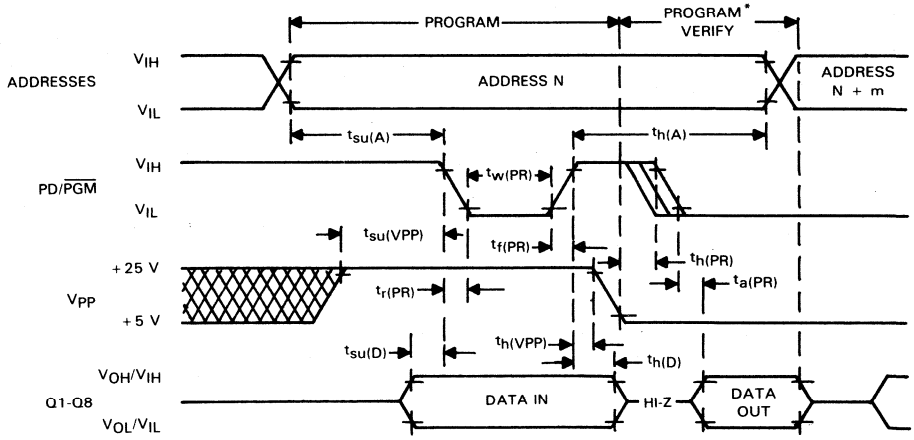
NOTE: There is no chip select pin on the '2532.
The chip-select function is incorporated in the power-down mode.

standby mode



† $t_{a(PR)}$ referenced to PD/$\overline{PGM}$ or the address, whichever occurs last.

program cycle timing



* Program verify equivalent to read mode.

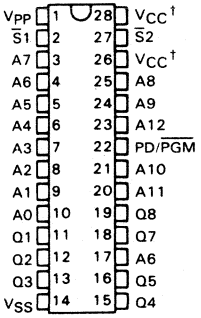
Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS2564, SMJ2564
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

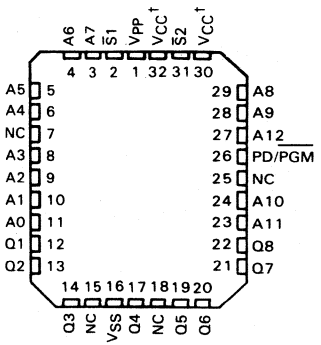
MAY 1981 – REVISED SEPTEMBER 1983

- **Organization . . . 8192 X 8**
- **Single +5-V Power Supply**
- **Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)**
- **All Input/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time:**
  - **TMS2564-35 . . . 350 ns**
  - **TMS2564-45 . . . 450 ns**
  - **SMJ2564-45 . . . 450 ns**
- **8-Bit Output for Use in Microprocessor-Based Systems**
- **N-Channel Silicon-Gate Technology**
- **3-State Output Buffers**
- **Guaranteed DC Noise Immunity with Standard TTL Loads**
- **No Pull-Up Resistors Required**
- **Low Power Dissipation:**
  - **Active . . . 400 mW Typical**
  - **Standby . . . 125 mW Typical**
- **Available in Full Military Temperature Range Version (SMJ2564)**

TMS2564 . . . JL OR JDL PACKAGE
SMJ2564 . . . J PACKAGE
(TOP VIEW)



SMJ2564 . . . FE PACKAGE
(TOP VIEW)



†Connected internally, V_{CC} need be supplied to only one of these two pins.

PIN NOMENCLATURE	
A(N)	Address Inputs
NC	No Connection
PD/$\overline{PGM}$	Power Down/Program
Q(N)	Input/Output
$\overline{S}$(N)	Chip Selects
V_{CC}	+5-V Power Supply
V_{PP}	+25-V Power Supply
V_{SS}	0-V Ground

description

The '2564 is a 65,536-bit ultraviolet-light-erasable, electrically-programmable read-only memory. This device is fabricated using N-channel silicon-gate technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54/74 TTL circuits without the use of external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

The TMS2564 is offered in a dual-in-line ceramic package (JL or JDL suffix) rated for operation from 0°C to 70°C. The SMJ2564 is offered in a 28-pin dual-in-line ceramic package (J) and a leadless ceramic chip carrier (FE), rated for operation from −55°C to 125°C. The J package is designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers, whereas the FE package is intended for surface mounting on solder pads on 0.050-inch (1,27 mm) centers. The FE package offers a three-layer rectangular chip carrier with dimensions 0.450 × 0.550 × 0.100 (11,43 × 13,97 × 2,54 mm).

ADVANCE INFORMATION
MILITARY PRODUCTS (SMJ) ONLY

This document contains information on a new product. Specifications are subject to change without notice.

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Since this EPROM operates from a single +5-V supply (in the read mode), it is ideal for use in microprocessor systems. One other supply (+25 V) is needed for programming. Programming requires a single TTL-level pulse per location. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

The '2564 is compatible with other 5-volt ROMs and EPROMs, including those in a 24-pin package.

operation

FUNCTION (PINS)	MODE								
	Read	Output Disable			Power Down	Start Programming	Inhibit Programming		
PD/$\overline{PGM}$ (22)	V_{IL}	V_{IH}	X	X	V_{IH}	Pulsed V_{IH} to V_{IL}	V_{IH}	X	X
$\overline{S}1$ (2)	V_{IL}	X	V_{IH}	X	X	V_{IL}	X	V_{IH}	X
$\overline{S}2$ (27)	V_{IL}	X	X	V_{IH}	X	V_{IL}	X	X	V_{IH}
V_{PP} (1)	+5 V		+5 V		+5 V	+25 V	+25 V		
V_{CC}† (26/28)	+5 V	+5 V			+5 V	+5 V	+5 V		
Q (11 to 13, 15 to 19)	Q	HI-Z			HI-Z	D	HI-Z		

X = Don't care.
†Do not use the internal jumper of 26-28 to conduct PC board currents.

read/output disable

When the outputs of two or more '2564's are paralled on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the '2564, the low-level signal is applied to the PD/$\overline{PGM}$ and $\overline{S}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8.

power down

Active power dissipation can be cut by over 68% by applying a high TTL signal to the PD/$\overline{PGM}$ pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the '2564 is erased by exposing the chip through the transparent lid to high intensity ultra-violet light having a wavelength of 253.7 nm (2537 angstroms). The recommended minimum exposure dose (UV intensity X exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in about 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore when using the '2564, the window should be covered with an opaque label.

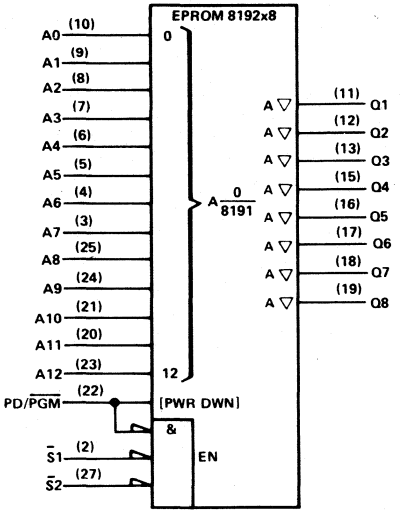
start programming

After erasure (all bits in logic high state), logic "0's" are programmed into the desired locations. A low can be erased only by ultraviolet light. The programming mode is achieved when Vpp is 25 V. Data is presented in parallel (8 bits) on pins Q1 to Q8. Once addresses and data are stable, a 10-millisecond low TTL pulse should be applied to the $\overline{PGM}$ pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. More than one '2564 can be programmed when the devices are connected in parallel. During programming, both chip select signals should be held low unless program inhibit is desired.

inhibit programming

When two or more '2564's are connected in parallel, data can be programmed into all devices or only chosen devices. '2564's not intended to be programmed should have a high level applied to PD/$\overline{PGM}$ or $\overline{S}1$ or $\overline{S}2$.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions in IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} (see note 1)	−0.3 V to 7 V
Supply voltage, V_{PP} (see note 1)	−0.3 V to 28 V
All input voltages (see Note 1)	−0.3 V to 7 V
Output voltage (operating with respect to V_{SS})	−0.3 V to 7 V
Operating free-air temperature range: TMS2564	0°C to 70°C
Operating case temperature range: SMJ2564	−55°C to 125°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "Absolute maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{SS} (substrate).

recommended operating conditions

PARAMETER	TMS2564-35			TMS2564-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH}	2.2		$V_{CC}+1$	2.2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.1†		0.8	−0.1†		0.8	V
Read cycle time, $t_{c(rd)}$	350			450			ns
Operating free-air temperature, T_A	0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied so that the device is not damaged.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (± 1 V).

† The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels and time intervals.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS2564			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V			±10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = MAX, PD/$\overline{PGM}$ = V_{IL}			18	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/$\overline{PGM}$ = V_{IL}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/$\overline{PGM}$ = V_{IH}		25	35	mA
I_{CC2}	V_{CC} supply current (active)	PD/$\overline{PGM}$ = V_{IL}		80	160	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended voltage and operating free-air temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TMS2564		UNIT
			TYP‡	MAX	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† This parameter is tested on sample basis only.
‡ Typical values are T_A = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	TMS2564-35		TMS2564-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 54/74 TTL Load, $t_r \leq 20$ ns, $t_f \leq 20$ ns, See Figure 1		350		450	ns
$t_{a(S)}$	Access time from $\overline{S1}$ and $\overline{S2}$ (whichever occurs last)			120		120	ns
$t_{a(PR)}$	Access time from PD/$\overline{PGM}$			350		450	ns
$t_{v(A)}$	Output data valid after address change		0		0		ns
$t_{dis(S)}$	Output disable time from chip select during read only (whichever occurs last)‡		0	100	0	100	ns
$t_{dis(PR)}$	Output disable time from PD/$\overline{PGM}$ during standby‡		0	100	0	100	ns

† All typical values are at T_A = 25°C and nominal voltages.
‡ Value calculated from 0.5 volt delta to measured output level.

recommended timing requirements for programming T_A = 25°C (see Note 4)

PARAMETER		TMS2564			UNIT
		MIN	TYP†	MAX	
$t_{w(PR)}$	Pulse duration, program pulse	9		55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(PR)}$	Program pulse hold time	0			ns
$t_{h(VPP)}$	V_{PP} hold time	2			μs

† Typical values are at nominal voltages.

NOTES: 4. Timing measurement reference levels: inputs 0.8 V and 2.2 V, outputs 0.65 V and 2.2 V, and V_{PP} during programming = 25 V ± 1 V.
5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$, $t_{a(S)}$, and t_{dis}, PD/$\overline{PGM}$ = V_{IL}.

recommended operating conditions

PARAMETER	SMJ2564			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.5	5	5.5	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}		V
Supply voltage, V_{SS}		0		V
High level input voltage, V_{IH}	2.2		$V_{CC}+1$	V
Low level input voltage, V_{IL}	−0.1†		0.8	V
Read cycle time, $t_{c(rd)}$	450			ns
Operating case temperature, T_C	−55		125	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied so that the device is not damaged.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (± 1 V).

† The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels and time intervals.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	SMJ2564			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.5 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V			±10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = MAX, PD/$\overline{PGM}$ = V_{IL}			18	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/$\overline{PGM}$ = V_{IL}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/$\overline{PGM}$ = V_{IH}		25	40	mA
I_{CC2}	V_{CC} supply current (active)	PD/$\overline{PGM}$ = V_{IL}		80	160	mA

† Typical values are at T_C = 25°C and nominal voltages.

capacitance over recommended voltage and case temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	SMJ2564		UNIT
			TYP‡	MAX	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† This parameter is tested on sample basis only.

‡ Typical values are T_C = 25°C and nominal voltages.

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	SMJ2564 MIN	SMJ2564 MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 54/74 TTL Load, $t_r \leq 20$ ns, $t_f \leq 20$ ns, See Figure 1		450	ns
$t_{a(S)}$	Access time from $\overline{S1}$ and $\overline{S2}$ (whichever occurs last)			150	ns
$t_{a(PR)}$	Access time from PD/$\overline{PGM}$			450	ns
$t_{v(A)}$	Output data valid after address change		0		ns
$t_{dis(S)}$	Output disable time from chip select during read only (whichever occurs last)‡		0	100	ns
$t_{dis(PR)}$	Output disable time from PD/$\overline{PGM}$ during standby‡		0	100	ns

† All typical values are at T_C = 25°C and nominal voltages.

‡ Value calculated from 0.5 volt delta to measured output level.

recommended timing requirements for programming T_C = 25°C (see Note 4)

PARAMETER		SMJ2564 MIN	SMJ2564 TYP†	SMJ2564 MAX	UNIT
$t_{w(PR)}$	Pulse duration, program pulse	9		55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(PR)}$	Program pulse hold time	0			ns
$t_{h(VPP)}$	V_{PP} hold time	2			μs

† Typical values are at nominal voltages.

NOTES: 4. Timing measurement reference levels: inputs 0.8 V and 2.2 V, outputs 0.65 V and 2.2 V, and V_{PP} during programming = 25 V ± 1 V.
5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$, $t_{a(S)}$, and t_{dis}, PD/$\overline{PGM}$ = V_{IL}.

PARAMETER MEASUREMENT INFORMATION

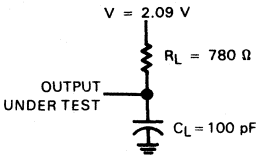
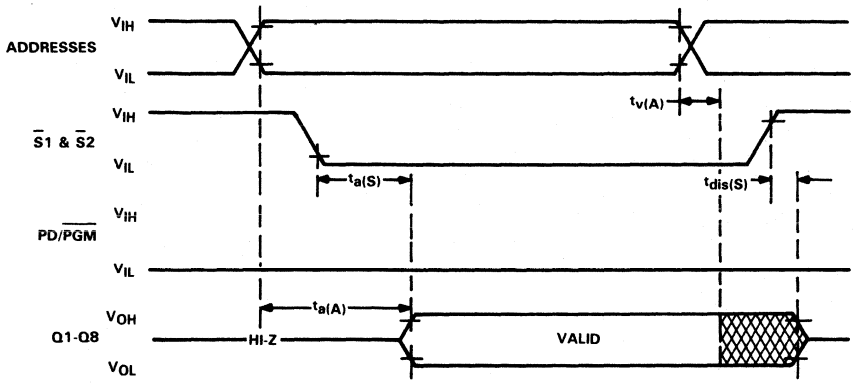
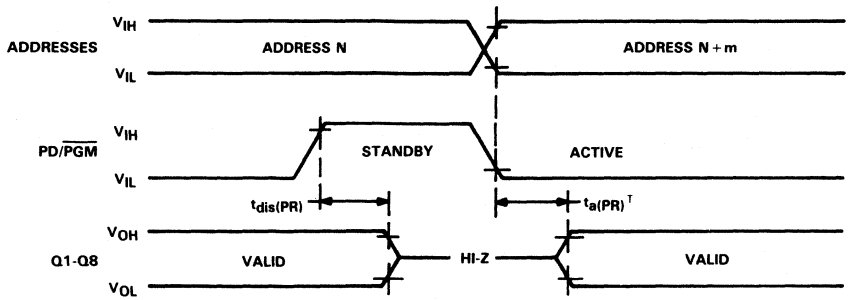


FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing

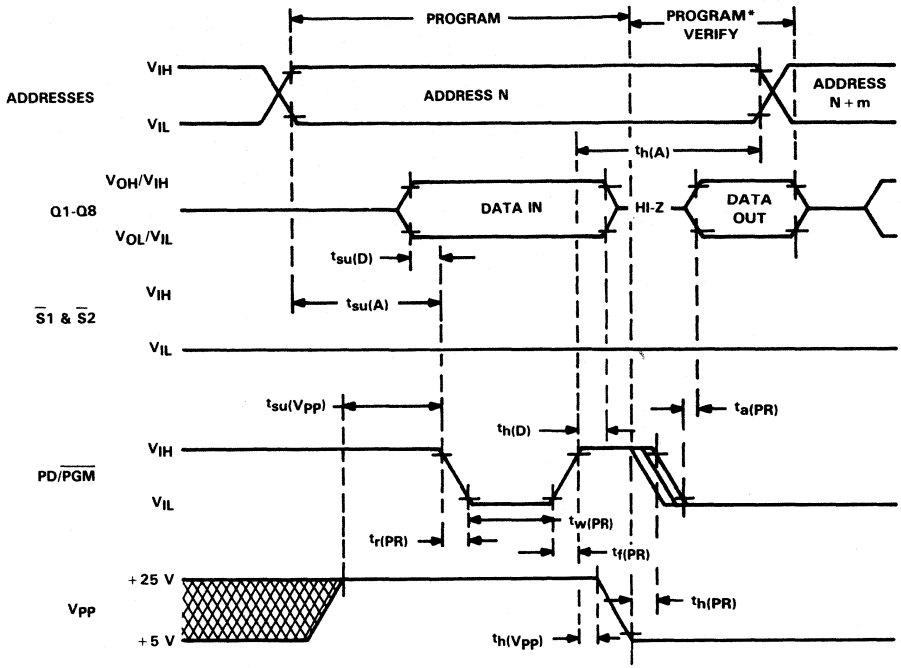


standby mode



†$t_{a(PR)}$ referenced to PD/$\overline{PGM}$ or the address, whichever occurs last.
$\overline{S1}$ and $\overline{S2}$ in Don't Care State in Standby Mode.

program cycle timing



*Equivalent to read mode.

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS2708, TMS27L08, SMJ2708, SMJ27L08
1024-WORD BY 8-BIT
ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

DECEMBER 1979 – REVISED AUGUST 1983

- 1024 X 8 Organization
- All Inputs and Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time

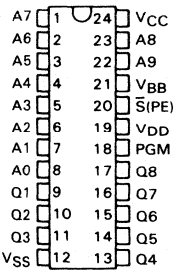
'2708-35	350 ns
'2708-45	450 ns
'27L08-45	450 ns

- 3-State Outputs for OR-Ties
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor-Based Systems
- Power Dissipation

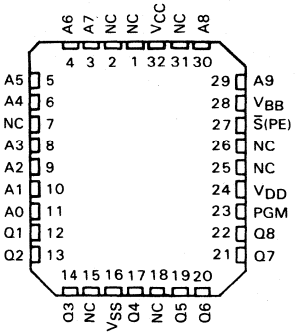
'27L08	580 mW Max Active
'2708	800 mW Max Active

- 10% Power Supply Tolerance (TMS27L08-45 and all SMJ' versions)
- Plug-Compatible Pin-Outs Allowing Interchangeability/Upgrade to 16K With Minimum Board Change
- Available in Full Military Temperature Range Versions (SMJ2708)

TMS2708 . . . JL PACKAGE
SMJ2708 . . . J PACKAGE
(TOP VIEW)



SMJ2708 . . . FE PACKAGE
(TOP VIEW)



NC – No Connection

description

The '2708-35, '2708-45, and '27L08-45 are ultraviolet light-erasable, electrically programmable read-only memories. They have 8,192 bits organized as 1024 words of 8-bit length. The devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54/74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 54/74 or 54LS/74LS TTL circuit without external resistors. The '27L08 guarantees 200 mV dc noise immunity in the high state and 250 mV in the low state. The data outputs for the '2708-35, '2708-45, and '27L08-45 are three-state for OR-tying multiple devices on a common bus.

PIN NOMENCLATURE	
A0-A7	Address Inputs
NC	No Connection
PGM	Program
Q1-Q8	Data Out
$\overline{S}$(PE)	Chip Select/Program Enable
V_{BB}	−5-V Power Supply
V_{CC}	+5-V Power Supply
V_{DD}	+12-V Power Supply
V_{SS}	0-V Ground

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These EPROMs are designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. The TMS' Series is supplied in a 24-pin dual-in-line ceramic cerdip (JL suffix) package designed for insertion in mounting-hole rows on 600-mil (15.2 mm) centers. They are designed for operation from 0°C to 70°C.

The SMJ' Series is offered in a 24-pin dual-in-line ceramic package (J) and also in a 32-pin leadless ceramic chip carrier (FE). The J package is designed for insertion in mounting-hole rows on 600-mil (15.2 mm) centers whereas the FE package is intended for surface mounting on solder pads on 0.05-inch (1.27 mm) centers. The FE package is a three-layer 32-pad rectangular chip carrier with dimensions of 0.450 × 0.550 × 0.100 inches (11.43 × 13.97 × 2.54 mm). This series is designed for operation from −55°C to 125°C.

operation (read mode)

address (A0-A9)

The address-valid interval determines the device cycle time. The 10-bit positive-logic address is decoded on-chip to select one of the 1024 words of 8-bit length in the memory array. A0 is the least-significant bit and A9 is the most-significant bit of the word address.

chip select, program enable [$\overline{S}$ (PE)]

When the chip select is low, all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high, all eight outputs are in a high-impedance state.

data out (Q1-Q8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

program

The program pin must be held below V_{CC} in the read mode.

operation (program mode)

erase

Before programming, the '2708-35, '2708-45, or '27L08-45 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light that has a wavelength of 253.7 nanometers (2537 Angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are in the high state.

programming

Programming consists of successively depositing a small amount of charge to a selected memory cell that is to be changed from the erased high state to the low state. A low can be changed to a high only by erasure. Programming is normally accomplished on a PROM or EPROM Programmer, an example of which is TI's Universal PROM Programming Module in conjunction with the 990 prototyping system. Programming must be done at room temperature (25°C) only.

to start programming (see program cycle timing diagram)

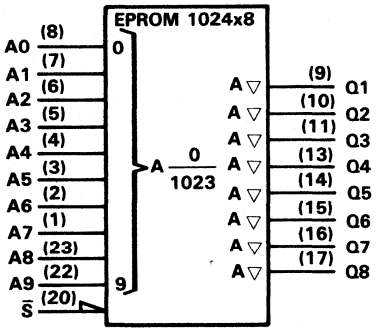
First bring the $\overline{S}$ (PE) pin to +12 V to disable the outputs and convert them to inputs. This pin is held high for the duration of the programming sequence. The first word to be programmed is addressed (it is customary to begin with the "0" address) and the data to be stored is placed on the Q1-Q8 program inputs. Then a +25 V program pulse is applied to the program pin. After 0.1 to 1.0 milliseconds the program pin is brought back to 0 V. After at least one microsecond the word address is sequentially changed to the next location, the new data is set up and the program pulse is applied.

Programming continues in this manner until all words have been programmed. This constitutes one of N program loops. The entire sequence is then repeated N times with $N \times t_{W(PR)} \geq 100$ ms. Thus, if $t_{W(PR)} = 1$ ms; then N = 100, the minimum number of program loops required to program the EPROM.

to stop programming

After cycling through the N program loops, the last program pulse is brought to 0 V, then Program Enable [$\overline{S}$ (PE)] is brought to V_{IL} which takes the device out of the program mode. The data supplied by the programmer must be removed before the address is changed since the program inputs are now data outputs and change of address could cause a voltage conflict on the output buffer. Q1-Q8 outputs are invalid up to 10 microseconds after the program enable pin is brought from $V_{IH(PE)}$ to V_{IL}.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions in IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{BB} (see Note 1)	−0.3 V to 7 V
Supply voltage, V_{CC} (see Note 1)	−0.3 V to 15 V
Supply voltage, V_{DD} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 V to 15 V
All input voltage (except program) (see Note 1)	−0.3 V to 20 V
Program input (see Note 1)	−0.3 V to 35 V
Output voltage (operating, with respect to V_{SS})	−2 V to 7 V
Operating free-air temperature range: TMS'	0°C to 70°C
Operating case temperature range: SMJ'	−65°C to 150°C
Storage temperature range	−55°C to 125°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage. V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	TMS2708-35 TMS2708-45			TMS27L08-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{BB}	−4.75	−5	−5.25	−4.5	−5	−5.5	V
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
Supply voltage, V_{DD}	11.4	12	12.6	10.8	12	13.2	V
Supply voltage V_{SS}		0			0		V
High-level input voltage, V_{IH} (except program and program enable)	2.4		$V_{CC}+1$	2.2		$V_{CC}+1$	
High-level program enable input voltage, $V_{IH(PE)}$	11.4	12	12.6	10.8	12	13.2	V
High-level program input voltage, $V_{IH(PR)}$	25	26	27	25	26	27	V
Low-level input voltage, V_{IL} (except program)	V_{SS}		0.65	V_{SS}		0.65	V
Low-level program input voltage, $V_{IL(PR)}$ Note: $V_{IL(PR)}$ max ≤ $V_{IH(PR)}$ −25 V	V_{SS}		1	V_{SS}		1	V
High-level program pulse input current (sink), $I_{IH(PR)}$			40			40	mA
Low-level program pulse input current (source), $I_{IL(PR)}$			3			3	mA
Operating free-air temperature, T_A	0		70	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS2708-35 TMS2708-45			TMS27L08-45			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −100 μA	3.7			3.7			V
		I_{OH} = −1 mA	2.4			2.4			
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.45			0.40	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		1	10		1	10	μA
I_O	Output current (leakage)	$\overline{S}$ (PE) = 5 V, V_O = 0.4 V to 5.25 V		1	10		1	10	μA
I_{BB}	Supply current from V_{BB}	All inputs high, $\overline{S}$ (PE) = 5 V, T_A = °C (worst case)		30	45		9	18	mA
I_{CC}	Supply current from V_{CC}			6	10		0.9	6	mA
I_{DD}	Supply current from V_{DD}			50	65		20	34	mA
$P_{D(AV)}$	Power Dissipation	T_A = 70°C			800			350	mW
		T_A = 0°C, $\overline{S}$ = 0 V					245	475	
		T_A = 0°C, $\overline{S}$ = +5 V					290	580	

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz†

PARAMETER		TMS'		UNIT
		TYP‡	MAX	
C_i	Input capacitance	4	6	pF
C_o	Output capacitance	8	12	pF

†This parameter is tested on sample basis only.
‡All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS2708-35		TMS2708 TMS27L08		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from Address	C_L = 100 pF 1 Series 54/74 TTL load $t_{f(S)}$, $t_{f(A)}$ = 20 ns		350		450	ns
$t_{a(S)}$	Access time from $\overline{S}$			120		120	ns
$t_{v(A)}$	Output data valid after address change		0		0		ns
t_{dis}	Output disable time†		0	120	0	120	ns
$t_{c(rd)}$	Read cycle time		350		450		ns

†Value calculated from 0.5 volt delta to measured output level.

recommended timing requirements for programming T_A = 25°C

PARAMETER		TMS'		UNIT
		MIN	MAX	
$t_{w(PR)}$	Pulse duration, program pulse	0.1	1	ms
t_t	Transition times (except program pulse)		20	ns
$t_{t(PR)}$	Transition times, program pulse	50	2000	ns
$t_{su(A)}$	Address setup time	10		μs
$t_{su(D)}$	Data setup time	10		μs
$t_{su(PE)}$	Program enable setup time	10		μs
$t_{h(A)}$	Address hold time	1000		ns
$t_{h(DA)}$	Address hold time after program input data stopped	0		ns
$t_{h(D)}$	Data hold time	1000		ns
$t_{h(PE)}$	Program enable hold time	500		ns
t_{SLAX}	Delay time, $\overline{S}$(PE) low to address change	0		ns

recommended operating conditions

PARAMETER	SMJ2708-35 SMJ2708-45			SMJ27L08-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{BB}	−4.75	−5	−5.25	−4.5	−5	−5.5	V
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
Supply voltage, V_{DD}	11.4	12	12.6	10.8	12	13.2	V
Supply voltage V_{SS}		0			0		V
High-level input voltage, V_{IH} (except program and program enable	2.4		$V_{CC}+1$	2.2		$V_{CC}+1$	
High-level program enable input voltage, $V_{IH(PE)}$	11.4	12	12.6	10.8	12	13.2	V
High-level program input voltage, $V_{IH(PR)}$	25	26	27	25	26	27	V
Low-level input voltage, V_{IL} (except program)	V_{SS}		0.65	V_{SS}		0.65	V
Low-level program input voltage, $V_{IL(PR)}$ Note: $V_{IL(PR)}$ max ≤ $V_{IH(PR)}$ − 25 V	V_{SS}		1	V_{SS}		1	V
High-level program pulsle input current (sink), $I_{IH(PR)}$			40			40	mA
Low-level program pulse input current (source), $I_{IL(PR)}$			3			3	mA
Operating case temperature, T_C	−55		125	−55		125	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SMJ2708-35 SMJ2708-45			SMJ27L08-45			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −100 μA	3.7			3.7			V
		I_{OH} = −1 mA	2.4			2.4			
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.45			0.40	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		1	10		1	10	μA
I_O	Output current (leakage)	$\overline{S}$ (PE) = 5 V, V_O = 0.4 V to 5.5 V		1	10		1	10	μA
I_{BB}	Supply current from V_{BB}	All inputs high, $\overline{S}$ (PE) = 5 V,		30	45		9	18	mA
I_{CC}	Supply current from V_{CC}			6	10		0.9	6	mA
I_{DD}	Supply current from V_{DD}			50	65		20	34	mA

capacitance over recommended supply voltage range and operating case temperature range, f = 1 MHz†

PARAMETER		SMJ'		UNIT
		TYP‡	MAX	
C_i	Input capacitance	4	6	pF
C_o	Output capacitance	8	12	pF

†This parameter is tested on sample basis only.

‡All typical values are at T_C = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating case temperature range

PARAMETER		TEST CONDITIONS	SMJ2708-35		SMJ2708 SMJ27L08		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from Address	C_L = 100 pF, 1 Series 54/74 TTL load, $t_{f(S)}$, $t_{f(A)}$ = 20 ns		350		450	ns
$t_{a(S)}$	Access time from $\overline{S}$			120		120	ns
$t_{v(A)}$	Output data valid after address change		0		0		ns
t_{dis}	Output disable time†		0	120	0	120	ns
$t_{c(rd)}$	Read cycle time		350		450		ns

†Value calculated from 0.5 volt delta to measured output level.

recommended timing requirements for programming T_C = 25°C

PARAMETER		SMJ'		UNIT
		MIN	MAX	
$t_{w(PR)}$	Pulse duration, program pulse	0.1	1	ms
t_t	Transition times (except program pulse)		20	ns
$t_{t(PR)}$	Transition times, program pulse	50	2000	ns
$t_{su(A)}$	Address setup time	10		μs
$t_{su(D)}$	Data setup time	10		μs
$t_{su(PE)}$	Program enable setup time	10		μs
$t_{h(A)}$	Address hold time	1000		ns
$t_{h(DA)}$	Address hold time after program input data stopped	0		ns
$t_{h(D)}$	Data hold time	1000		ns
$t_{h(PE)}$	Program enable hold time	500		ns
t_{SLAX}	Delay time, $\overline{S}$(PE) low to address change	0		ns

PARAMETER MEASUREMENT INFORMATION

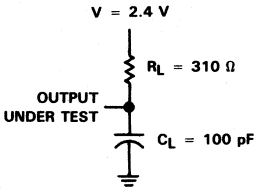
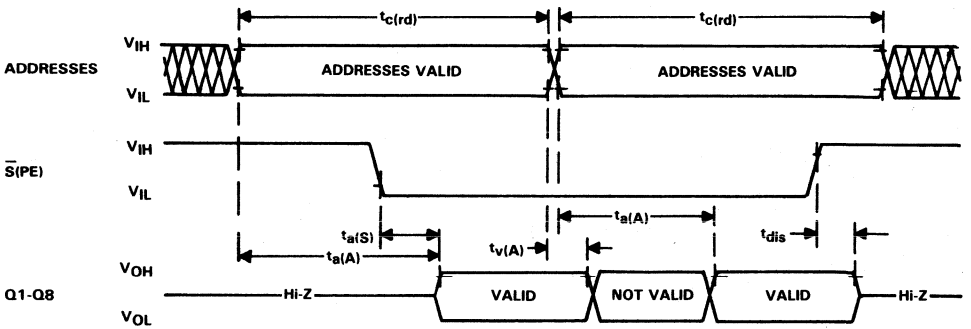
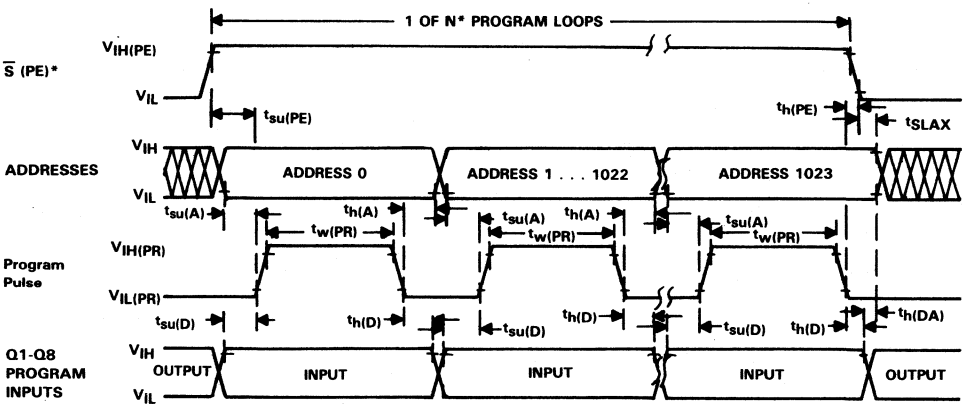


FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing

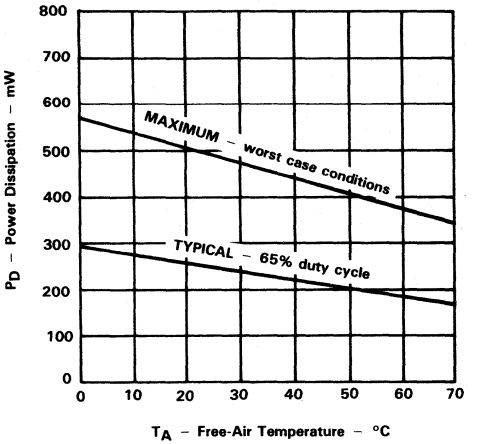


*$\overline{S}$ (PE) is at +12 V through N program loops where N < 100 ms/tw (PR).
NOTE: Q1-Q8 outputs are invalid up to 10 μsec after programming $\overline{S}$ (PE) goes low).

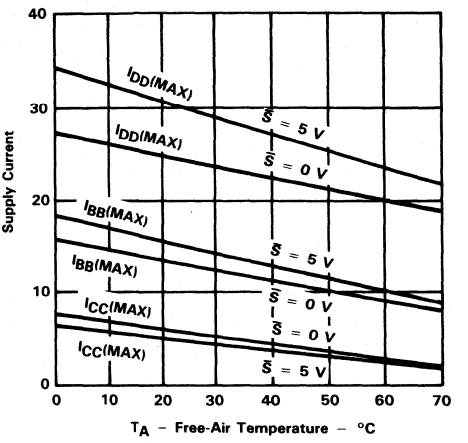
All timing reference points in this data sheet (inputs and outputs) are 90% points.

TYPICAL '27L08-45 CHARACTERISTICS

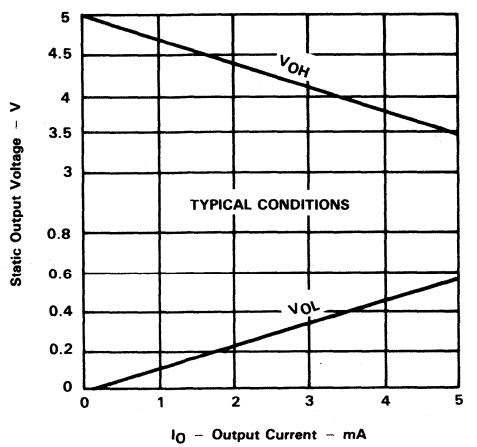
DEVICE POWER DISSIPATION vs TEMPERATURE



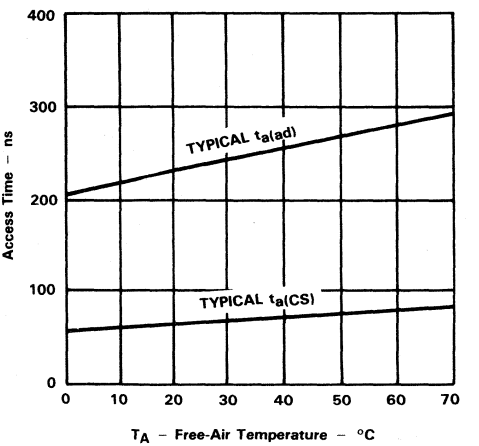
CURRENT vs TEMPERATURE



STATIC OUTPUT VOLTAGE vs OUTPUT CURRENT



ACCESS TIME vs TEMPERATURE



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS2716
2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

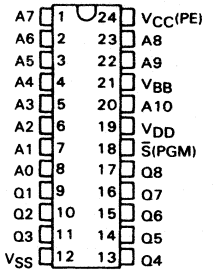
DECEMBER 1979 – REVISED OCTOBER 1983

- **2048 X 8 Organization**
- **All Inputs and Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Performance Ranges:**

	ACCESS TIME (MAX)	CYCLE TIME (MIN)
TMS2716-30	300 ns	300 ns
TMS2716-45	450 ns	450 ns

- **3-State Outputs for OR-Ties**
- **N-Channel Silicon-Gate Technology**
- **8-Bit Output for Use in Microprocessor-Based Systems**
- **Low Power . . . 315 mW (Typical)**

TMS2716 . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A10	Addresses
Q1-Q8	Data Out
$\overline{S}$(PGM)	Chip Select (Program)
V_{BB}	−5-V Supply
V_{CC}(PE)	+5-V Supply (Program Enable)
V_{DD}	+12-V Supply
V_{SS}	0 V Ground

description

The TMS2716 is an ultra-violet light-erasable, electrically programmable read-only memory. It has 16,384 bits organized as 2048 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 circuits without the use of external pull-up resistors and each output can drive one Series 74 or 74LS TTL circuit without external resistors. The TMS2716 guarantees 250 mV dc noise immunity in the low state. Data outputs are three-state for OR-tying multiple devices on a common bus. The TMS2716 is plug-in compatible with the TMS2708 and the TMS27L08. Pin compatible mask programmed ROMs are available for large volume requirements.

This EPROM is designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. It is supplied in a 24-pin dual-in-line cerpak (JL suffix) package designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers. It is designed for operation from 0°C to 70°C.

operation (read mode)

address (A0-A10)

The address-valid interval determines the device cycle time. The 11-bit positive-logic address is decoded on-chip to select one of 2048 words of 8-bit length in the memory array. A0 is the least-significant bit and A10 most-significant bit of the word address.

chip select, program [$\overline{S}$ (PGM)]

When the chip select is low, all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high, all eight outputs are in a high-impedance state.

program

In the program mode, the chip select feature does not function as pin 18 inputs only the program pulse. The program mode is selected by the V_{CC}(PE) pin. Either 0 V or +12 V on this pin will cause the TMS2716 to assume program cycle.

data out (Q1-Q8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

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operation (program mode)

erase

Before programming, the TMS2716 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity × exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state.

programming

Programming consists of successively depositing a small amount of charge to a selected memory cell that is to be changed from the erased high state to the low state. A low can be changed to a high only by erasure. Programming be normally accomplished on a PROM or EPROM Programmer, an example of which is TI's Universal PROM Programming Module in conjunction with the 990 prototyping system. Programming must be done at room temperature (25°C) only.

to start programming (see program cycle timing diagram)

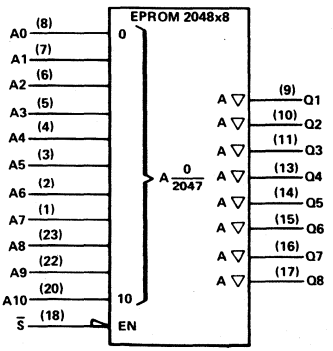
First bring the V_{CC}(PE) pin to +12 V or 0 V to disable the outputs and convert them to inputs. This pin is held high for the duration of the programming sequence. The first word to be programmed is addressed (it is customary to begin with the "0" address) and the data to be stored is placed on the Q1-Q8 program inputs. Then a +26 V program pulse is applied to the program pin. After 0.1 to 1.0 milliseconds the program pin is brought back to 0 V. After at least one microsecond the word address is sequentially changed to the next location, the new data is set up and the program pulse is applied.

Programming continues in this manner until all words have been programmed. This constitutes one of N program loops. The entire sequence is then repeated N times with $N \times t_{W(PR)} \geq 100$ ms. Thus, if $t_{W(PR)} = 1$ ms; then N = 100, the minimum number of program loops required to program the EPROM.

to stop programming

After cycling through the N program loops, the last program pulse is brought to 0 V, then Program Enable V_{CC}(PE) is brought back to ±5 volts which takes the device out of the program mode. The data supplied by the programmer must be removed before the address is changed since the program inputs are now data outputs and a change of address could cause a voltage conflict on the output buffer. Q1-Q8 outputs are invalid up to 10 microseconds after the program enable pin is brought from $V_{IH(PE)}$ to $V_{IL(PE)}$.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions in IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{BB} (see Note 1)	−0.3 V to 7 V
Supply voltage, V_{CC} (see Note 1)	−0.3 V to 15 V
Supply voltage, V_{DD} (see Note 1)	−0.3 V to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 V to 15 V
All input voltage (except program) (see Note 1)	−0.3 V to 20 V
Program input (see Note 1)	−0.3 V to 35 V
Output voltage (operating, with respect to V_{SS})	−2 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operating of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (except program and program enable)	2.4		$V_{CC}+1$	V
High-level program enable input voltage, $V_{IH(PE)}$	11.4	12	12.6	V
High-level program input voltage, $V_{IH(PR)}$	25	26	27	V
Low-level input voltage, V_{IL} (except program)	V_{SS}		0.65	V
Low-level program input voltage, $V_{IL(PR)}$ Note: $V_{IL(PR)}$ max ≤ $V_{IH(PR)}$ − 25 V	V_{SS}		1	V
High-level program pulse input current (sink), $I_{IH(PR)}$			40	mA
Low-level program pulse input current (source), $I_{IL(PR)}$			3	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 μA	3.7			V
		I_{OH} = −1 mA	2.4			
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.45	V
I_I	Input current (leakage)	V_{IL} = 0 V to 5.25 V		1	10	μA
I_O	Output current (leakage)	$\overline{S}$ (Program) = 5 V, V_O = 0.4 V to 5.25 V		1	10	μA
I_{BB}	Supply current from V_{BB}	All inputs high,		10	20	mA
I_{CC}	Supply current from V_{CC}	$\overline{S}$ (Program) = 5 V,		1	8	mA
I_{DD}	Supply current from V_{DD}	T_A = 0°C (worst case)		26	45	mA
I_{PE}	Supply current from PE on V_{CC} Pin	V_{PE} = V_{DD}		2	4	mA
$P_{D(AV)}$	Power Dissipation	T_A = 70°C			540	mW
		T_A = 0°C $\overline{S}$ = 0 V		315	595	
		T_A = 0°C $\overline{S}$ = +5 V		375	720	

† All typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
C_i	Input capacitance [except $\overline{S}$ (Program)]	4	6	pF
$C_{i(S)}$	$\overline{S}$ (Program) input capacitance	20	30	pF
C_o	Output capacitance	8	12	pF

† All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS2716-30		TMS2716-45		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL Load $t_{f(S)}$, $t_{f(A)}$ = 20 ns See Figure 1		300		450	ns
$t_{a(S)}$	Access time from $\overline{S}$			120		120	ns
$t_{v(A)}$	Output data valid after address change		0		0		ns
t_{dis}	Output disable time†		0	120	0	120	ns
$t_{c(rd)}$	Read cycle time		300		450		ns

† Value calculated from 0.5 volt delta to measured output level.

T_A = 25°C program characteristics over recommended supply voltage range

PARAMETER		MIN	MAX	UNIT
$t_{w(PR)}$	Pulse duration, program pulse	0.1	1	ms
t_t	Transition times (except program pulse)		20	ns
$t_{t(PR)}$	Transition times, program pulse	30	2000	ns
$t_{su(A)}$	Address setup time	10		μs
$t_{su(D)}$	Data setup time	10		μs
$t_{su(PE)}$	Program enable setup time	10		μs
$t_{h(A)}$	Address hold time	1000		ns
$t_{h(DA)}$	Address hold time after program input data stopped	0		ns
$t_{h(D)}$	Data hold time	1000		ns
$t_{h(PE)}$	Program enable hold time	500		ns
t_{SLAX}	Delay time, $\overline{S}$ (Program) low to address change	0		ns

PARAMETER MEASUREMENT INFORMATION

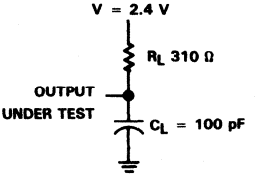
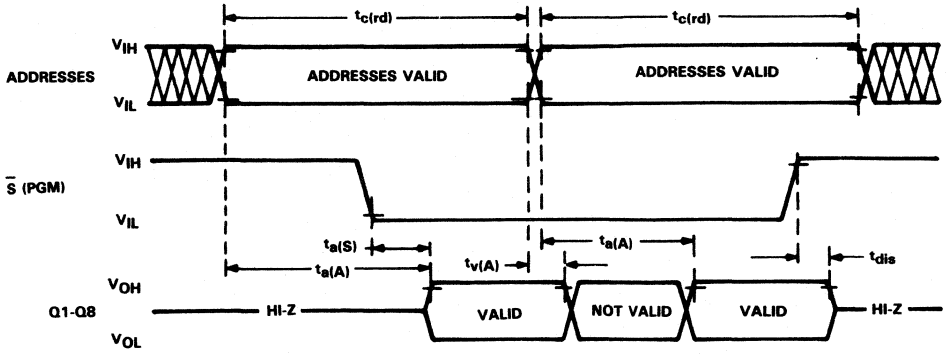
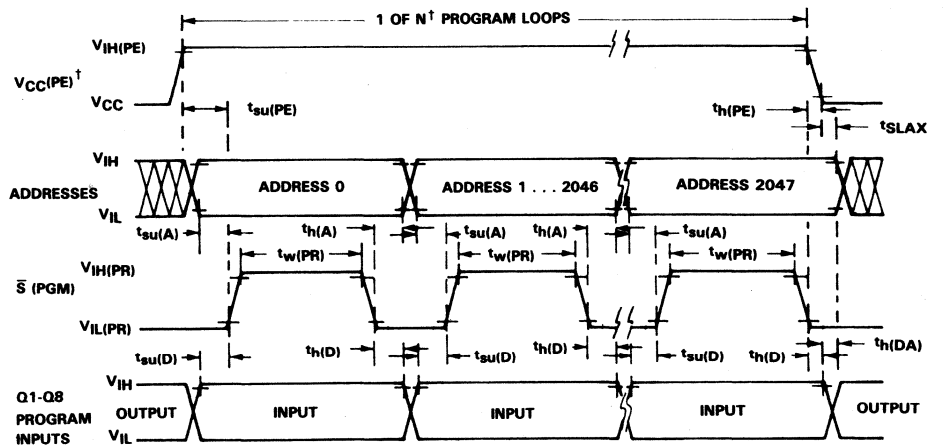


FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



program cycle timing



† $V_{CC(PE)}$ is at 0 V or +12 V through N program loops where N ≥ 100 ms/$t_{w(PR)}$.
NOTE: Q1-Q8 outputs are invalid up to 10 μs after programming ($V_{CC(PE)}$ goes low).

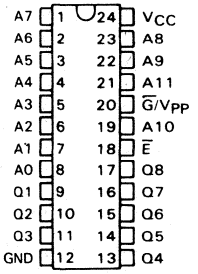
Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

- **Organization . . . 4096 X 8**
- **Single +5-V Power Supply**
- **All Inputs and Outputs Are TTL Compatible**
- **Performance Ranges:**

	ACCESS TIME (MAX)	CYCLE TIME (MIN)
TMS2732A-30	300 ns	300 ns
TMS2732A-35	350 ns	350 ns
TMS2732A-45	450 ns	450 ns

- **Low Standby Power Dissipation . . . 158 mW (Maximum)**
- **JEDEC Approved Pinout . . . Industry Standard**
- **21-V Power Supply Required for Programming**
- **N-Channel Silicon-Gate Technology**
- **8-Bit Output for Use in Microprocessor Based Systems**
- **Static Operation (No Clocks, No Refresh)**
- **Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or S(−55°C to 100°C) Temperature Ranges in the Future**

TMS2732A . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A11	Addresses
$\overline{E}$	Chip Enable
$\overline{G}$/VPP	Output Enable/+21 V
Q1 – Q8	Outputs
VCC	+5-V Power Supply

6

EPROM Devices

description

The TMS2732A is an ultraviolet light-erasable, electrically programmable read-only memory. It has 32,768 bits organized as 4,096 words of 8-bit length. The TMS2732A only requires a single 5-volt power supply with a tolerance of ±5%.

The TMS2732A provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in multibus microprocessor systems. The TMS2732A has a power-down mode that reduces maximum power dissipation from 657 mW to 158 mW when the device is placed on standby.

This EPROM is supplied in a 24-pin dual-in-line ceramic package and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMS2732A are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Deselect	Power Down (Standby)	Program	Program Verification	Inhibit Programming
$\overline{E}$ (18)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$/V_{PP} (20)	V_{IL}	V_{IH}	X	21 V	V_{IL}	21 V
V_{CC} (24)	5 V	5 V	5 V	5 V	5 V	5 V
Q1-Q8 (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IH} or V_{IL}

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read

The two control pins ($\overline{E}$ and $\overline{G}/V_{PP}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}/V_{PP}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum power dissipation from 657 mW to 158 mW. A TTL high-level signal applied to $\overline{E}$ selects the power down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}/V_{PP}$.

program

The programming procedure for the TMS2732A is the same as that for the TMS2532, except that in the program mode, $\overline{G}/V_{PP}$ is taken from a TTL low-level to 21 V.

The program mode consists of the following sequence of events. With the level on $\overline{G}/V_{PP}$ equal to 21 V; data to be programmed is applied in parallel to output pins Q8 – Q1. The location to be programmed is addressed. Once data and addresses are stable, a 10-millisecond TTL low-level pulse is applied to $\overline{E}$. The maximum width of this pulse is 55 milliseconds. The programming pulse must be applied at each location that is to be programmed. Locations may be programmed in any order.

Several TMS2732As can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program verify

After the EPROM has been programmed, the programmed bits should be verified. To verify bit states, $\overline{G}/V_{PP}$ and $\overline{E}$ are set to V_{IL}.

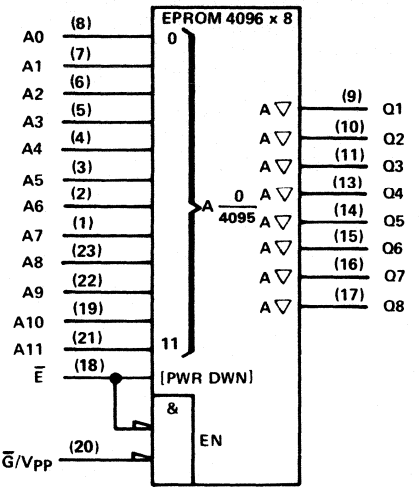
program inhibit

The program inhibit is useful when programming multiple TMS2732As connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ of the device that is not to be programmed.

erasure

The TMS2732A is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2732A, the window should be covered with an opaque label.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . −0.3 V to 7 V
Supply voltage, V_{PP} . . . . . −0.3 V to 22 V
All input voltage (except program) . . . . . −0.3 V to 7 V
Output voltage . . . . . −0.3 V to 7 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 125°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS2732A-30			TMS2732A-35			TMS2732A-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 2)		V_{CC}			V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0			0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	2		$V_{CC}+1$	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.1		0.8	−0.1		0.8	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$	300			350			450			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTES: 1. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
2. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 21 V (±0.5 V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 2.1$ mA			0.45	V
I_I	Input current (leakage)	$V_I = 0$ V to 5.25 V			±10	μA
I_O	Output current (leakage)	$V_O = 0.4$ V to 5.25 V			±10	μA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}, $\overline{G}$ at V_{IL}		20	30	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}		70	125	mA

†Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER			TEST CONDITIONS	MIN	TYP†	UNIT
C_i	Input capacitance	All except $\overline{G}/V_{PP}$	V_I = 0 V	4	6	pF
		$\overline{G}/V_{PP}$			20	
C_o	Output capacitance		V_O = 0 V		12	pF

†Typical values are at T_A = 25°C and nominal voltage.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS (See Note 3)	TMS2732A-30		TMS2732A-35		TMS2732A-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100pF, 1 Series 74 TTL Load, $t_r \le 20$ ns, $t_f \le 20$ ns, See Figure 1		300		350		450	ns
$t_{a(E)}$	Access time from $\overline{E}$			300		350		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			150		150		150	ns
$t_{dis(E)}$‡	Output disable time from $\overline{E}$			100		100		100	ns
$t_{dis(G)}$‡	Output disable time from $\overline{G}$			100		100		100	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first		0		0		0		ns

NOTE 3. Timing measurement reference levels: inputs 0.8 V and 2 V
outputs 0.8 V and 2 V.

‡Value calculated from 0.5 V delta to measured output level.

recommended conditions for programming, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{PP}	Supply voltage	20.5	21	21.5	V
V_{IH}	High-level input voltage	2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage	−0.1		0.8	V
$t_{w(E)}$	$\overline{E}$ pulse duration	9		55	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(VPP)}$	V_{PP} hold time	2			μs
$t_{rec(PG)}$	V_{PP} recovery time	2			μs
t_{EHD}	Delay time, data valid after $\overline{E}$ low			1	μs

programming characteristics, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage		−0.1		0.8	V
V_{OH}	High-level output voltage (verify)	$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low-level output voltage (verify)	$I_{OL} = 2.1$ mA			0.45	V
I_I	Input current (all inputs)	$V_I = V_{IL}$ or V_{IH}			10	μA
I_{PP}	Supply current	$\overline{E} = V_{IL}$, $\overline{G} = V_{PP}$			30	mA
I_{CC}	Supply current				125	mA
$t_{dis(PR)}$	Output disable time		0		100	ns

PARAMETER MEASUREMENT INFORMATION

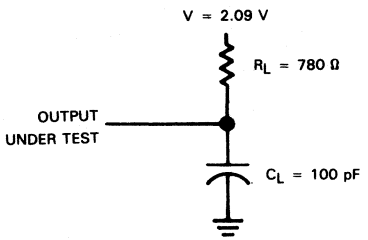
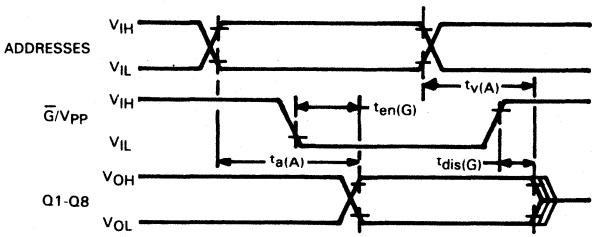
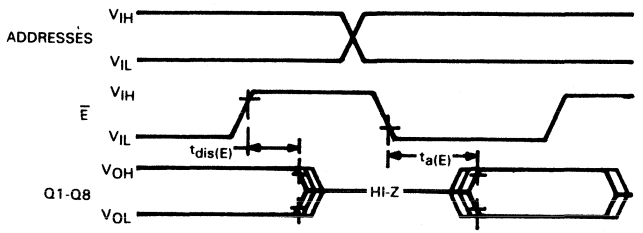


FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



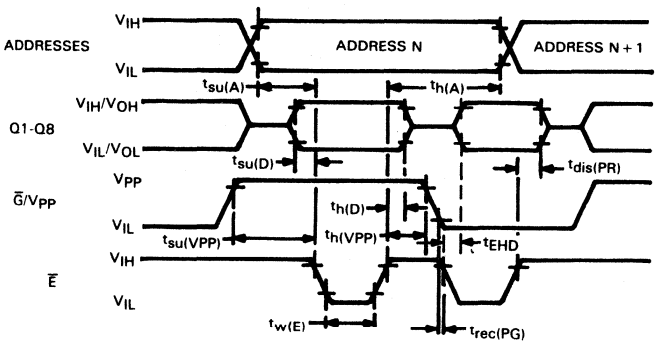
standby mode



6

EPROM Devices

program cycle timing



Timing measurement reference levels: Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V.

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS2764
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

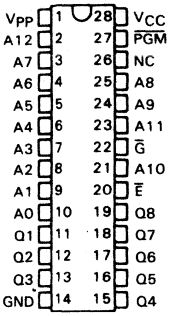
JULY 1983 – REVISED JANUARY 1984

- **Organization . . . 8192 X 8**
- **Single +5-V Power Supply**
- **Pin Compatible with TMS2732A EPROM**
- **All Inputs and Outputs are TTL Compatible**
- **Performance Ranges:**

	MAX ACCESS/ MIN CYCLE TIME
TMS2764-20	200 ns
TMS2764-25	250 ns
TMS2764-30	300 ns
TMS2764-35	350 ns
TMS2764-45	450 ns

- **Low Active Current . . . 100 mA (Max)**
- **JEDEC Approved Pinout**
- **21-V Power Supply Required for Programming**
- **Fast Programming Algorithm**
- **N-Channel Silicon-Gate Technology**
- **8-Bit Output for Use in Microprocessor-Based Systems**
- **Static Operation (No Clocks, No Refresh**
- **Available with MIL-STD-883B Processing and L(0°C to 70°C), E(−40°C to 85°C), or M(−55°C to 125°C) Temperature Ranges in the Future**

TMS2764 . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A12	Addresses
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
$\overline{PGM}$	Program
Q1-Q8	outputs
V_{CC}	+5-V Power Supply
V_{PP}	+21-V Power Supply

6 EPROM Devices

description

The TMS2764 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 65,536 bits organized as 8,192 words of 8-bit length. The TMS2764-20 only requires a single 5-volt power supply with a tolerance of ±5%, and has a maximum access time of 200 ns. This access time is compatible with high-performance microprocessors.

The TMS2764 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS2764 has a power-down mode that reduces maximum active current from 100 mA to 35 mA when the device is placed on standby.

This EPROM is supplied in a 28-pin, 600-mil dual-in-line ceramic package and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMS2764 are listed in the following table.

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	X
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IL} or V_{IH}

read

The dual control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip eanble ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 100 mA to 35 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

erasure

Before programming, the TMS2764 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 mW/cm^2 UV lamp will erase the device in approximately 20 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS2764, the window should be covered with an opaque label.

fast programming

Note that the application of a voltage in excess of 22 V to V_{PP} may damage the TMS2764.

After erasure, logic "0's" are programmed into the desired locations. Programming consists of the following sequence of events. With the level on V_{PP} equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied, if correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at V_{CC} = 6.0 V and V_{PP} = 21.0 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V. A flowchart of the fast programming routine is shown in Figure 1.

multiple device programming

Several TMS2764's can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS2764's connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

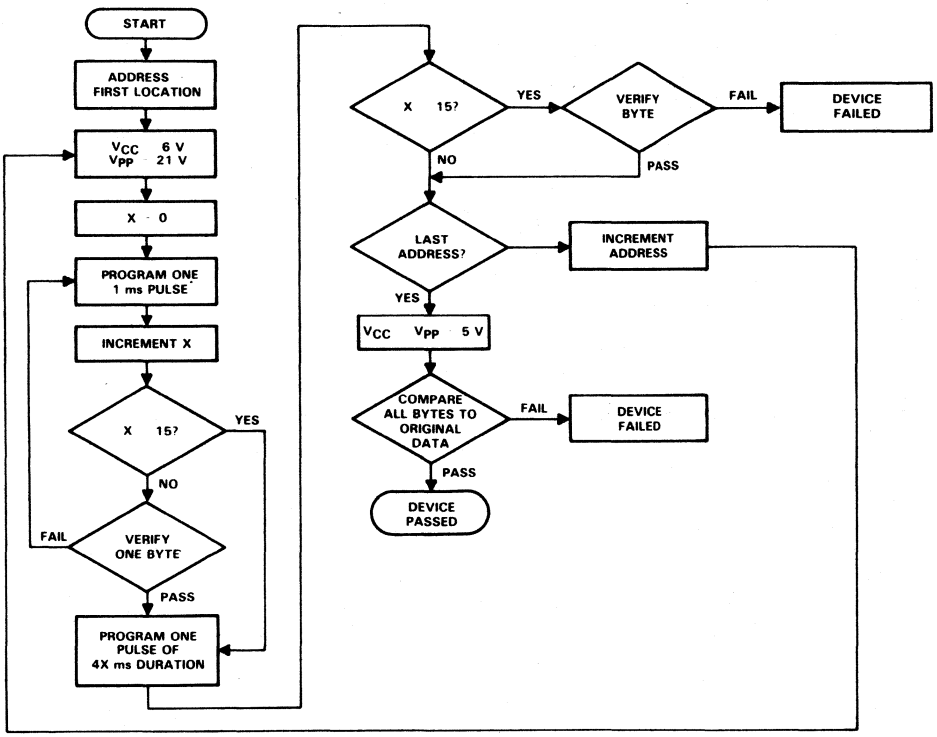
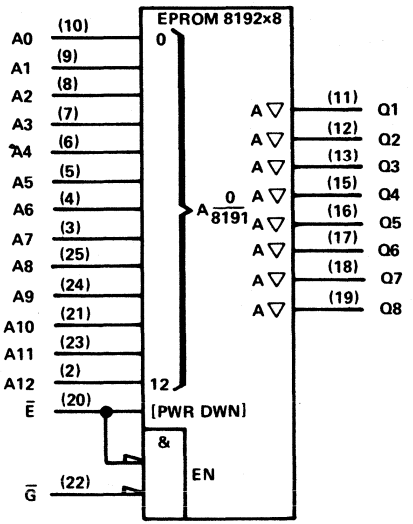


FIGURE 1 – FAST PROGRAMMING FLOWCHART

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.6 V to 7 V
Supply voltage, V_{PP}	−0.6 V to 22 V
All input voltage	−0.6 V to 7 V
Output voltage	−0.6 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS2764			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{PP}		V_{CC}		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL} (see Note 1)	−0.1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 1: The algebraic convention, where the more negative (less positive) limit is deisgnated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (load)	V_I = 0 V to 5.25 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V			±10	μA
I_{PP1}	V_{PP} supply current (read)	V_{PP} = 5.25 V			5	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{E}$ and $\overline{PGM}$ at V_{IL}			50	mA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}			35	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}			100	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V		4	6	pF
C_o	Output capacitance	V_O = 0 V		8	12	pF

† Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range, C_L = 100 pF, 1 Series 74 TTL load (see note 2 and figure 2)

PARAMETER		TMS2764-20		TMS2764-25		TMS2764-30		TMS2764-35		TMS2764-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		200		250		300		350		450	ns
$t_{a(\overline{E})}$	Access time frm $\overline{E}$		200		250		300		350		450	ns
$t_{en(\overline{G})}$	Output enable time from $\overline{G}$		75		100		120		150		150	ns
$t_{dis(\overline{G})}$‡	Output disable time from $\overline{G}$	0	60	0	85	0	105	0	130	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first	0		0		0		0		0		ns

NOTE 2: Fall all switching characteristics and timing measurements, input timing reference levels are 0.8 V and 2 V; output timing reference levels are 0.8 V and 2 V.

‡ Value calculated from 0.5 volt delta to measured output level; $t_{dis(G)}$ is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first. Refer to read cycle timing diagram.

recommended conditions for fast programming routine, T_A = 25°C (see note 2 and fast programming cycle timing diagram)

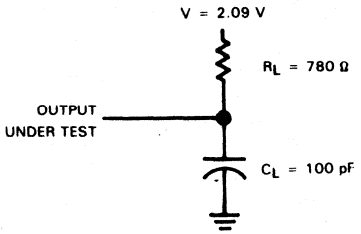
PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	5.75	6	6.25	V
V_{PP}	Supply voltage (see Note 4)	20.5	21	21.5	V
$t_{w(IPGM)}$	$\overline{PGM}$ initial program pulse duration (see Note 5)	0.95	1	1.05	ms
$t_{w(FPGM)}$	$\overline{PGM}$ final pulse duration (see Note 6)	3.8		63	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs

fast programming characteristics, T_A = 25°C (see note 2 and fast programming cycle timing diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{dis(G)FP}$	Output disable time from $\overline{G}$ (see Note 7)	C_L = 100 pF	0		130	ns
$t_{en(G)FP}$	Output enable time from $\overline{G}$	1 Series 74 TTL load			150	

NOTES:
2. For all switching characteristics and timing measurements, input timing reference levels are 0.8 V and 2 V; output timing reference levels are 0.8 V and 2 V.
3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
4. When programming the TMS2764, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.
5. The Initial program pulse duration tolerance is 1 ms ± 5%.
6. The length of the Final pulse will vary from 3.8 ms to 63 ms depending on the number of Initial pulse applications (X).
7. This parameter is only sampled and is not 100% tested.

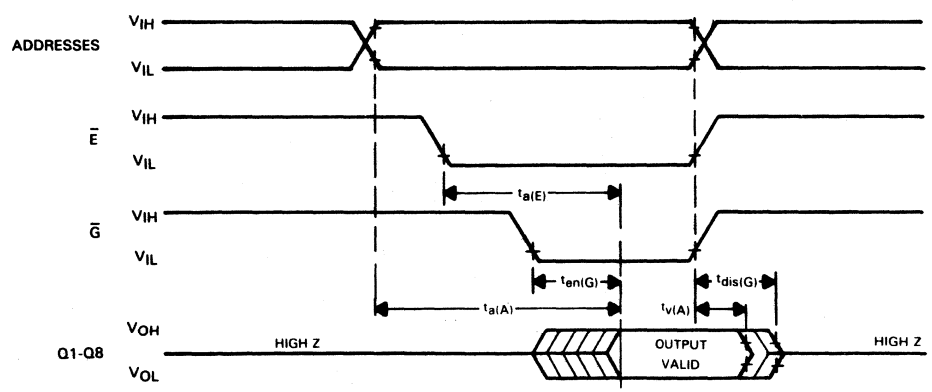
PARAMETER MEASUREMENT INFORMATION



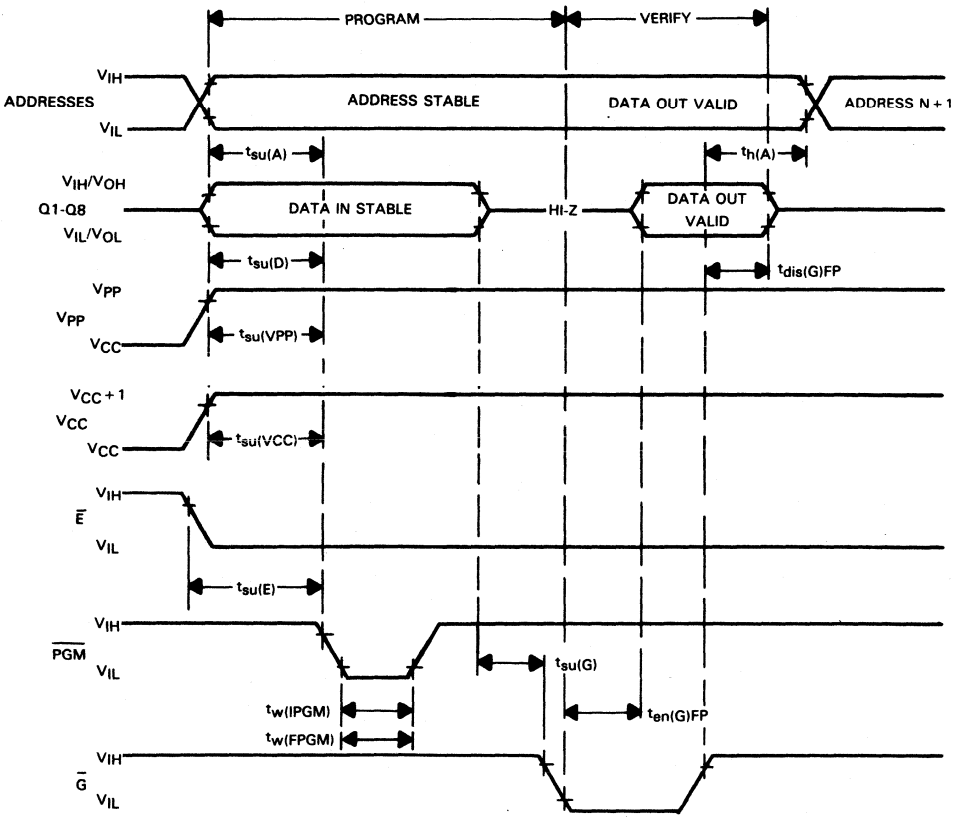
NOTE: $t_f \leq 20$ ns and $t_r \leq 20$ ns.

FIGURE 2 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



fast program cycle timing



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS27128
131,072-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

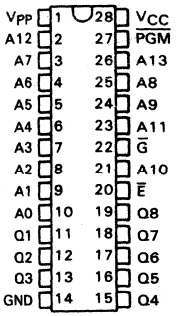
OCTOBER 1983 — REVISED JANUARY 1984

- **16,384 X 8 Organization**
- **Single +5-V Power Supply**
- **Pin Compatible with TMS2764 EPROM**
- **All Inputs and Outputs Are TTL Compatible**
- **Max Access/Min Cycle Time:**

TMS27128-25	250 ns
TMS27128-30	300 ns
TMS27128-45	450 ns

- **Low Active Current**
  – 100 mA (Maximum)
- **JEDEC Approved Pinout**
- **Fast Programming Algorithm**

TMS27128 . . . JL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A13	Addresses
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
$\overline{PGM}$	Program
Q1-Q8	Outputs
V_{CC}	+5-V Power Supply
V_{PP}	+21-V Power Supply

description

The TMS27128 is an ultraviolet light-erasable, electrically programmable read-only memory. It has 131,072 bits organized as 16,384 words of 8-bit length. The TMS27128 only requires a single 5-volt power supply. The TMS27128-25 provides an access time of 250 ns, which is compatible with high-speed microprocessors.

The TMS27128 provides two output control lines: Output Enable ($\overline{G}$) and Chip Enable/Power Down ($\overline{E}$). This feature allows the $\overline{G}$ control line to eliminate bus contention in microprocessor systems. The TMS27128 has a standby mode that reduces the maximum power dissipation from 525 mW to 210 mW when the device is placed on standby.

This EPROM is supplied in a 28-pin dual-in-line ceramic package (JL suffix). It is pin compatible with the TMS2764 EPROM and is designed for operation from 0°C to 70°C.

operation

The six modes of operation for the TMs27128 are listed in the following table.

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down (Standby)	Fast Programming	Program Verification	Inhibit Programming
$\overline{E}$ (20)	V_{IL}	X	V_{IH}	V_{IL}	V_{IL}	V_{IH}
$\overline{G}$ (22)	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X
$\overline{PGM}$ (27)	V_{IH}	V_{IH}	X	V_{IL}	V_{IH}	X
V_{PP} (1)	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	X
V_{CC} (28)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
Q1-Q8 (11 to 13, 15 to 19)	Q	HI-Z	HI-Z	D	Q	HI-Z

X = V_{IL} or V_{IH}

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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TEXAS INSTRUMENTS

read

The dual control pins ($\overline{E}$ and $\overline{G}$) must have low-level TTL signals in order to provide data at the outputs. Chip enable ($\overline{E}$) should be used for device selection. Output enable ($\overline{G}$) should be used to gate data to the output pins.

power down

The power-down mode reduces the maximum active current from 100 mA to 40 mA. A TTL high-level signal applied to $\overline{E}$ selects the power-down mode. In this mode, the outputs assume a high-impedance state, independent of $\overline{G}$.

erasure

Before programming, the TMS27128 is erased by exposing the chip to shortwave ultraviolet light that has a wavelength of 253.7 nanometers (2537 angstroms). The recommended minimum exposure dose (UV intensity × exposure time) is fifteen watt-seconds per square centimeter. A typical 12 mW/cm^2 UV lamp will erase the device in approximately 20 minutes. The lamp should be located about 2.5 centimeters (1 inch) above the chip during erasure. After erasure, all bits are at a high level. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27128, the window should be covered with an opaque label.

fast programming

Note that the application of a voltage in excess of 22 V to V_{PP} may damage the TMS27128.

After erasure, logic "0's" are programmed into the desired locations. Programming consists of the following sequence of events. With the level on V_{PP} equal to 21 V and $\overline{E}$ at TTL low, data to be programmed is applied in parallel to output pins Q8-Q1. The location to be programmed is addressed. Once data and addresses are stable, a TTL low-level pulse is applied to $\overline{PGM}$. Programming pulses must be applied at each location that is to be programmed. Locations may be programmed in any order.

Programming uses two types of programming pulse: Prime and Final. The length of the Prime pulse is 1 millisecond; this pulse is applied X times. After each application the byte being programmed is verified. If the correct data is read, the Final programming pulse is then applied, if correct data is not read, a further 1 millisecond programming pulse is applied up to a maximum X of 15. The Final programming pulse is 4X milliseconds long. This sequence of programming pulses and byte verification is done at V_{CC} = 6.0 V and V_{PP} = 21.0 V. When the full fast programming routine is complete, all bits are verified with V_{CC} = V_{PP} = 5 V. A flowchart of the fast programming routine is shown in Figure 1.

multiple device programming

Several TMS27128's can be programmed simultaneously by connecting them in parallel and following the programming sequence previously described.

program inhibit

The program inhibit is useful when programming multiple TMS27128's connected in parallel with different data. Program inhibit can be implemented by applying a high-level signal to $\overline{E}$ or $\overline{PGM}$ of the device that is not to be programmed.

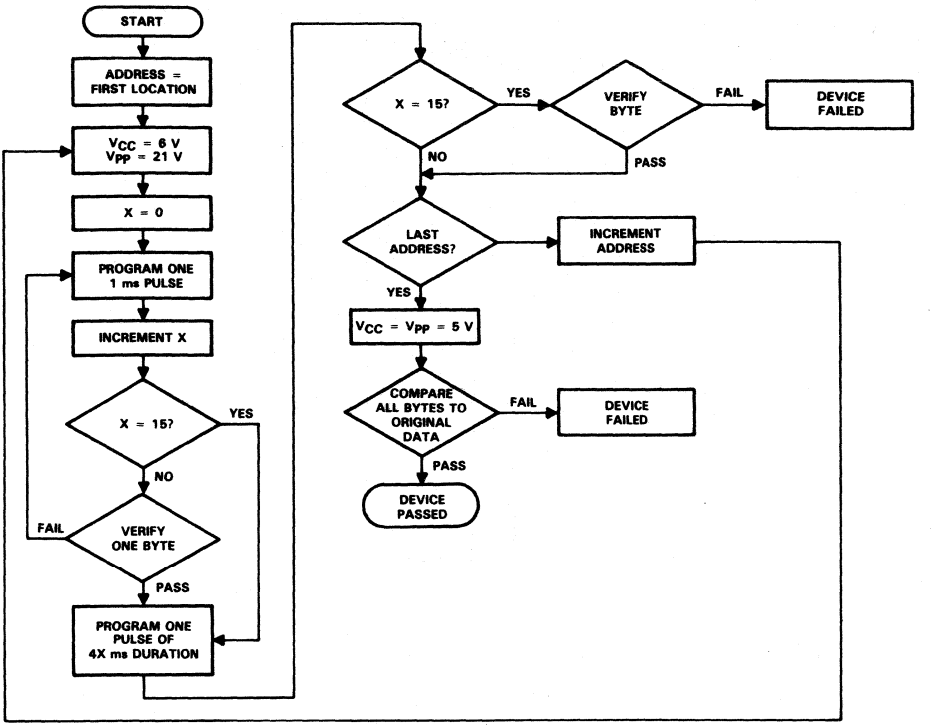
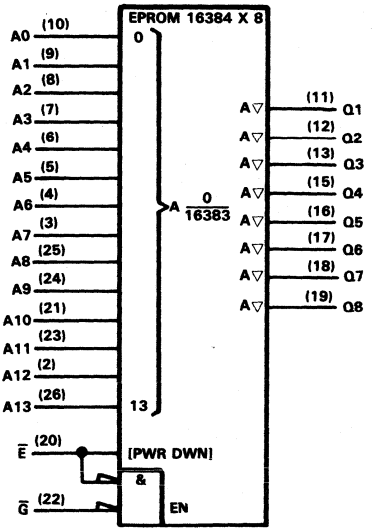


FIGURE 1 – FAST PROGRAMMING FLOWCHART

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC}	−0.6 V to 7 V
Supply voltage, V_{PP}	−0.6 V to 22 V
All input voltage	−0.6 V to 7 V
Output voltage	−0.6 V to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS27128			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{PP}		V_{CC}		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL} (see Note 1)	−0.1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 1: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V			±10	μA
I_{PP1}	V_{PP} supply current (read)	V_{PP} = 5.25 V			5	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{E}$ and $\overline{PGM}$ at V_{IL}			50	mA
I_{CC1}	V_{CC} supply current (standby)	$\overline{E}$ at V_{IH}			40	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{E}$ and $\overline{G}$ at V_{IL}			100	mA

† Typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V		4	6	pF
C_o	Output capacitance	V_O = 0 V		8	12	pF

† Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range, C_L = 100 pF, 1 Series 74 TTL load (see note 2 and figure 2)

PARAMETER		TMS27128-25		TMS27128-30		TMS27128-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		250		300		450	ns
$t_{a(E)}$	Access time from E		250		300		450	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		100		120		150	ns
$t_{dis(G)}$‡	Output disable time from $\overline{G}$	0	60	0	105	0	130	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first	0		0		0		ns

NOTE 2: For switching characteristics and timing measurements, input timing reference levels are 0.8 V and 2 V; output timing reference levels are 0.8 V and 2 V.

‡ Value calculated from 0.5 volt delta to measured output level; $t_{dis(G)}$ is specified from $\overline{G}$ or $\overline{E}$, whichever occurs first. Refer to read cycle timing diagram.

recommended conditions for fast programming routine, T_A = 25°C (see note 2 and fast programming cycle timing diagram)

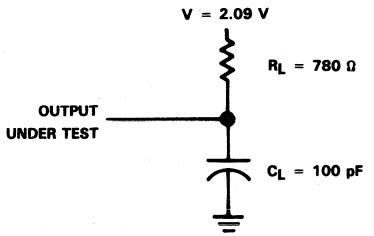
PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 3)	5.75	6	6.25	V
V_{PP}	Supply voltage (see Note 4)	20.5	21	21.5	V
$t_{w(IPGM)}$	$\overline{PGM}$ initial program pulse duration (see Note 5)	0.95	1	1.05	ms
$t_{w(FPGM)}$	$\overline{PGM}$ final pulse duration (see Note 6)	3.8		63	ms
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	V_{PP} setup time	2			μs
$t_{su(VCC)}$	V_{CC} setup time	2			μs
$t_{h(A)}$	Address hold time	0			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{su(E)}$	$\overline{E}$ setup time	2			μs
$t_{su(G)}$	$\overline{G}$ setup time	2			μs

fast programming characteristics, T_A = 25°C (see note 2 and fast programming cycle timing diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{dis(G)FP}$	Output disable time from $\overline{G}$ (see Note 7)	C_L = 100 pF	0		130	ns
$t_{en(G)FP}$	Output enable time from $\overline{G}$	1 Series 74 TTL load			150	

NOTES:
2. For all switching characteristics and timing measurements, input timing reference levels are 0.8 V and 2 V; output timing reference levels are 0.8 V and 2 V.
3. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
4. When programming the TMS27128, connect a 0.1 μF capacitor between V_{PP} and GND to suppress spurious voltage transients which may damage the device.
5. The Initial program pulse duration tolerance is 1 ms ± 5%.
6. The length of the Final pulse will vary from 3.8 ms to 63 ms depending on the number of Initial pulse applications (X).
7. This parameter is only sampled and is not 100% tested.

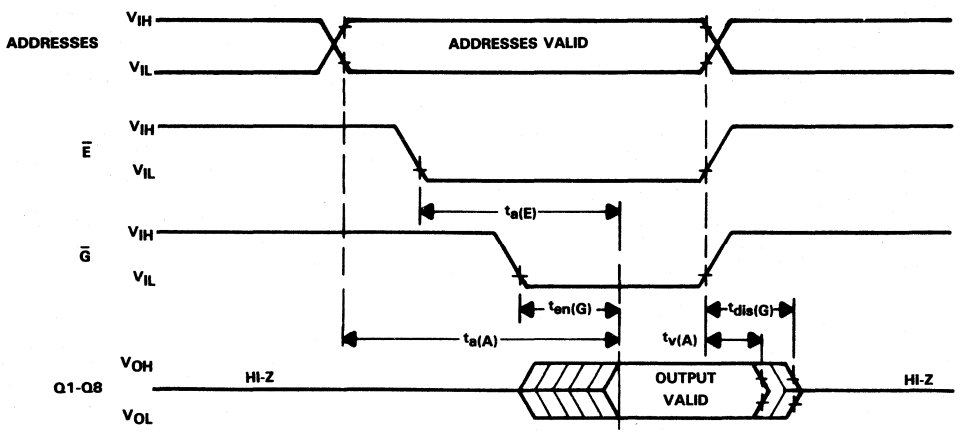
PARAMETER MEASUREMENT INFORMATION



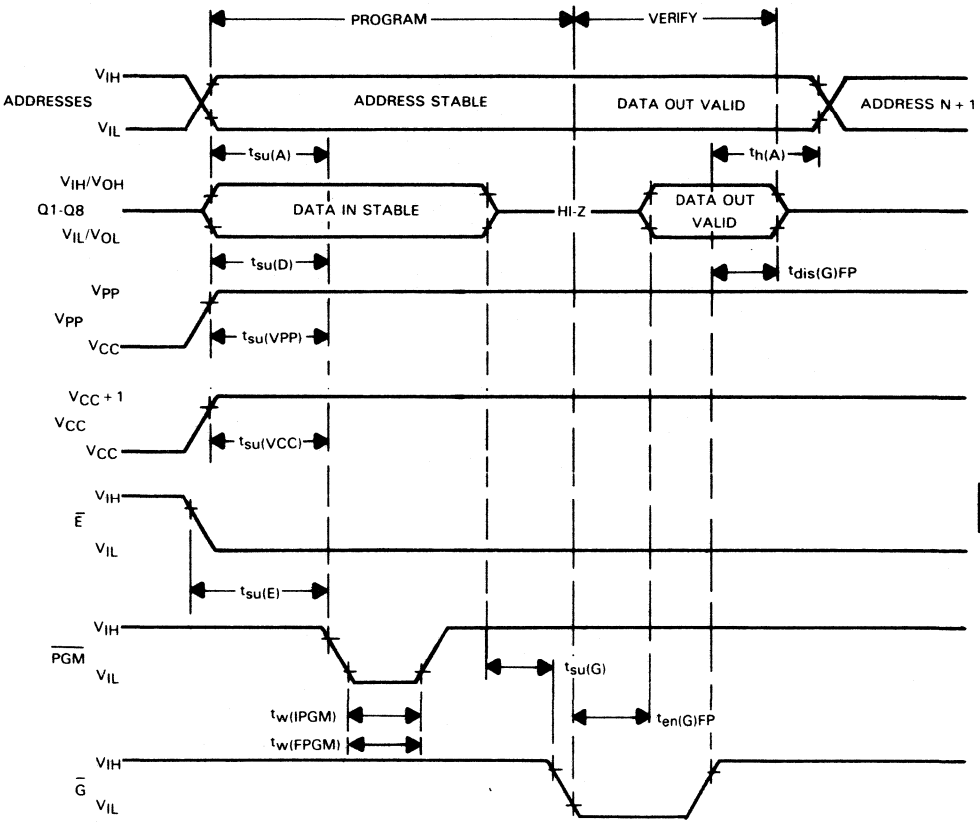
NOTE: $t_f \leq 20$ ns and $t_r \leq 20$ ns.

FIGURE 2 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



fast program cycle timing



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is available from Texas Instruments in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

Please contact

Texas Instruments
P.O. Box 401560
Dallas, Texas 75240

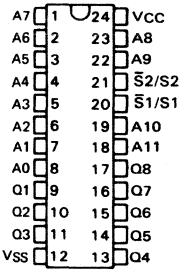
to obtain this brochure.

TMS4664
8192-WORD BY 8-BIT READ-ONLY MEMORY

JUNE 1983 – REVISED OCTOBER 1983

- 8192 X 8 Organization
- Partitioned into Two 4K X 8 Banks
- Fully Static (No Clocks, No Refresh)
- All Inputs and Outputs TTL Compatible
- Single 5-V Power Supply
- Two Chip-Selects for Flexibility and Power-Down Option
- Maximum Access Time from Address . . . 450 ns
- Typical Active Power Dissipation . . . 275 mW
- Available in Chip-on-Board Package Also

TMS4664 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A11	Addresses
Q1 – Q8	Data Out
$\bar{S}1/S1$, $\bar{S}2/S2$	Chip Selects
V_{CC}	+5-V Supply
V_{SS}	Ground

description

The TMS4664 is a 65,536-bit read-only memory organized as 8192 words of 8-bit length. The array is partitioned into two 4096-words of 8-bit length banks. This makes the TMS4664 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any external pull-up resistor. Each output can drive two Series 74 or 74S loads without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Two chip-select controls allow data to be read. These controls are programmable, providing additional system decode flexibility. The data is always available, it is not dependent on external clocking of the control pins.

The TMS4664 is designed for high-density fixed-memory consumer applications.

This ROM is supplied in a 24-pin dual-in-line plastic (NL suffix) package designed for insertion in mounting-hole rows on 600-mil centers. It is also available in the chip-on-board package. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on-chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 the most-significant bit of the word address. Additionally each bank of the array is activated by a particular address. Address FF8 will allow entry and access to the low order bank and FF9 will allow entry and access to the high order bank. After a set of A12 (FF9 or FF8), a normal read cycle must be completed before another set is performed.

All address changes must be made within 30 ns of when the first address changes to prevent address skewing.

chip select/output enable (pins 20 and 21)

Each of these pins can be programmed during mask fabrication to be active with either a high or a low level input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

This document contains information on a new product.
Specifications are subject to change without notice.

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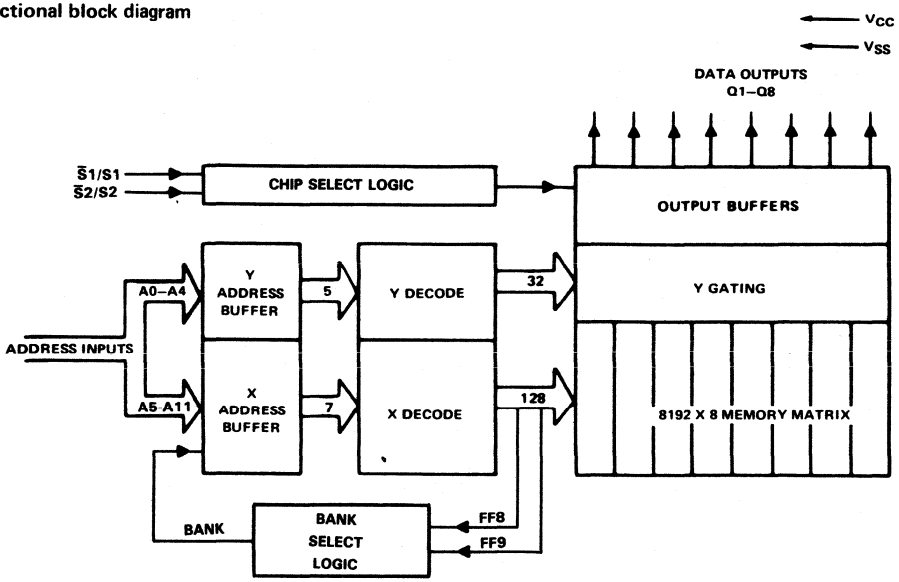
data out (Q1-Q8)

The eight outputs must be enabled by both pins 20 and 21 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant.

The outputs will drive two Series 54/74 TTL circuits without external components.

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1)	−0.5 V to 7 V
Applied output voltage (see Note 1)	−0.5 V to 7 V
Applied input voltage (see Note 1)	−0.5 V to 7 V
Power dissipation	500 mW
Operating free-air temperature	0°C to 70°C
Storage temperature	−55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 3.2 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	$0V \le V_{IN} \le 5.5$ V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	$V_I = V_{CC}$ output not loaded		80	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10%, 2 series 74 TTL loads, C_L = 100 pF†

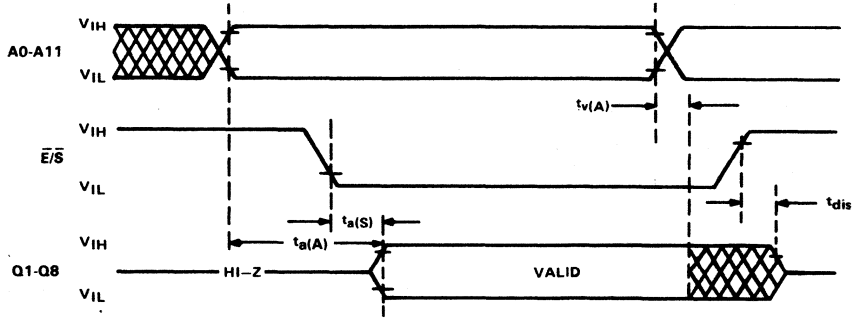
PARAMETER		MIN	MAX	UNIT
$t_{a(A)}$	Access time from address‡		450	ns
$t_{a(S)}$	Access time from chip select‡		200	ns
$t_{v(A)}$	Output data valid after address change	20		ns
t_{dis}	Output disable time from chip select		150	ns

†All AC measurements are made at 10% and 90% points

‡Access time from page select is double normal access time.

NOTE 1: All address changes must be made within 30 ns of when the first address changes to prevent address skewing.

read cycle timing



PROGRAMMING DATA

PROGRAMMING REQUIREMENTS: The TMS4664 NL is a fixed program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer inputs supplied in the format below. The device is organized as 8192 8-bit words with address locations numbered 0 to 8191. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. All data words and addresses in the following format are coded in hexadecimal numbers. In coding all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least significant bit and Q8 the most significant bit. For addresses, A0 is least significant bit and A11 is the most significant.

The input media containing the programming data can be in the form of cards or EPROMs.

Either 16K, 32K, or 64K EPROMs can be used or any combination of them.

The following is a description of how the cards must be formatted, should they be used instead of EPROMs.

INPUT CARD FORMAT

Each code deck submitted by customer shall consist of the following:

1. Title Card
2. Comment Cards
3. Start of Data Card
4. Data Cards

The cards shall be standard 80 column cards with the information in the following format:

TITLE CARD

Card Column	Information
1 – 5	The word 'TITLE' shall be punched in these columns.
6	Blank
7, 8	The letters 'ZA' shall be punched in these columns.
9 – 14	Leave blank. A special device code number will be assigned by Texas Instruments. (left justified)
15	Blank
16 – 30	Customer's Part Number, if required. (left justified)
31	Blank
32	Customer's Part Number to be included as part of device symbolization. Options: Y = Yes N = No
33 – 36	Blank
37	Type of Package Options: B = Chip on board P = Plastic
38 – 40	Blank
41	Logic Level for device pin 20. Options: 1 = chip select mode, outputs enabled with high level. 0 = chip select mode, outputs enabled with low level.
42	Logic Level for device pin 21. Options: 1 = chip select mode, outputs enabled with high level. 0 = chip select mode, outputs enabled with low level.
43	Blank.
44	Blank.
45 – 49	Texas Instruments Device Series (4664, etc.) (left justified)

COMMENT CARDS

Any number of comment cards may be used for specifying the customer's name, individual to contact, telephone number, address, any special instructions, etc. The format for these cards is as follows: The Letter 'C' (for comment) must be punched in column 1, columns 2 – 4 must be blank, and comments can be punched in columns 5 – 80.

START OF DATA CARD

This card is to identify that the next card will be the beginning of customer's code. Format is as follows: Columns 1 – 4 must have '&ROM' punched in them. The remainder of card is blank.

DATA CARDS

There will be 256 data cards supplied for each customer code. Each card will contain (in hexadecimal) the data for 32 memory locations. Each data card shall be in the following format:

Card Column	Information
1 – 4	Hexadecimal address of first word on the card, four bits in length.
5, 6	Blank.
7 – 70	Data. Each 8-bit data byte is represented by two ASCII characters to represent a hexadecimal value of '00' to 'FF'.
71, 72	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from columns 1 to 70, evaluate modulo 256 (carry from high order bit ignored). For purposes of calculating the checksum, the value of columns 5 and 6 are defined to be zero. Adding together, modulo 256, all 8-bit bytes from columns 1 to 70 (columns 5 and 6 = 0), then adding the checksum, results in zero.
73 – 76	Blank.
77 – 80	Card sequence number, in decimal. (right justified).

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

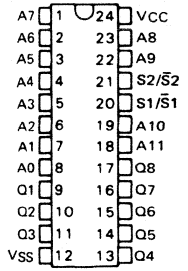
TMS4732
4096-WORD BY 8-BIT READ-ONLY MEMORY

MAY 1977 – REVISED JULY 1983

- **4096 X 8 Organization**
- **All Inputs and Outputs TTL Compatible**
- **Fully Static (No Clocks, No Refresh)**
- **Single 5-V Power Supply**
- **Maximum Access Time From Address:**

  TMS4732-30 300 ns
  TMS4732-35 350 ns
  TMS4732-45 450 ns
- **Typical Power Dissipation . . . 275 mW**
- **3-State Outputs for OR-Ties**
- **Pin-Compatible with TMS2532 EPROM**
- **Two Output Enable Controls for Chip Select Flexibility**

TMS4732 . . . JL OR NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A11	Addresses
Q1 – Q8	Data Out
S1/S̄1, S2/S̄2	Chip Selects
V_{CC}	+5-V Supply
V_{SS}	Ground

description

The TMS4732 is a 32,768-bit read-only memory organized as 4096 words of 8-bit length. This makes the TMS4732 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any internal pull-up resistor. Each output can drive one Series 74 or 74S load without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Two chip-select controls allow data to be read. These controls are programmable, providing additional system decode flexibility. The data is always available, it is not dependent on external clocking of the control pins.

The TMS4732 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. The part is pin compatible with the TMS2532 4096 × 8 EPROM, which aids in prototyping and code verification.

This ROM is supplied in 24-pin dual-in-line-plastic (NL suffix) or ceramic (JL suffix) packages designed for insertion in mounting-hole rows on 600-mil centers or chip on board. The device is designed for operation from 0°C to 70°C.

operation

address (A0 – A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on-chip to select one of 4096 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 the most-significant bit of the word address.

chip select/output enable (pins 20 and 21)

Each of these pins can be programmed during mask fabrication to be active with either a high- or a low-level input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

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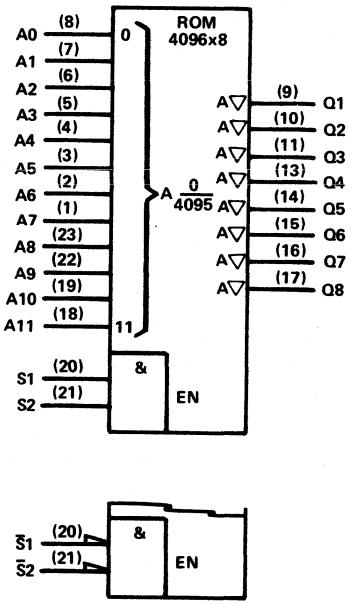
data out (Q1 – Q8)

The eight outputs must be enabled by pins 20 and 21 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

The outputs will drive two Series 54/74 TTL circuits without external components.

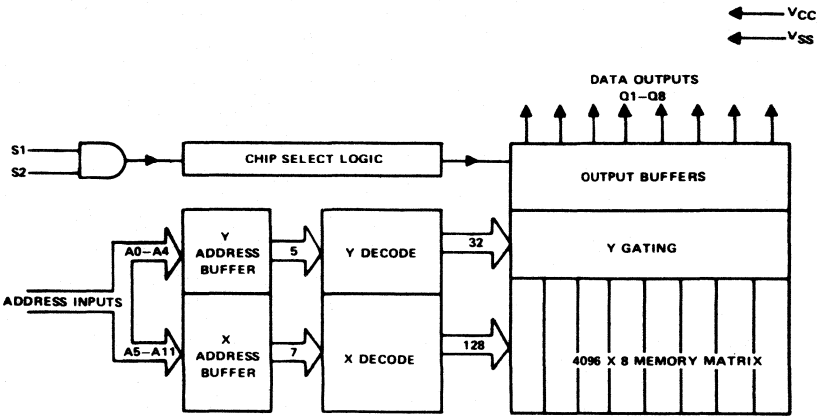
logic symbol†



Pins 20 and 21 can be active-high as shown in the upper symbol or active-low as shown in the lower (partial) symbol.

†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . −0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . −0.5 V to 7 V
Applied input voltage (see Note 1) . . . . . −0.5 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2	2.4	$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

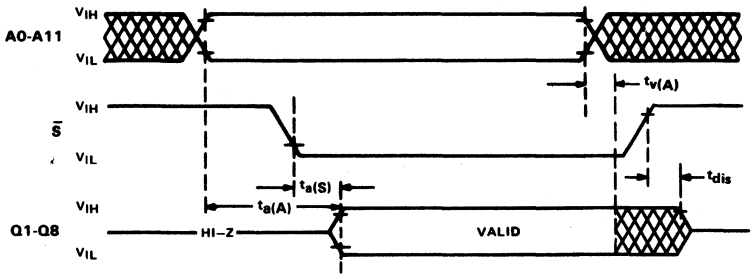
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 3.2 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		80	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10%, 2 series 74 TTL loads, C_L = 100 pF†

PARAMETER		TMS4732-30		TMS4732-35		TMS4732-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		300		350		450	ns
$t_{a(S)}$	Access time from chip select		120		120		120	ns
$t_{v(A)}$	Output data valid after address change	20		20		20		ns
t_{dis}	Output disable time from chip select		100		100		100	ns

†All AC measurements are made at 10% and 90% points

read cycle timing



PROGRAMMING DATA

ROGRAMMING REQUIREMENTS: The TMS4732 is a fixed program memory in which the programming is performed by
l at the factory during the manufacturing cycle to the specific customer inputs supplied in the format below. The device
s organized as 4096 8-bit words with address locations numbered 0 to 4095. The 8-bit words can be coded as a 2-digit
exadecimal number between 00 and FF. All data words and addresses in the following format are coded in hexadecimal
umbers. In coding, all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least
ignificant bit and Q8 the most significant bit. For addresses, A0 is the least significant bit and A11 is the most significant.

he input media containing the programming data can be in the form of cards or EPROMs.

ither 16K, 32K, or 64K EPROMs can be used, or any combination of them.

he following is a description of how the cards must be formatted, should they be used instead of EPROMS.

INPUT CARD FORMAT

ach code deck submitted by customer shall consist of the following:

1. Title Card
2. Comment Cards
3. Start of Data Card
4. Data Cards

The cards shall be standard 80 column cards with the information in the following format:

TITLE CARD

Card Column	Information
1 – 5	The word 'TITLE' shall be punched in these columns.
6	Blank
7, 8	The letters 'ZA' shall be punched in these columns.
9 – 14	Leave blank. A special device code number will be assigned by Texas Instruments. (left justified)
15	Blank
16 – 30	Customer's Part Number, if required. (left justified)
31	Blank
32	Customer's Part Number to be included as part of device symbolization. Options: Y = Yes N = No
33 – 36	Blank
37	Type of Package Options: C = ceramic P = plastic B = chip on board
38 – 40	Blank

41	Logic Level for device pin 20. Options: 1 = chip-select mode outputs enabled with high level. 0 = chip-select mode, outputs enabled with low level.
42	Logic Level for device pin 21 Options: 1 = chip-select mode outputs enabled with high level. 0 = chip-select mode, outputs enabled with low level.
43	Blank
44	Blank
45 – 49	Texas Instruments Device Series (4732B, 4732C, etc.) (left justified)

COMMENT CARDS

Any number of comment cards may be used for specifying the customer's name, individual to contact, telephone number, address, any special instructions, etc. The format for these cards is as follows: The letter 'C' (for comment) must be punched in column 1, columns 2-4 must be blank, and comments can be punched in columns 5-80.

START OF DATA CARD

This card is to identify that the next card will be in the beginning of customer's code. Format is as follows: Columns 1-4 must have '&ROM' punched in them. The remainder of card is blank.

DATA CARDS

There will be 128 data cards supplied for each customer code. Each card will contain (in hexadecimal) the data for 32 memory locations. Each data card shall be in the following format:

Card Column	Information
1 – 3	Hexadecimal address of first word on the card, four bits in length.
4	Blank
5 – 68	Data. Each 8-bit data byte is represented by two ASCII characters to represent a hexadecimal value of '00' to 'FF'.
69 – 70	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from columns 1 to 68, evaluate modulo 256 (carry from high order bit ignored). For purposes of calculating the checksum, the value of column 4 is defined as zero. Adding together, modulo 256, all 8-bit bytes from columns 1 to 68 (column 4 = 0), then adding the checksum, results in zero.

EXAMPLE JCL DECK TO RUN GATE PLACEMENT

```
//  CIC JOB CARD
//  EXEC GATEPLM, DEV=TM4732A, DOMTAPE=volume serial number
Input Cards
//  The input card to PFP is: //PFP DD DSN=&&PFPIN, DISP=OLD
```

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS4764
8192-WORD BY 8-BIT READ-ONLY MEMORY

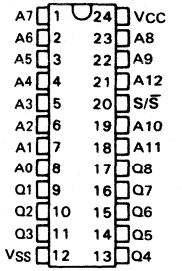
JUNE 1981 – REVISED JULY 1983

- **8192 X 8 Organization**
- **Fully Static (No Clocks, No Refresh)**
- **All Inputs and Outputs TTL Compatible**
- **Single 5-V Power Supply**
- **Maximum Access Time From Address:**

TMS4764-30	300 ns
TMS4764-35	350 ns
TMS4764-45	450 ns

- **Typical Active Power Dissipation . . . 275 mW**

TMS4764 . . . JL OR NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A12	Addresses
Q1 – Q8	Data Out
S/S̄	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground

description

The TMS4764 is a 65,536-bit read-only memory organized as 8192 words of 8-bit length. This makes the TMS4764 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any internal pull-up resistor. Each output can drive two Series 74 or 74S loads without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Pin 20 is programmable, providing additional system flexibility. The data is always available, it is not dependent on external clocking of pin 20.

The TMS4764 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. It is pin compatible with TI's full line of ROMs and EPROMs.

This ROM is supplied in 24-pin dual-in-line-plastic (NL suffix) or ceramic (JL suffix) packages designed for insertion in mounting-hole rows on 600-mil centers or chip on board. The device is designed for operation from 0°C to 70°C.

operation

address (A0 – A12)

The address valid interval determines the device cycle time. The 13-bit positive-logic address is decoded on-chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A12 the most-significant bit of the word address.

chip select (S or S̄)

Pin 20 can be programmed during mask fabrication to be active with either a high- or a low-level input. When the signal is active, all eight outputs are enabled and the eight-bit addressed word can be read. When the signal is not active, all eight outputs are in a high-impedance state.

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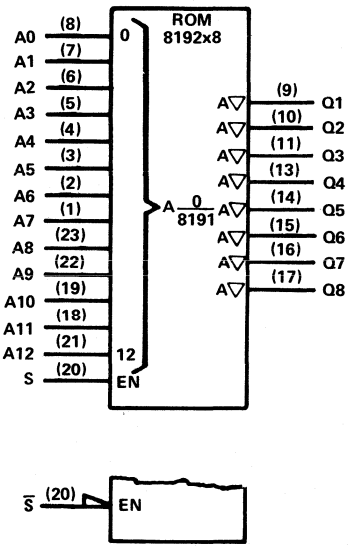
data out (Q1 – Q8)

The eight outputs must be enabled by pin 20 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

The outputs will drive two Series 54/74 TTL circuits without external components.

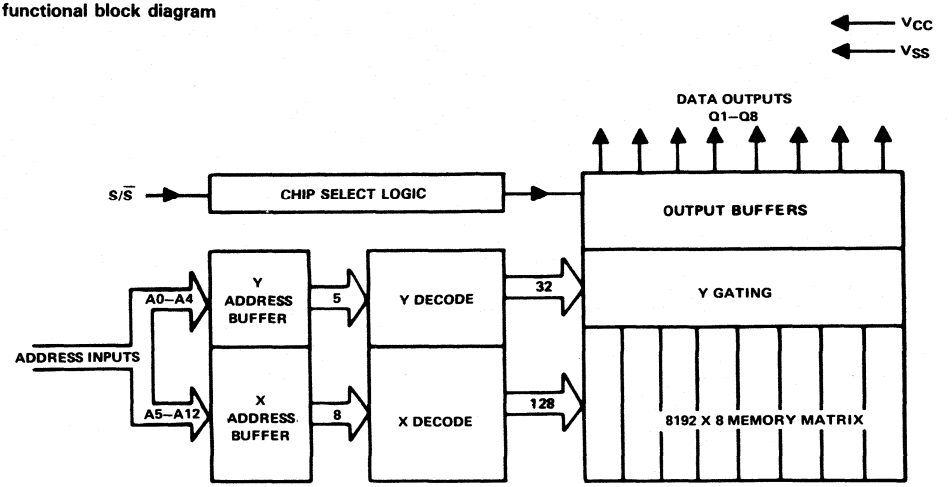
logic symbol†



Pin 20 can be active-high as shown in the upper symbol or active-low as shown in the lower (partial) symbol.

†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . −0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . −0.5 V to 7 V
Applied input voltage (see Note 1) . . . . . −0.5 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

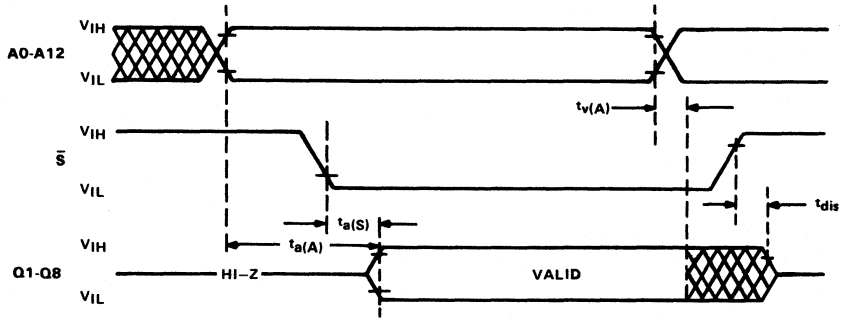
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 3.2 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	0V ≤ V_{IN} ≤ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	V_I = V_{CC} output not loaded		80	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10%, 2 series 74 TTL loads, C_L = 100 pF†

PARAMETER		TMS4764-30		TMS4764-35		TMS4764-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		300		350		450	ns
$t_{a(S)}$	Access time from chip select		120		120		120	ns
$t_{v(A)}$	Output data valid after address change	20		20		20		ns
t_{dis}	Output disable time from chip select		100		100		100	ns

† All AC measurements are made at 10% and 90% points

read cycle timing



ROM Devices

7

PROGRAMMING DATA

PROGRAMMING REQUIREMENTS: The TMS4764 is a fixed program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer inputs supplied in the format below. The device is organized as 8192 8-bit words with address locations numbered 0 to 8191. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. All data words and addresses in the following format are coded in hexadecimal numbers. In coding, all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least significant bit and Q8 the most significant bit. For addresses, A0 is least significant bit and A12 is the most significant.

The input media containing the programming data can be in the form of cards or EPROMs.

Either 16K, 32K, or 64K EPROMs can be used, or any combination of them.

The following is a description of how the cards must be formatted, should they be used instead of EPROMS.

PROGRAMMING INSTRUCTIONS – 64K ROM

Each code deck submitted by customer shall consist of the following:

1. Title Card
2. Comment Cards
3. Start of Data Card
4. Data Cards

The cards shall be standard 80 column cards with the information in the following format:

TITLE CARD

Card Column	Information
1 – 5	The word 'TITLE' shall be punched in these columns.
6	Blank
7, 8	The letters 'ZA' shall be punched in these columns.
9 – 14	Leave blank. A special device code number will be assigned by Texas Instruments. (left justified)
15	Blank
16 – 30	Customer's Part Number, if required. (left justified)
31	Blank
32	Customer's Part Number to be included as part of device symbolization. Options: Y = Yes N = No
33 – 36	Blank
37	Type of Package Options: C = ceramic P = plastic B = chip on board
38 – 40	Blank

41	Logic Level for pin 20 on 24-pin package. Options: 1 = chip-select mode outputs enabled with high level. 0 = chip-select mode, outputs enabled with low level.
42 – 44	Blank
45 – 49	Texas Instruments Device Series (ie. 4764B, 4764C, etc.) (left justified)

COMMENT CARDS

Any number of comment cards may be used for specifying the customer's name, individual to contact, telephone number, address, any special instructions, etc. The format for these cards is as follows: The letter 'C' (for comment) must be punched in column 1, columns 2-4 must be blank, and comments can be punched in columns 5-80.

START OF DATA CARD

This card is to identify that the next card will be in the beginning of customer's code. Format is as follows: Columns 1-4 must have '&ROM' punched in them. The remainder of card is blank.

DATA CARDS

There will be 256 data cards supplied for each customer code. Each card will contain (in hexadecimal) the data for 32 memory locations. Each data card shall be in the following format:

Card Column	Information
1 – 4	Hexadecimal address of first word on the card, four bits in length.
5, 6	Blank
7 – 70	Data. Each 8-bit data byte is represented by two ASCII characters to represent a hexadecimal value of '00' to 'FF'.
71, 72	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from columns 1 to 70, evaluate modulo 256 (carry from high order bit ignored). For purposes of calculating the checksum, the value of columns 5 and 6 are defined to be zero. Adding together, modulo 256, all 8-bit bytes from columns 1 to 70 (columns 5 and 6 = 0), then adding the checksum, results in zero.
73 – 76	Blank
77 – 80	Card sequence number, in decimal. (right justified).

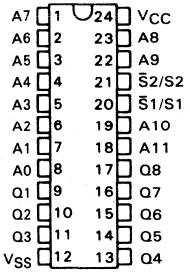
Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS4964
8192-WORD BY 8-BIT READ-ONLY MEMORY

JUNE 1983 – REVISED OCTOBER 1983

- **8192 X 8 Organization**
- **Partitioned into Eight 1K X 8 Pages**
- **Fully Static (No Clocks, No Refresh)**
- **All Inputs and Outputs TTL Compatible**
- **Single 5-V Power Supply**
- **Two Chip-Selects for Flexibility and Power-Down Option**
- **Maximum Access Time from Address . . . 450 ns**
- **Typical Active Power Dissipation . . . 275 mW**
- **Available in Chip-on-Board Package Also**

TMS4964 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A11	Addresses
Q1 – Q8	Data Out
S̄1/S1, S̄2/S2	Chip Selects
V_{CC}	+5-V Supply
V_{SS}	Ground

description

The TMS4964 is a 65,536-bit read-only memory organized as 8192 words of 8-bit length. The array is subdivided into eight 1024 bits × 8 pages. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

All inputs can be driven directly by Series 74 TTL circuits without the use of any external pull-up resistor. Each output can drive two Series 74 or 74S loads without external resistors. The data outputs are three-state for OR-tieing multiple devices on a common bus. Two chip-select controls allow data to be read. These controls are programmable, providing additional system decode flexibility. The data is always available, it is not dependent on external clocking of the control pins.

The TMS4964 is designed for high-density fixed-memory consumer applications.

This ROM is supplied in a 24-pin dual-in-line plastic (NL suffix) package designed for insertion in mounting-hole rows on 600-mil centers. It is also available in the chip-on-board package. The device is designed for operation from 0°C to 70°C.

operation

address (A0-A11)

The address-valid interval determines the device cycle time. The 12-bit positive-logic address is decoded on-chip to select one of 8192 words of 8-bit length in the memory array. A0 is the least-significant bit and A11 the most-significant bit of the word address. Additionally 24 addresses can generate traps which allow the selection of any 3 of 7 pages to be active at any point in time. The 8th page is always active. After a write to a pointer register, a normal read cycle must be completed before another write is performed. A normal read is an address outside of the range FE0 to FE7.

All address changes must be made within 30 ns of when the first address changes to prevent address skewing.

chip select/output enable (pins 20 and 21)

Each of these pins can be programmed during mask fabrication to be active with either a high or low level input. When both signals are active, all eight outputs are enabled and the eight-bit addressed word can be read. When either signal is not active, all eight outputs are in a high-impedance state.

This document contains information on a new product.
Specifications are subject to change without notice.

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data out (Q1-Q8)

The eight outputs must be enabled by both pins 20 and 21 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

The outputs will drive two Series 54/74 TTL circuits without external components.

page operation

The ROM is organized into 8K x 8-bit bytes. Only 12 address bits or a maximum of 4K bytes may be accessed at one time. The 4K address space is segmented into four 1K banks and memory is partitioned into eight 1K pages. Bank 3 containing page 7 is always resident. Any three of the eight pages, 0 thru 7, are immediately accessable. The banks, which are defined by page pointers, are selected by address bits A3 and A4 (see Table 1).

TABLE 1

A4	A3	BANK	ADDRESS RANGE
L	L	0	000 – 3FF
L	H	1	400 – 7FF
H	L	2	800 – BFF
Resident		3	C00 – FDF

H = high level, L = low level

The content of the page pointers is loaded with address bits A2, A1 and A0. Three different pages in the range 0 thru 7 may be loaded one into each of the three pointers. Table 2 shows address/page pointer relationship.

TABLE 2

A2	A1	A0	PAGE
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level

The pointers are write-only locations; to load the pointers, A11 thru A05 are set to high logic levels. Then pointers are always loaded by the range of addresses shown in Table 3.

TABLE 3

POINTER	ADDRESS RANGE
0	FE0 to FE7
1	FE8 to FEF
2	FF0 to FF7

When an address outside the range FE0 to FF7 is accessed, address bits A11 and A10 select pointer 0, 1 or 2 and the pointer content is mapped to the internal address bits A12, A11 and A10. When A10 and A11 are both high, page 7 is selected (see Table 4). Internal address bits A9 thru A0 are the same as the external address bits A9 thru A0.

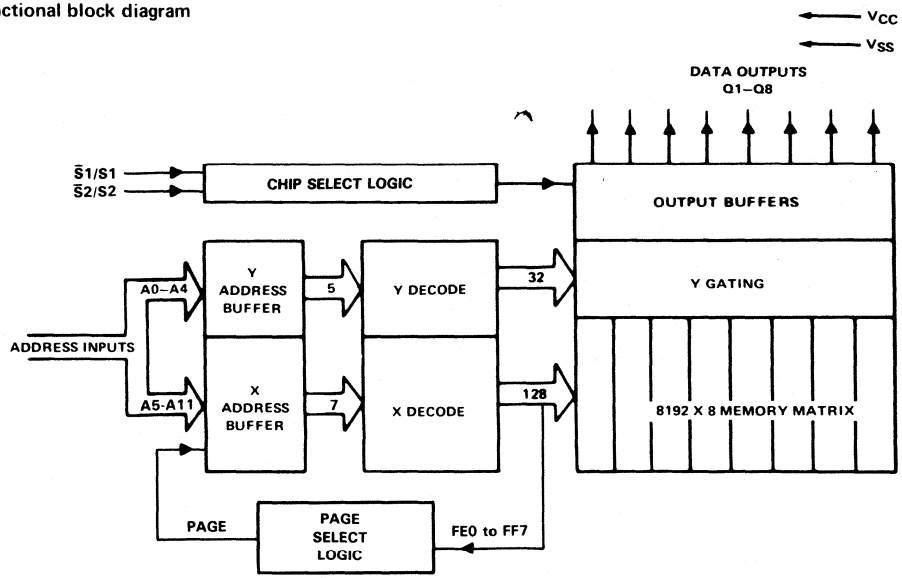
TABLE 4

A11	A10	SELECTED
L	L	Pointer 0
L	H	Pointer 1
H	L	Pointer 2
H	H	Page 7

H = high level, L = low level

As an example, suppose it is desired to select the third 1K ROM page by addresses 400 thru 7FF. This address space is represented by pointer 1 because of the condition of A11 and A10. To write to pointer 1; bits A4, A3 = LH. The contents of the pointer is 3; bits A2, A1, A0 = LHH. Therefore, location FEB is accessed.

functional block diagram



absolute maximum ratings

Supply voltage to ground potential (see Note 1) . . . . . −0.5 V to 7 V
Applied output voltage (see Note 1) . . . . . −0.5 V to 7 V
Applied input voltage (see Note 1) . . . . . −0.5 V to 7 V
Power dissipation . . . . . 500 mW
Operating free-air temperature . . . . . 0°C to 70°C
Storage temperature . . . . . −55°C to 150°C

Note 1: Voltage values are with respect to V_{SS}

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10% (unless otherwise noted)

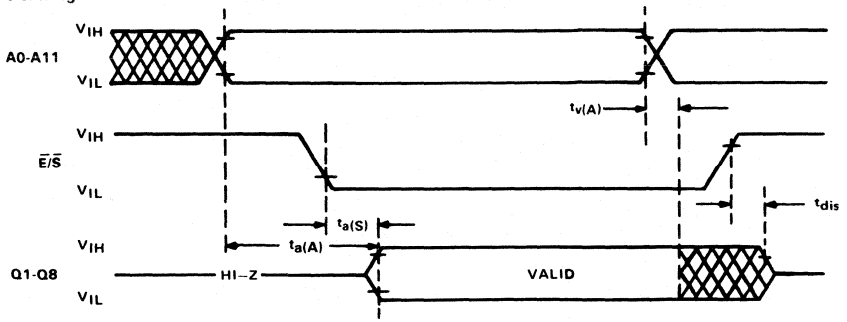
PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −400 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 3.2 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	$0V \le V_{IN} \le 5.5$ V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	$V_I = V_{CC}$ output not loaded		80	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10%, 2 series 74 TTL loads, C_L = 100 pF†

PARAMETER		MIN	MAX	UNIT
$t_{a(A)}$	Access time from address‡		450	ns
$t_{a(S)}$	Access time from chip select‡		200	ns
$t_{v(A)}$	Output data valid after address change	20		ns
t_{dis}	Output disable time from chip select		150	ns

†All AC measurements are made at 10% and 90% points
‡Access time from page select is double normal access time.
NOTE 1: All address changes must be made within 30 ns of when the first address changes to prevent address skewing.

read cycle timing



PROGRAMMING DATA

PROGRAMMING REQUIREMENTS: The TMS4964NL is a fixed program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer inputs supplied in the format below. The device is organized as 8192 8-bit words with address locations numbered 0 to 8191. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. All data words and addresses in the following format are coded in hexadecimal numbers. In coding all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least significant bit and Q8 the most significant bit. For addresses, A0 is least significant bit and A11 is the most significant.

The input media containing the programming data can be in the form of cards or EPROMs.

Either 16K, 32K, or 64K EPROMs can be used or any combination of them.

The following is a description of how the cards must be formatted, should they be used instead of EPROMs.

INPUT CARD FORMAT

Each code deck submitted by customer shall consist of the following:

1. Title Card
2. Comment Cards
3. Start of Data Card
4. Data Cards

The cards shall be standard 80 column cards with the information in the following format:

TITLE CARD

Card Column	Information
1-5	The word 'TITLE' shall be punched in these columns.
6	Blank
7,8	The letters 'ZA' shall be punched in these columns.
9-14	Leave blank. A special device code number will be assigned by Texas Instruments. (left justified)
15	Blank
16-30	Customer's Part Number, if required. (left justified)
31	Blank
32	Customer's Part Number to be included as part of device symbolization. Options: Y = Yes N = No
33-36	Blank
37	Type of Package Options: B = chip on board P = plastic
38-40	Blank
41	Logic Level for device pin 20. Options: 1 = chip select mode, outputs enabled with high level. 0 = chip select mode, outputs enabled with low level.
42	Logic Level for device pin 21. Options: 1 = chip select mode, outputs enabled with high level. 0 = chip select mode, outputs enabled with low level.
43	Blank.
44	Blank.
45-49	Texas Instruments Device Series (4964, etc.) (left justified)

COMMENT CARDS

Any number of comment cards may be used for specifying the customer's name, individual to contact, telephone number, address, any special instructions, etc. The format for these cards is as follows: The letter 'C' (for comment) must be punched in column 1, columns 2-4 must be blank, and comments can be punched in columns 5-80.

START OF DATA CARD

This card is to identify that the next card will be the beginning of customer's code. Format is as follows: Columns 1-4 must have '&ROM' punched in them. The remainder of card is blank.

DATA CARDS

There will be 256 data cards supplied for each customer code. Each card will contain (in hexadecimal) the data for 32 memory locations. Each data card shall be in the following format:

Card Column	Information
1-4	Hexadecimal address of first word on the card, four bits in length.
5,6	Blank.
7-70	Data. Each 8-bit data byte is represented by two ASCII characters to represent a hexadecimal value of '00' to 'FF'.
71,72	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from columns 1 to 70, evaluate modulo 256 (carry from high order bit ignored). For purposes of calculating the checksum, the value of columns 5 and 6 are defined to be zero. Adding together, modulo 256, all 8-bit bytes from columns 1 to 70 (columns 5 and 6 = 0), then adding the checksum, results in zero.
73-76	Blank.
77-80	Card sequence number, in decimal. (right justified).

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS47128
16,384-WORD BY 8-BIT READ-ONLY MEMORY

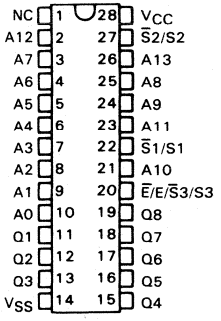
JUNE 1983

- **16,384 X 8 Organization**
- **Fully Static (No Clocks, No Refresh)**
- **All Inputs and Outputs TTL Compatible**
- **Single 5-V Power Supply**
- **Optional Power Down or Chip Select**
- **64K Bank Select Option**
- **Maximum Access Time from Address or Power Down:**

TMS47128-25	250 ns
TMS47128-35	350 ns
TMS47128-45	450 ns

- **Worst Case Active Power Dissipation . . . 330 mW**
- **Worst Case Standby Power Dissipation . . . 66 mW**

TMS47128 . . . JL OR NL PACKAGE†
STANDARD ROM
(TOP VIEW)



† The package for the bank select ROM is shown on page 2.

description

The TMS47128 is a 131,072-bit read-only memory organized as 16,384 words of 8-bit length. This makes the TMS47128 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

There are two versions of the TMS47128: the standard ROM with options on chip selects and power down, and the bank select ROM with similar options. The operation section of this data sheet describes both versions.

PIN NOMENCLATURE STANDARD ROM	
A0-A13	Addresses
Ē/E/S̄3/S3	Chip Enable/Power Down or Chip Select
NC	No Connection
Q1-Q8	Data Out
S̄1/S1, S̄2/S2	Chip Selects
V_{CC}	+5-V Supply
V_{SS}	Ground

The TMS47128 is fully compatible with Series 74, 74S, or 74LS TTL. The data outputs are three-state for OR-tieing multiple devices on a common bus. Pins 20, 22, and 27 are mask-programmable, providing additional system flexibility. The data is always available, it is not dependent on external clocking of pins 20, 22, or 27.

The TMS47128 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. It is pin compatible with TI's full line of ROMs and EPROMs.

This ROM is supplied in 28-pin dual-in-line plastic (NL suffix) or ceramic (JL suffix) packages designed for insertion in mounting-hole rows on 600 mil centers. The device is designed for operation from 0°C to 70°C.

operation, standard ROM

address (A0-A13)

The address-valid interval determines the device cycle time. The 14-bit positive-logic address is decoded on-chip to select one of 16,384 words of 8-bit length in the memory array. A0 is the least-significant bit and A13 the most-significant bit of the word address.

chip select (S̄1 or S1 and S̄2 or S2)

Pins 22 and 27 can be programmed during mask fabrication to be active with either a high- or a low-level input. When

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the signals on pins 20, 22, and 27 are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When any of the signals on pins 20, 22, and 27 are not active, all eight outputs are in a high-impedance state.

power down (E or $\overline{E}$) or chip select (S3 or $\overline{S3}$)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin (E or $\overline{E}$) or a third chip-select pin (S3 or $\overline{S3}$). Each option can be active-high or active-low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 12 mA. With the chip-select option, pin 20 is functionally identical to pins 22 and 27.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20, 22, and 27 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

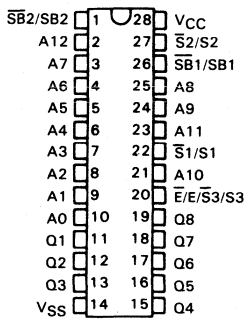
operation, bank select ROM option

Pins 26 ($\overline{SB1}$ or SB1) and 1 ($\overline{SB2}$ or SB2) can be programmed during mask fabrication to select either of two 64K banks. When this option is selected, A0 through A12 address an 8K × 8 word bank. The bank select pins can be either active high or active low with SB1 selecting bank 1 and SB2 selecting bank 2. Bank one represents the least-significant 64K bank and bank two represents the most-significant bank. All bank select pins in the inactive state or more than one bank select pin active will drive all outputs to the high-impedance state.

The chip-select and power-down options previously described for the standard ROM apply equally to the bank select ROM version.

Bank select input level specifications are identical to the input level specifications of the standard ROM.

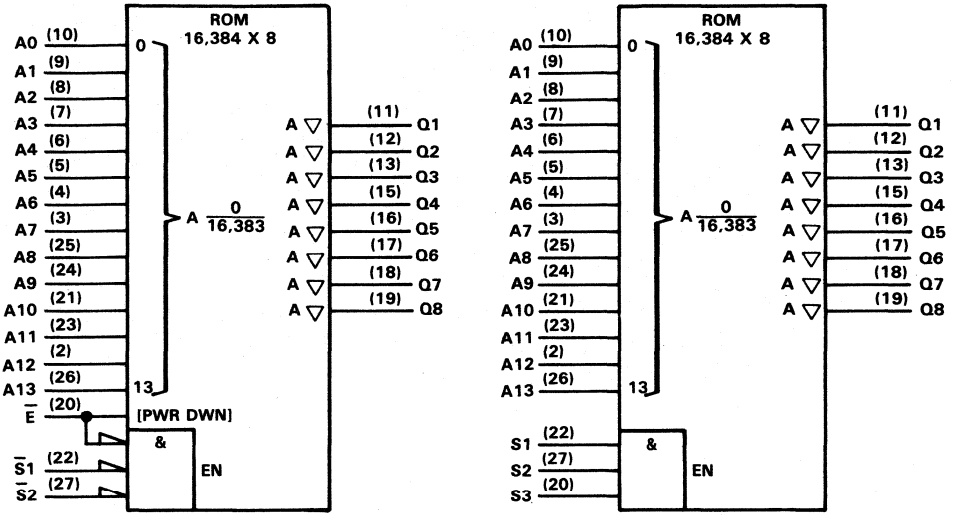
TMS47128 . . . JL OR NL PACKAGE
BANK SELECT ROM
(TOP VIEW)



PIN NOMENCLATURE BANK SELECT ROM	
A0-A12	Addresses
$\overline{E}$/E/$\overline{S3}$/S3	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
$\overline{S1}$/S1, $\overline{S2}$/S2	Chip Selects
$\overline{SB1}$/SB1, $\overline{SB2}$/SB2	Bank Selects
V_{CC}	+5-V Supply
V_{SS}	Ground

logic symbols†

STANDARD ROMS

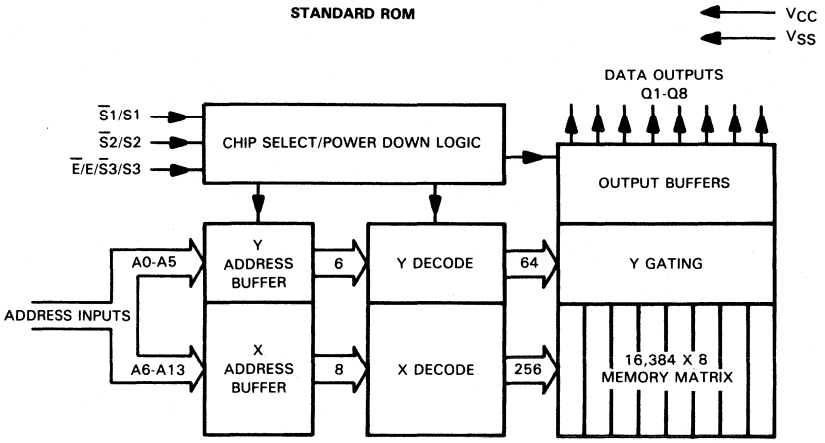


Pins 20, 22 and 27 can be active-low as shown in the symbol on the left or active-high as shown in the symbol on the right. In addition, pin 20 can be either a third chip select (S3 or $\overline{S3}$) or a chip enable/power down (E or $\overline{E}$).

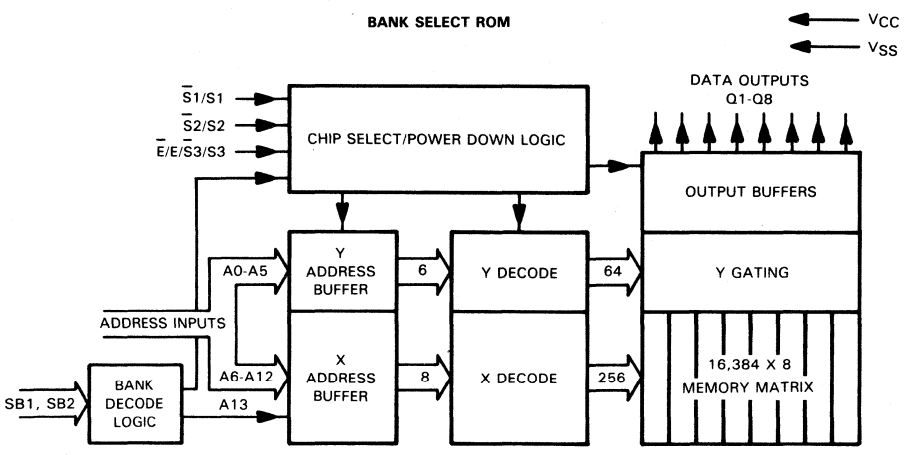
†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

functional block diagrams

STANDARD ROM



BANK SELECT ROM



absolute maximum ratings

Supply voltage to ground potential (see Note 1)	−0.5 V to 7 V
Applied output voltage (see Note 1)	−1 V to 7 V
Applied input voltage (see Note 1)	−1 V to 7 V
Power dissipation	500 mW
Operating free-air temperature	0°C to 70°C
Storage temperature	−55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{DD} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} = 5.5 V,	$0_V \le V_{IN} \le$ 5.5 V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	$V_I = V_{CC}$ Output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			12	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10%, see figure 1†

PARAMETER		TMS47128-25		TMS47128-35		TMS47128-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(AD)}$	Access time from address		250		350		450	ns
$t_{a(S)}$	Access time from chip select		120		120		120	
$t_{a(PD)}$	Access time from power down/chip enable		250		350		450	
$t_{v(A)}$	Output data valid after address change	10		10		10		
t_{dis}	Output disable time from chip select/chip enable		100		100		100	
$t_{en(S)}$	Output enable time from chip select	10		10		10		
$t_{en(E)}$	Output enable time from chip enable	10		10		10		

† All AC measurements are made at 10% and 90% points.

64K bank decode switching characteristics†

PARAMETER		TMS47128-25		TMS47128-35		TMS47128-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(SB)}$	Access time from bank select		250		350		450	ns
$t_{en(SB)}$	Output enable time from bank select	10		10		10		
$t_{dis(SB)}$	Output disable time from bank select		100		100		100	

† Previously defined switching characteristics remain unchanged.

PARAMETER MEASUREMENT INFORMATION

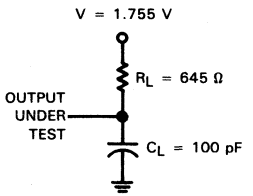
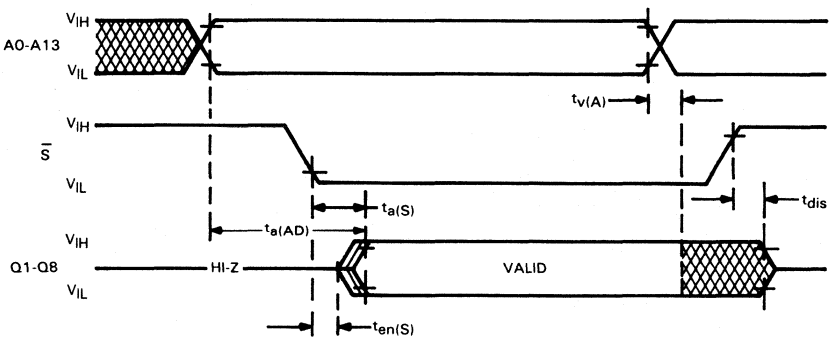
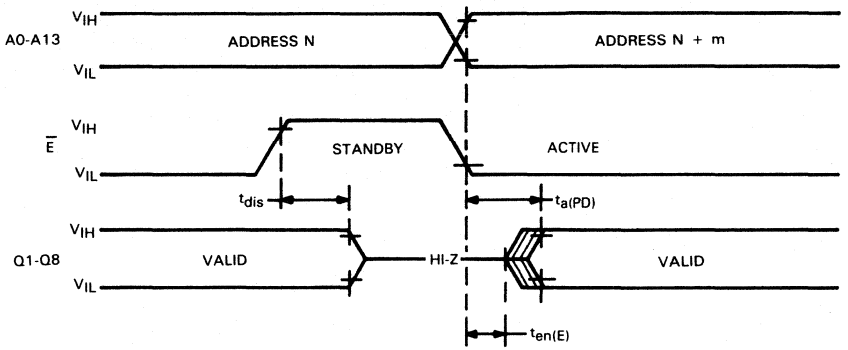


FIGURE 1 – LOAD CIRCUIT

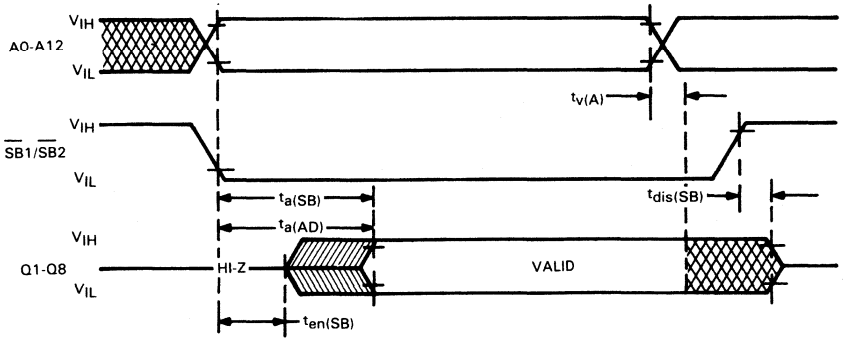
read cycle timing



standby mode



64K bank select mode read cycle timing



PROGRAMMING DATA

PROGRAMMING REQUIREMENTS: The TMS47128 is a fixed program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer inputs supplied in the format below. The device is organized as 16,384 8-bit words with address locations numbered 0 to 16,383. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. All data words and addresses in the following format are coded in hexadecimal numbers. In coding all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least significant bit and Q8 the most significant bit. For addresses, A0 is least significant bit and A13 is the most significant.

The input media containing the programming data can be in the form of EPROMs, cards, or data formatted in card images (contact TI for details).

Either 16K, 32K, or 64K EPROMs can be used or any combination of them.

The following is a description of how the cards/card images must be formatted, should they be used instead of EPROMs.

INPUT CARD FORMAT

Each code deck submitted by customer shall consist of the following:

1. Title Card
2. Comment Cards
3. Start of Data Card
4. Data Cards

The cards shall be standard 80 column cards with the information in the following format:

TITLE CARD

Card Column	Information
1 – 5	The word 'TITLE' shall be punched in these columns.
6	Blank.
7, 8	The letters 'ZA' shall be punched in these columns.
9 – 15	ZA Number.
16	Blank.
17 – 30	Customer's Part Number, if required (left justifed)
31	Blank.
32	Customer's Part Number to be included as part of device symbolization. Options: Y = Yes N = No
33	Blank.
34 – 35	28
36	Blank.
37	Type of Package Options: C = ceramic P = plastic

38	Blank.
39	Customer defined option for device mode pin 20 Options: P = power down C = chip select
40	Customer defined option for device mode Options: S = standard ROM B = bank select ROM
41	Logic level for pin 20 Options: 1 = power down or chip select high 0 = power down or chip select low
42	Logic level for pin 22 Options: 1 = chip select enable high 0 = chip select enable low
43	Logic level for pin 27 Options: 1 = bank select enable high 0 = bank select enable low
44	Logic level for pin 26 bank select (1) mode Options: Blank = standard ROM no bank select (A13) 1 = bank select enable high 0 = bank select enable low
45	Logic level for pin 1 bank select (2) mode Options: Blank = standard ROM no bank select (NC) 1 = bank select enable high 0 = bank select enable low Pin 1 selects high order addresses.
46	Blank.
47 – 52	Texas Instruments Device Series (i.e., 47256, 47128) (left justified)

COMMENT CARDS

Any number of comment cards may be used for specifying the customer's name, individual to contact, telephone number, address, any special instructions, etc. The format for these cards is as follows: The letter 'C' (for comment) must be punched in column 1, columns 2 – 4 must be blank, and comments can be punched in columns 5 – 80.

START OF DATA CARD

This card is to identify that the next card will be the beginning of customer's code. Format is as follows; Columns 1 – 4 must have '&ROM' punched in them. The remainder of card is blank.

DATA CARDS

There will be 512 data cards supplied for each customer code. Each card will contain (in hexadecimal) the data for 32 memory locations. Each data card shall be in the following format:

Card Column	Information
1 – 4	Hexadecimal address of first word on the card, four bits in length.
5, 6	Blank.
7 – 70	Data. Each 8-bit data byte is represented by two ASCII characters to represent a hexadecimal value of '00' to 'FF'.
71, 72	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from columns 1 to 70, evaluate modulo 256 (carry from high order bit ignored). For purposes of calculating the checksum, the value of columns 5 and 6 are defined to be zero. Adding together, modulo 256, all 8-bit bytes from column 1 to 70 (columns 5 and 6 = 0), then adding the checksum, results in zero.
73 – 76	Blank.
77 – 80	Card sequence number, in decimal (right justified).

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS47256
32,768-WORD BY 8-BIT READ-ONLY MEMORY

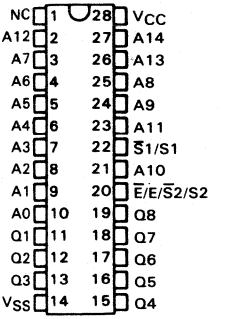
JUNE 1983

- **32,768 X 8 Organization**
- **Fully Static (No clocks, No Refresh)**
- **All Inputs and Outputs TTL Compatible**
- **Single 5-V Power Supply**
- **Optional Power Down or Chip Select**
- **64K Bank Select Option**
- **Maximum Access Time from Address or Power Down:**

TMS47256-25	250 ns
TMS47256-35	350 ns
TMS47256-45	450 ns

- **Worst Case Active Power Dissipation . . . 330 mW**
- **Worst Case Standby Power Dissipation . . . 66 mW**

TMS47256 . . . JL OR NL PACKAGE†
STANDARD ROM
(TOP VIEW)



† The package for the bank select ROM is shown on page 2.

description

The TMS47256 is a 262,144-bit read-only memory organized as 32,768 words of 8-bit length. This makes the TMS47256 ideal for microprocessor based systems. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with bipolar circuits.

There are two versions of the TMS47256: the standard ROM with options on chip selects and power down, and the bank select ROM with similar options. The operation section of this data sheet describes both versions.

PIN NOMENCLATURE STANDARD ROM	
A0-A14	Addresses
Ē/E/S̄2/S2	Chip Enable/Power Down or Chip Select
NC	No Connection
Q1-Q8	Data Out
S̄1/S1	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground

The TMS47256 is fully compatible with Series 74, 74S, or 74LS TTL. The data outputs are three-state for OR-tieing multiple devices on a common bus. Pins 20 and 22 are mask-programmable, providing additional system flexibility. The data is always available, it is not dependent on external clocking of pins 20 and 22.

The TMS47256 is designed for high-density fixed-memory applications such as logic function generation and microprogramming. It is pin compatible with TI's full line of ROMs and EPROMs.

This ROM is supplied in 28-pin dual-in-line plastic (NL suffix) or ceramic (JL suffix) packages designed for insertion in mounting-hole rows on 600 mil centers. The device is designed for operation from 0°C to 70°C.

operation, standard ROM

address (A0-A14)

The address-valid interval determines the device cycle time. The 15-bit positive-logic address is decoded on-chip to select one of 32,768 words of 8-bit length in the memory array. A0 is the least-significant bit and A14 the most-significant bit of the word address.

chip select (S̄1 or S1)

Pin 22 can be programmed during mask fabrication to be active with either a high- or low-level input. When the signal

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on both pins 22 and 20 are active, all eight outputs are enabled; and the eight-bit addressed word can be read. When the signal on either pin 22 or 20 is not active, all eight outputs are in a high-impedance state.

power down ($\overline{E}$ or E) or chip select ($\overline{S2}$ or S2)

Pin 20 can be programmed during mask fabrication to be a chip-enable/power-down pin ($\overline{E}$ or E) or a secondary chip-select pin ($\overline{S2}$ or S2). Each option can be active-high or active-low. When the chip-enable/power-down pin is inactive, the chip is put into the standby mode. This reduces I_{CC1}, which in the active state is 60 mA, to a standby I_{CC2} of 12 mA. With the chip-select option, pin 20 is functionally identical to pin 22.

data out (Q1-Q8)

The eight outputs must be enabled by pins 20 and 22 before the output word can be read. Data will remain valid until the address is changed or the outputs are disabled (chip deselected). When disabled, the three-state outputs are in a high-impedance state. Q1 is considered the least-significant bit, Q8 the most-significant bit.

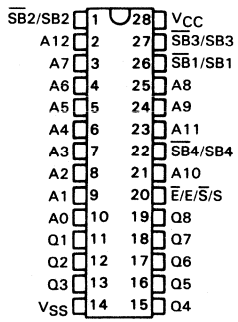
operation, bank select ROM option

Pins 26 ($\overline{SB1}$ or SB1), 1 ($\overline{SB2}$ or SB2), 27 ($\overline{SB3}$ or SB3), and 22 ($\overline{SB4}$ or SB4) can be programmed during mask fabrication to select any one of four 64K banks. When this option is selected, A0 through A12 address an 8K × 8 word bank. The bank select pins can be either active high or active low with SB1, SB2, SB3, and SB4 selecting banks one, two, three, and four, respectively. Bank one represents the least-significant 64K bank and bank four represents the most-significant bank. All bank select pins in the inactive state or more than one bank select pin active will drive all outputs to the high-impedance state.

The chip-select and power-down options previously described for the standard ROM differ only slightly for the bank select ROM version; the only difference being that there are two possible chip selects for the standard ROM while only one chip select is available for the bank select ROM. Data out functions the same for both versions.

Bank select input level specifications are identical to the input level specifications of the standard ROM.

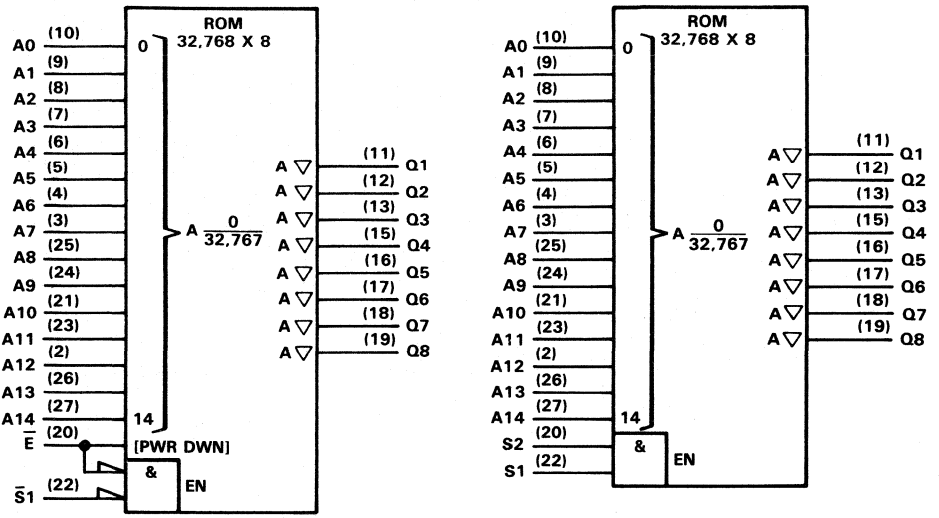
TMS47256 . . . JL OR NL PACKAGE
BANK SELECT ROM
(TOP VIEW)



PIN NOMENCLATURE BANK SELECT ROM	
A0-A12	Addresses
$\overline{E}$/E/$\overline{S}$/S	Chip Enable/Power Down or Chip Select
Q1-Q8	Data Out
$\overline{SB1}$/SB1, $\overline{SB2}$/SB2, $\overline{SB3}$/SB3, $\overline{SB4}$/SB4	Bank Selects
V_{CC}	+5-V Supply
V_{SS}	Ground

logic symbols†

STANDARD ROMS

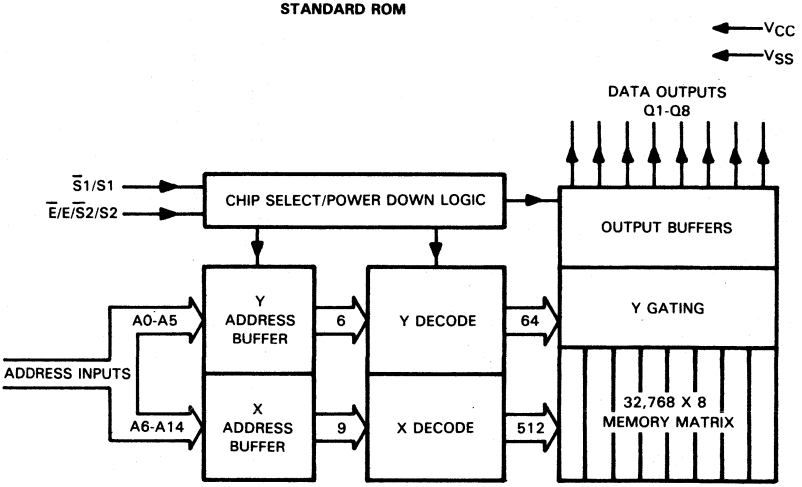


Pins 20 and 22 can be active-low as shown in the symbol on the left or active-high as shown in the symbol on the right. In addition, pin 20 can be either a secondary chip select (S2 or $\overline{S2}$) or a chip enable/power down (E or $\overline{E}$).

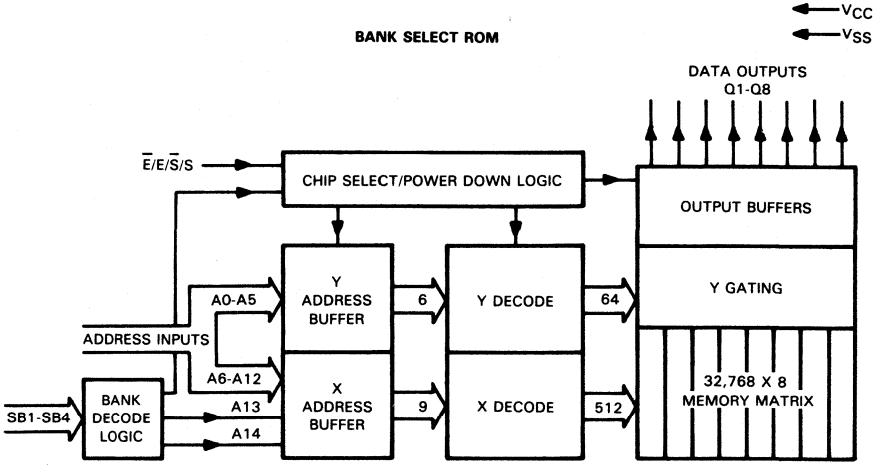
†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

functional block diagrams

STANDARD ROM



BANK SELECT ROM



absolute maximum ratings

Supply voltage to ground potential (see Note 1)	−0.5 V to 7 V
Applied output voltage (see Note 1)	−1 V to 7 V
Applied input voltage (see Note 1)	−1 V to 7 V
Power dissipation	500 mW
Operating free-air temperature	0°C to 70°C
Storage temperature	−55°C to 150°C

NOTE 1: Voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics, T_A = 0°C to 70°C, V_{DD} = 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V,	I_{OL} = 2.1 mA		0.4	V
I_I	Input current	V_{CC} 5.5 V,	$0_V \le V_{IN} \le 5.5$ V		10	μA
I_O	Output leakage current	V_O = 0.4 V to V_{CC},	Chip deselected		±10	μA
I_{CC1}	Supply current from V_{CC} (active)	V_{CC} = 5.5 V,	$V_I = V_{CC}$ Output not loaded		60	mA
I_{CC2}	Supply current from V_{CC} (power down)	V_{CC} = 5.5 V			12	mA
C_i	Input capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	T_A = 25°C,		12	pF

switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5 V ±10%, see figure 1†

PARAMETER		TMS47256-25		TMS47256-35		TMS47256-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(AD)}$	Access time from address		250		350		450	ns
$t_{a(S)}$	Access time from chip select		120		120		120	
$t_{a(PD)}$	Access time from power down/chip enable		250		350		450	
$t_{v(A)}$	Output data valid after address change	10		10		10		
t_{dis}	Output disable time from chip select/chip enable		100		100		100	
$t_{en(S)}$	Output enable time from chip select	10		10		10		
$t_{en(E)}$	Output enable time from chip enable	10		10		10		

† All AC measurements are made at 10% and 90% points.

64K bank decode switching characteristics†

PARAMETER		TMS47256-25		TMS47256-35		TMS47256-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(SB)}$	Access time from bank select		250		350		450	ns
$t_{en(SB)}$	Output enable time from bank select	10		10		10		
$t_{dis(SB)}$	Output disable time from bank select		100		100		100	

† Previously defined switching characteristics remain unchanged.

PARAMETER MEASUREMENT INFORMATION

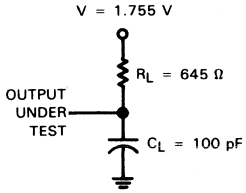
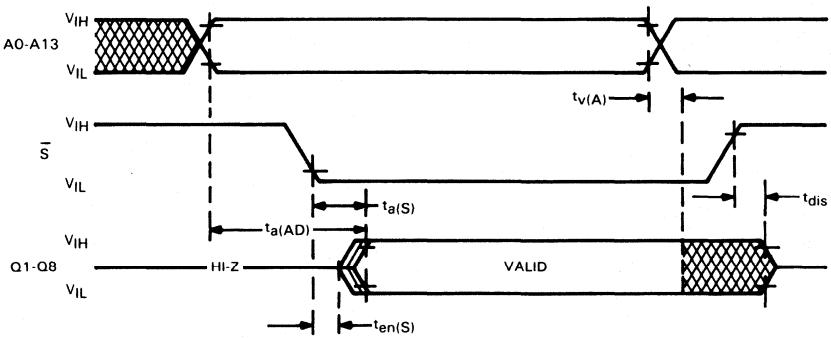
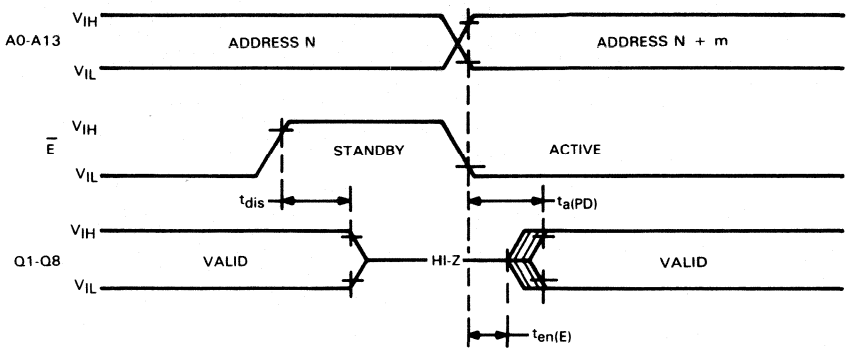


FIGURE 1 – LOAD CIRCUIT

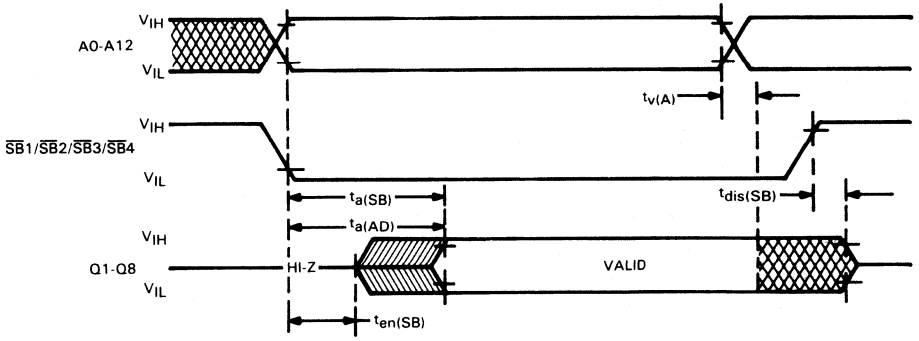
read cycle timing



standby mode



64K bank select mode read cycle timing



PROGRAMMING DATA

PROGRAMMING REQUIREMENTS: The TMS47256 is a fixed program memory in which the programming is performed by TI at the factory during the manufacturing cycle to the specific customer inputs supplied in the format below. The device is organized as 16,384 8-bit words with address locations numbered 0 to 32,767. The 8-bit words can be coded as a 2-digit hexadecimal number between 00 and FF. All data words and addresses in the following format are coded in hexadecimal numbers. In coding all binary words must be in positive logic before conversion to hexadecimal. Q1 is considered the least significant bit and Q8 the most significant bit. For addresses, A0 is least significant bit and A14 is the most significant.

The input media containing the programming data can be in the form of EPROMs, cards, or data formatted in card images (contact TI for details).

Either 16K, 32K, or 64K EPROMs can be used or any combination of them.

The following is a description of how the cards/card images must be formatted, should they be used instead of EPROMs.

INPUT CARD FORMAT

Each code deck submitted by customer shall consist of the following:

1. Title Card
2. Comment Cards
3. Start of Data Card
4. Data Cards

The cards shall be standard 80 column cards with the information in the following format:

TITLE CARD

Card Column	Information
1 – 5	The word 'TITLE' shall be punched in these columns.
6	Blank.
7, 8	The letters 'ZA' shall be punched in these columns.
9 – 14	ZA Number.
15	Blank.
16 – 30	Customer's Part Number, if required (left justifed)
31	Blank.
32	Customer's Part Number to be included as part of device symbolization. Options: Y = Yes N = No
33	Blank.
34 – 35	28
36	Blank.
37	Type of Package Options: C = ceramic P = plastic

38	Blank.
39	Customer defined option for device mode pin 20 Options: P = power down C = chip select
40	Customer defined option for device mode Options: S = standard ROM B = bank select ROM
41	Logic level for pin 20 Options: 1 = power down or chip select high 0 = power down or chip select low
42	Logic level for pin 22 chip select or bank select (4) mode Options: Blank = standard ROM no bank select (chip select) 1 = chip select enable high or bank select enable high 0 = chip select enable low or bank select enable low
43	Logic level for pin 27 bank select (3) mode Options: Blank = standard ROM no bank select (A14) 1 = bank select enable high 0 = bank select enable low
44	Logic level for pin 26 bank select (1) mode Options: Blank = standard ROM no bank select (A13) 1 = bank select enable high 0 = bank select enable low
45	Logic level for pin 1 bank select (2) mode Options: Blank = standard ROM no bank select (NC) 1 = bank select enable high 0 = bank select enable low Pin 1 selects high order addresses.
46	Blank.
47 – 52	Texas Instruments Device (i.e., 47256, 47128) (left justified)

COMMENT CARDS

Any number of comment cards may be used for specifying the customer's name, individual to contact, telephone number, address, any special instructions, etc. The format for these cards is as follows: The letter 'C' (for comment) must be punched in column 1, columns 2 – 4 must be blank, and comments can be punched in columns 5 – 80.

START OF DATA CARD

This card is to identify that the next card will be the beginning of customer's code. Format is as follows; Columns 1 – 4 must have '&ROM' punched in them. The remainder of card is blank.

DATA CARDS

There will be 1024 data cards supplied for each customer code. Each card will contain (in hexadecimal) the data for 32 memory locations. Each data card shall be in the following format:

Card Column	Information
1 – 4	Hexadecimal address of first word on the card, four bits in length.
5, 6	Blank.
7 – 70	Data. Each 8-bit data byte is represented by two ASCII characters to represent a hexadecimal value of '00' to 'FF'.
71, 72	Checksum. The checksum is the negative of the sum of all 8-bit bytes in the record from columns 1 to 70, evaluate modulo 256 (carry from high order bit ignored). For purposes of calculating the checksum, the value of columns 5 and 6 are defined to be zero. Adding together, modulo 256, all 8-bit bytes from column 1 to 70 (columns 5 and 6 = 0), then adding the checksum, results in zero.
73 – 76	Blank.
77 – 80	Card sequence number, in decimal (right justified).

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

ATTENTION

These devices contain circuits to protect the inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

Unused inputs must always be connected to an appropriate logic voltage level, preferably either supply voltage or ground.

Additional information concerning the handling of ESD sensitive devices is available from Texas Instruments in a document entitled *"Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies."*

Please contact

Texas Instruments
P.O. Box 401560
Dallas, Texas 75240

to obtain this brochure.

TMS2114, TMS2114L
1024-WORD BY 4-BIT STATIC RAMS

DECEMBER 1979 – REVISED AUGUST 1983

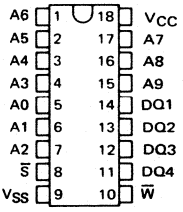
- Previously Called TMS4045/TMS40L45
- 1024 X 4 Organization
- Single +5-V Supply
- High Density 300-mil (7.62 mm) 18-Pin Package
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- 4 Performance Ranges:

	ACCESS READ OR WRITE TIME (MAX)	CYCLE (MIN)
TMS2114-15, TMS2114L-15	150 ns	150 ns
TMS2114-20, TMS2114L-20	200 ns	200 ns
TMS2114-25, TMS2114L-25	250 ns	250 ns
TMS2114-45, TMS2114L-45	450 ns	450 ns

- 400-mV Guaranteed DC Noise Immunity with Standard TTL Loads – No Pull-Up Resistors Required
- Common I/O Capability
- 3-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 2 Series 74, 1 Series 74S, or 8 Series 74LS TTL Loads
- Low Power Dissipation

	MAX (OPERATING)
TMS2114	550 mW
TMS2114L	330 mW

TMS2114, TMS2114L . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A9	Addresses
DQ1 – DQ4	Data In/Data Out
$\overline{S}$	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

This series of static random-access memories is organized as 1024 words of 4 bits each. Static design results in reducing overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74, 74S or 74LS TTL. No pull-up resistors are required. This 4K Static RAM series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship.

The TMS2114/2114L series is offered in the 18-pin dual-in-line plastic (NL suffix) package designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers. The series is guaranteed for operation from 0°C to 70°C.

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operation

addresses (A0 – A9)

The ten address inputs select one of the 1024 4-bit words in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip select ($\overline{S}$)

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in and data-out terminals. When chip select is at a logic low level, both terminals are enabled. When chip select is high, data-in is inhibited and data-out is in the floating or high-impedance state.

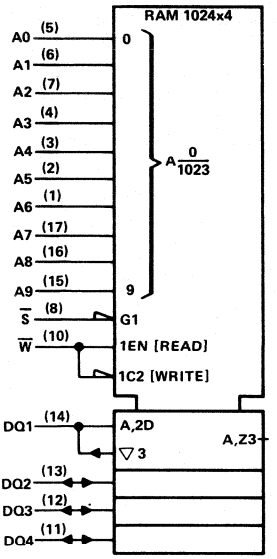
write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{S}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in/data-out (DQ1 – DQ4)

Data can be written into a selected device when the write enable input is low. The DQ terminal can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates, one Series 74S TTL gate, or eight Series 74LS TTL gates. The DQ terminals are in the high-impedance state when chip select ($\overline{S}$) is high or whenever a write operation is being performed. Data-out is the same polarity as data-in.

logic symbol†



FUNCTION TABLE

$\overline{W}$	$\overline{S}$	DQ1 – DQ4	MODE
L	L	VALID DATA	WRITE
H	L	DATA OUTPUT	READ
X	H	HI-Z	DEVICE DISABLED

†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage (any input) (see Note 1) . . . . . −1 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the ground material.

recommended operating conditions

PARAMETER	TMS2114 TMS2114L			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL} (see Note 2)	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minium, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{OH}	High-level voltage	I_{OH} = −1 mA	V_{CC} = MIN (operating)		2.4			V
V_{OL}	Low-level voltage	I_{OL} = 3.2 mA	V_{CC} = MIN (operating)				0.4	V
I_I	Input current	V_I = 0 V to MAX					10	μA
I_{OZ}	Off-state output current	$\overline{S}$ at 2 V or $\overline{W}$ at 0.8 V	V_O = 0 V to MAX				±10	μA
I_{CC}	Supply current from V_{CC}	I_O = 0 mA, T_A = 0°C (worst case)	TMS 2114	V_{CC} = MAX		90	100	mA
			TMS 2114L	V_{CC} = MAX		50	60	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz					8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz					8	pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

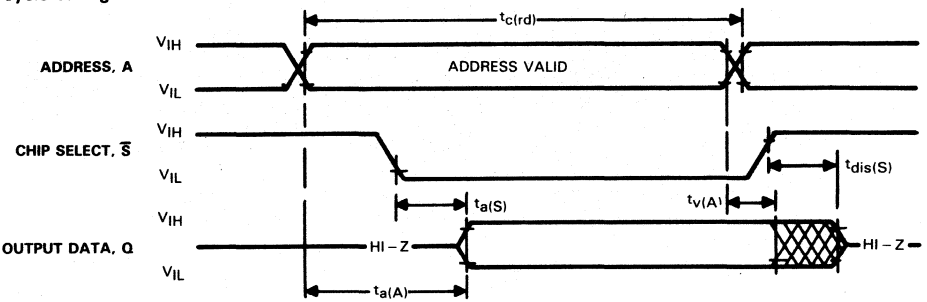
timing requirements over recommended supply voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

PARAMETER		TMS2114-15 TMS2114L-15		TMS2114-20 TMS2114L-20		TMS2114-25 TMS2114L-25		TMS2114-45 TMS2114L-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	150		200		250		450		ns
$t_{c(wr)}$	Write cycle time	150		200		250		450		ns
$t_{w(W)}$	Write pulse width	80		100		100		200		ns
$t_{su(A)}$	Address set up time	0		0		0		0		ns
$t_{su(S)}$	Chip select set up time	80		100		100		200		ns
$t_{su(D)}$	Data set up time	80		100		100		200		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{h(A)}$	Address hold time	0		0		0		20		ns

switching characteristics over recommended voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

PARAMETER		TMS2114-15 TMS2114L-15		TMS2114-20 TMS2114L-20		TMS2114-25 TMS2114L-25		TMS2114-45 TMS2114L-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250		450	ns
$t_{a(S)}$	Access time from chip select (or output enable) low		70		85		100		120	ns
$t_{a(W)}$	Access time from write enable high		70		85		100		120	ns
$t_{v(A)}$	Output data valid after address change	20		20		20		20		ns
$t_{dis(S)}$	Output disable time after chip select (or output enable) high		50		60		60		100	ns
$t_{dis(W)}$	Output disable time after write enable low		50		60		60		100	ns

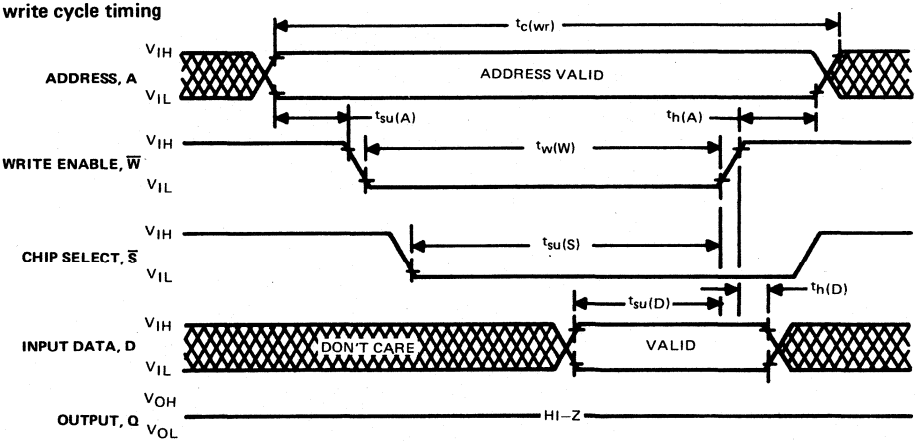
read cycle timing†



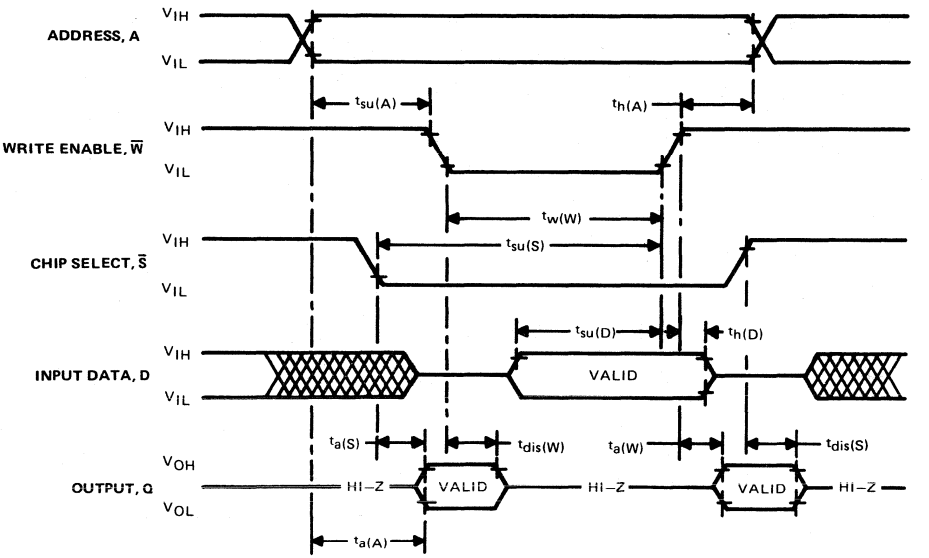
All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times equal 10 nanoseconds.

†Write enable is high for a read cycle.

early write cycle timing



read-write cycle timing



TYPICAL APPLICATION DATA

Early write cycle avoids DQ conflicts by controlling the write time with $\overline{S}$. On the diagram above, the write operation will be controlled by the leading edge of $\overline{S}$, not $\overline{W}$. Data can only be written when both $\overline{S}$ and $\overline{W}$ are low. Either $\overline{S}$ or $\overline{W}$ being high inhibits the write operation. To prevent erroneous data being written into the array, the addresses must be stable during the write cycle as defined by $t_{su(A)}$, $t_{w(W)}$, and $t_{h(A)}$.

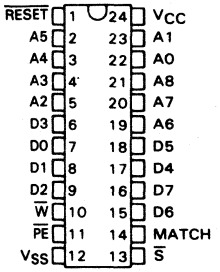
Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS2150
CACHE ADDRESS COMPARATOR

MARCH 1982 – REVISED SEPTEMBER 1983

- **Fast Address to Match Valid Delay – Two Speed Ranges: 45 ns, 55 ns**
- **512 X 9 Internal RAM**
- **300-Mil 24-Pin Ceramic Side Brazed Package**
- **Max Power Dissipation: 660 mW**
- **On-Chip Parity Generation and Checking**
- **Parity Error Output/Force Parity Error Input**
- **On-Chip Address/Data Comparator**
- **Asynchronous, Single-Cycle Reset**
- **Easily Expandable**
- **Fully Static, TTL Compatible**
- **Reliable SMOS (Scaled NMOS) Technology**

TMS2150 . . . JDL PACKAGE
(TOP VIEW)



description

The 8-bit-slice cache address comparator consists of a high-speed 512 X 9 static RAM array, parity generator, and parity checker, and 9-bit high-speed comparator. It is fabricated using N-channel silicon gate technology for high speed and simple interface with MOS and bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by a high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tieing. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A $\overline{RESET}$ input is provided for initialization. When $\overline{RESET}$ goes low, all 512 X 9 RAM locations will be cleared and the MATCH output will be forced high.

The cache address comparator operates from a single +5 V supply and is offered in a 24-pin 300-mil side brazed package. The device is fully TTL compatible and is guaranteed to operate from 0°C to 70°C.

MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{RESET} = V_{IL}$,
or: $\overline{S} = V_{IH}$,
or: $\overline{W} = V_{IL}$

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity, with $\overline{RESET} = V_{IH}$, $\overline{S} = V_{IL}$, and $\overline{W} = V_{IH}$

FUNCTION TABLE

OUTPUT		FUNCTION
MATCH	$\overline{PE}$	DESCRIPTION
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where $\overline{S} = V_{IL}$, $\overline{W} = V_{IH}$, $\overline{RESET} = V_{IH}$

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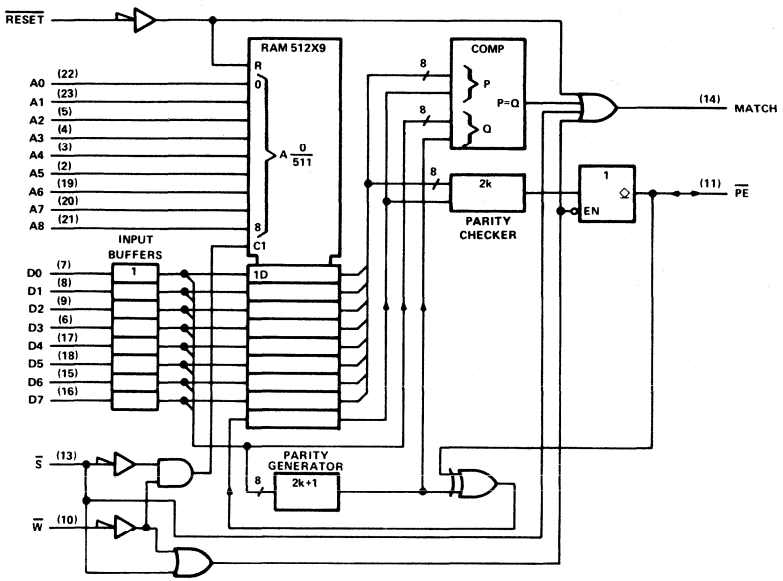
functional block diagram (positive logic)



PIN FUNCTION	DESCRIPTION
A0-A8, Address Inputs	Address 1 of 512-by-9-bit random-access memory locations.
D0-D7, Data Inputs	Compared with memory location addressed by A0-A8 when $\overline{W}$ = V_{IH} and $\overline{S}$ = V_{IL}. Provides input data to RAM when $\overline{W}$ = V_{IL} and $\overline{S}$ = V_{IL}.
$\overline{RESET}$, Input	Asynchronously clears entire RAM array and forces MATCH high when $\overline{RESET}$ = V_{IL} and $\overline{W}$ = V_{IH}.
$\overline{S}$, Chip Select Input	Enables device when $\overline{S}$ = V_{IL}. Deselects device and forces MATCH high when $\overline{S}$ = V_{IH}.
$\overline{W}$, Write Control Input	Writes D0-D7 + generated parity into RAM and forces MATCH high when $\overline{W}$ = V_{IL} with $\overline{S}$ = V_{IL}. Places selected device in compare mode if $\overline{W}$ = V_{IH}.
$\overline{PE}$, Parity Error Input/Output	During write cycles $\overline{PE}$ can force a parity error into the 9-bit location specified by A0-A8 when $\overline{PE}$ = V_{IL}. For compare cycles, $\overline{PE}$ = V_{OL} indicates a parity error in the stored data. $\overline{PE}$ is an open-drain output so an external pull-up resistor is required.
MATCH, Output	When MATCH = V_{OH} during a compare cycle, D0-D7 + parity equal the contents of the 9-bit memory location addressed by A0-A8.
V_{SS}	Circuit GND potential.
V_{CC}	+5 V circuit power supply.

absolute maximum ratings over operating free-air temperature range (unless otherwise specified)

Supply voltage range, V_{CC} (see Note 1) . . . . . −1.5 V to 7 V
Input voltage range, any input . . . . . −1.5 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2		6	V
Low-level input voltage, V_{IL} (See Note 2)	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS2150-4			TMS2150-5			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH(M)}$	MATCH high-level output voltage	I_{OH} = −2 mA, V_{CC} = 4.5 V	2.4			2.4			V
$V_{OL(M)}$	MATCH low-level output voltage	I_{OL} = 4 mA, V_{CC} = 4.5 V			0.4			0.4	V
$V_{OL(PE)}$	$\overline{PE}$ low-level output voltage	I_{OL} = 12 mA, V_{CC} = 4.5 V			0.4			0.4	V
I_I	Input current	V_I = 0 V to 5.5 V			10			10	μA
$I_{OL(PE)}$	$\overline{PE}$ output sink current	V_{OL} = 0.4 V, V_{CC} = 4.5 V	12			12			mA
I_{OS}	Short-circuit MATCH output current	V_{CC} = 5.5 V, V_O = GND			−150			−150	mA
I_{CC1}	Supply current (operative)	$\overline{RESET}$ = V_{IH}		95	135		85	128	mA
I_{CC2}	Supply current (reset)	$\overline{RESET}$ = V_{IL}		115	145		110	140	mA
C_i	Input capacitance	V_I = 0 V, f = 1 MHz			5			5	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz			6			6	pF

ac test conditions

Input pulse levels . . . . . GND to 3 V
Input rise and fall times . . . . . 5 ns
Input timing reference levels . . . . . 1.5 V
Output timing reference level . . . . . 1.5 V
Output loading . . . . . See Figures 1A and 1B

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS2150-4		TMS2150-5		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address to MATCH		45		55	ns
$t_{a(A\text{-}P)}$	Access time from address to $\overline{PE}$		55		65	ns
$t_{a(S)}$	Access time from $\overline{S}$ to MATCH		25		35	ns
$t_{p(D)}$	Propagation time, data inputs to MATCH		35		45	ns
$t_{p(R\text{-}MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		30		40	ns
$t_{p(S\text{-}MH)}$	Propagation time, $\overline{S}$ high to MATCH high		30		40	ns
$t_{p(W\text{-}MH)}$	Propagation time, $\overline{W}$ low to MATCH high		25		35	ns
$t_{p(W\text{-}PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		25		35	ns
$t_{v(A)}$	MATCH valid time after change of address	5		5		ns
$t_{v(A\text{-}P)}$	$\overline{PE}$ valid time after change of address	15		15		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS2150-4		TMS2150-5		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time	45		55		ns
$t_{c(rd)}$	Read cycle time	45		55		ns
$t_{w(RL)}$	Pulse duration, $\overline{RESET}$ low	35		45		ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low	30		35		ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	25		30		ns
$t_{su(P)}$	PE setup time before $\overline{W}$ high	25		30		ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	25		35		ns
$t_{su(RH)}$	$\overline{RESET}$ inactive setup time before first tag cycle	0		0		ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0		5		ns
$t_{h(D)}$	Data hold time after $\overline{W}$ high	5		10		ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	0		5		ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0		0		ns
t_{AVWH}	Address valid to write enable	45		50		ns

PARAMETER MEASUREMENT INFORMATION

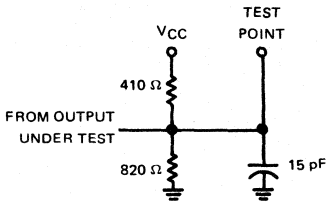


FIGURE 1A – $\overline{PE}$ OUTPUT LOAD CIRCUIT

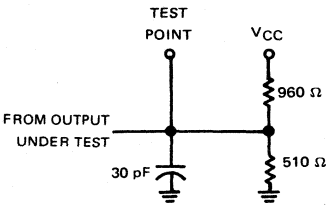
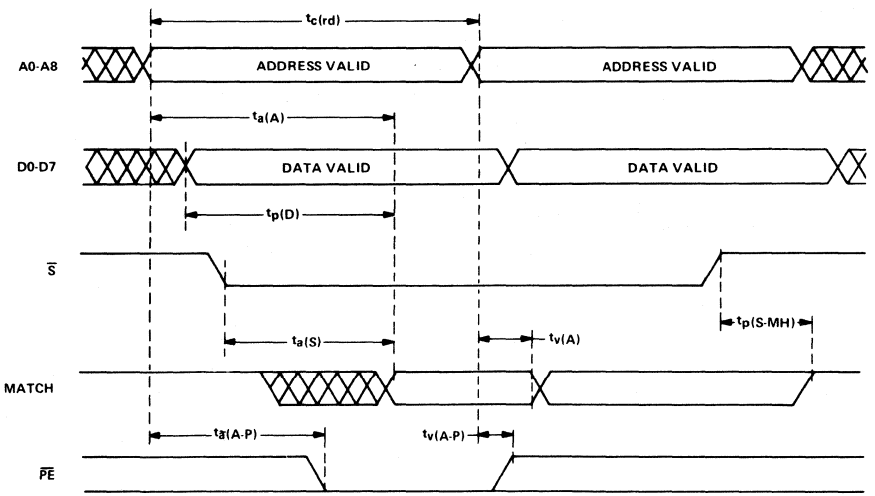


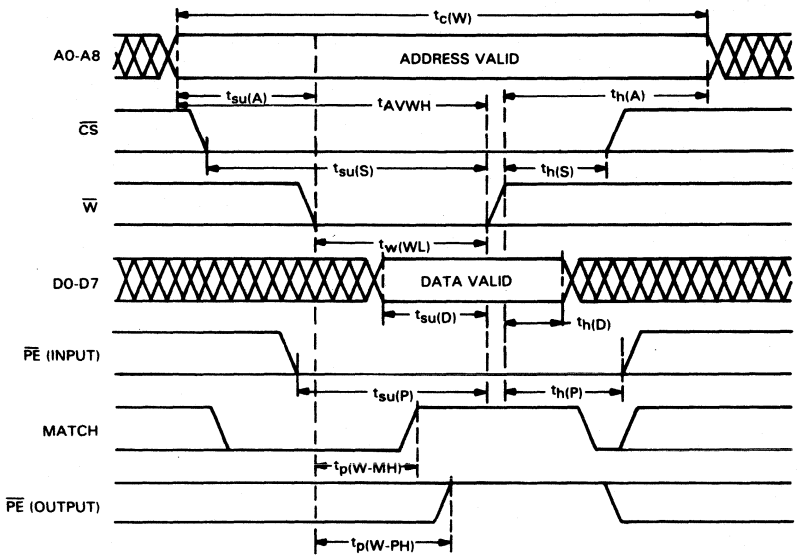
FIGURE 1B – MATCH OUTPUT LOAD CIRCUIT

compare cycle timing

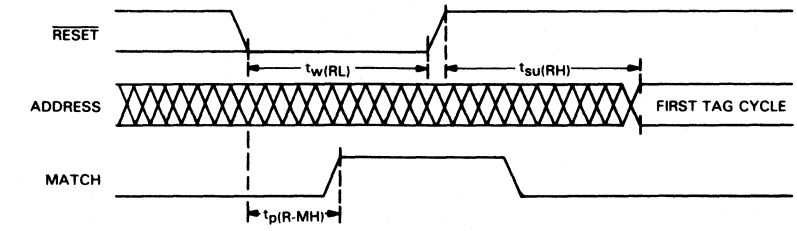


NOTE: Input pulse levels are 0 V and 3 V, with rise and fall times of 5 ns. The timing reference levels on the input pulses are 0.8 V and 2.0 V. The timing reference level for output pulses is 1.5 V. See Figures 1A and 1B for output loading.

write cycle timing



reset cycle timing



NOTE: Input pulse levels are 0 V and 3 V, with rise and fall times of 5 ns. The timing reference levels on the input pulses are 0.8 V and 2.0 V. The timing reference level for output pulses is 1.5 V. See Figures 1A and 1B for output loading.

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

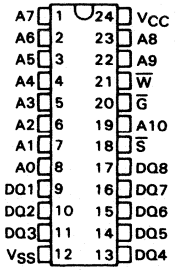
TMS4016
2048-WORD BY 8-BIT STATIC RAM

FEBRUARY 1981 – REVISED AUGUST 1983

- **2K X 8 Organization, Common I/O**
- **Single +5-V Supply**
- **Fully Static Operation (No Clocks, No Refresh)**
- **JEDEC Standard Pinout**
- **24-Pin 600 Mil (15.2 mm) Package Configuration**
- **Plug-in Compatible with 16K 5 V EPROMs**
- **8-Bit Output for Use in Microprocessor-Based Systems**
- **3-State Outputs with $\overline{S}$ for OR-ties**
- **$\overline{G}$ Eliminates Need for External Bus Buffers**
- **All Inputs and Outputs Fully TTL Compatible**
- **Fanout to Series 74, Series 74S or Series 74LS TTL Loads**
- **N-Channel Silicon-Gate Technology**
- **Power Dissipation Under 385 mW Max**
- **Guaranteed dc Noise Immunity of 400 mV with Standard TTL Loads**
- **4 Performance Ranges:**

	ACCESS TIME (MAX)
TMS4016-12	120 ns
TMS4016-15	150 ns
TMS4016-20	200 ns
TMS4016-25	250 ns

TMS4016 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A10	Addresses
DQ1 – DQ8	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{S}$	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TMS4016 static random-access memory is organized as 2048 words of 8 bits each. Fabricated using proven N-channel, silicon-gate MOS technology, the TMS4016 operates at high speeds and draws less power per bit than 4K static RAMs. It is fully compatible with Series 74, 74S, or 74LS TTL. Its static design means that no refresh clocking circuitry is needed and timing requirements are simplified. Access time is equal to cycle time. A chip select control is provided for controlling the flow of data-in and data-out and an output enable function is included in order to eliminate the need for external bus buffers.

Of special importance is that the TMS4016 static RAM has the same standardized pinout as TI's compatible EPROM family. This, along with other compatible features, makes the TMS4016 plug-in compatible with the TMS2516 (or other 16K 5 V EPROMs). Minimal, if any modifications are needed. This allows the microprocessor system designer complete flexibility in partitioning his memory board between read/write and non-volatile storage.

The TMS4016 is offered in the plastic (NL suffix) 24-pin dual-in-line package designed for insertion in mounting hole rows on 600-mil (15.2 mm) centers. It is guaranteed for operation from 0°C to 70°C.

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operation

addresses (A0 – A10)

The eleven address inputs select one of the 2048 8-bit words in the RAM. The address-inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

output enable ($\overline{G}$)

The output enable terminal, which can be driven directly from standard TTL circuits, affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

chip select ($\overline{S}$)

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in/data-out terminals. When chip select and output enable are at a logic low level, the D/Q terminals are enabled. When chip select is high, the D/Q terminals are in the floating or high-impedance state and the input is inhibited.

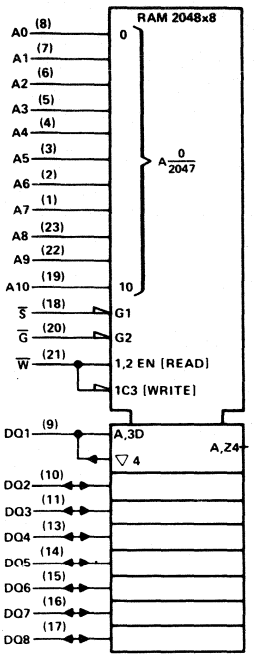
write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in/data-out (DQ1 – DQ8)

Data can be written into a selected device when the write enable input is low. The D/Q terminal can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fan-out of one Series 74 TTL gate, one Series 74S TTL gate, or five Series 74LS TTL gates. The D/Q terminals are in the high impedance state when chip select ($\overline{S}$) is high, output enable ($\overline{G}$) is high, or whenever a write operation is being performed. Data-out is the same polarity as data-in.

logic symbol†



FUNCTION TABLE

$\overline{W}$	$\overline{S}$	$\overline{G}$	DQ1-DQ8	MODE
L	L	X	VALID DATA	WRITE
H	L	L	DATA OUTPUT	READ
X	H	X	HI-Z	DEVICE DISABLED
H	L	H	HI-Z	OUTPUT DISABLED

† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage (any input) (see Note 1) . . . . . −1 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the V_{SS} terminal.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL} (see Note 2)	1		0.8	V
Operating free-air temperature, T_A	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High level voltage	$I_{OH} = -1$ mA,	$V_{CC} = 4.5$ V	2.4			V
V_{OL}	Low level voltage	$I_{OL} = 2.1$ mA,	$V_{CC} = 4.5$ V			0.4	V
I_I	Input current	$V_I = 0$ V to 5.5 V				10	μA
I_{OZ}	Off-state output current	$\overline{S}$ or $\overline{G}$ at 2 V or $\overline{W}$ at 0.8 V, $V_O = 0$ V to 5.5 V				10	μA
I_{CC}	Supply current from V_{CC}	$I_O = 0$ mA, $T_A = 0°C$ (worst case)	$V_{CC} = 5.5$ V,		40	70	mA
C_i	Input capacitance	$V_I = 0$ V,	$f = 1$ MHz			8	pF
C_o	Output capacitance	$V_O = 0$ V,	$f = 1$ MHz			12	pF

†All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		TMS4016-12		TMS4016-15		TMS4016-20		TMS4016-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	120		150		200		250		ns
$t_{c(wr)}$	Write cycle time	120		150		200		250		ns
$t_{w(W)}$	Write pulse width	60		80		100		120		ns
$t_{su(A)}$	Address setup time	20		20		20		20		ns
$t_{su(S)}$	Chip select setup time	60		80		100		120		ns
$t_{su(D)}$	Data setup time	50		60		80		100		ns
$t_{h(A)}$	Address hold time	0		0		0		0		ns
$t_{h(D)}$	Data hold time	5		10		10		10		ns

switching characteristics over recommended voltage range, T_A = 0°C to 70°C with output loading of Figure 1 (see notes 3 and 4)

PARAMETER		TMS4016-12		TMS4016-15		TMS4016-20		TMS4016-25		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		120		150		200		250	ns
$t_{a(S)}$	Access time from chip select low		60		75		100		120	ns
$t_{a(G)}$	Access time from output enable low		50		60		80		100	ns
$t_{v(A)}$	Output data valid after address change	10		15		15		15		ns
$t_{dis(S)}$	Output disable time after chip select high		40		50		60		80	ns
$t_{dis(G)}$	Output disable time after output enable high		40		50		60		80	ns
$t_{dis(W)}$	Output disable time after write enable low		50		60		60		80	ns
$t_{en(S)}$	Output enable time after chip select low	5		5		10		10		ns
$t_{en(G)}$	Output enable time after output enable low	5		5		10		10		ns
$t_{en(W)}$	Output enable time after write enable high	5		5		10		10		ns

NOTES: 3. $C_L = 100$ pF for all measurements except $t_{dis(W)}$ and $t_{en(W)}$.
$C_L = 5$ pF for $t_{dis(W)}$ and $t_{en(W)}$.
4. t_{dis} and t_{en} parameters are sampled and not 100% tested.

PARAMETER MEASUREMENT INFORMATION

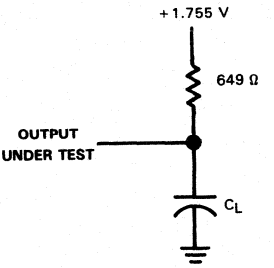
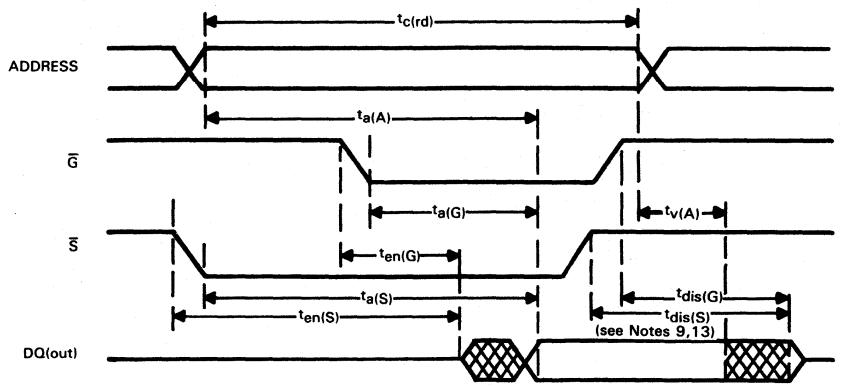


FIGURE 1 – OUTPUT LOAD

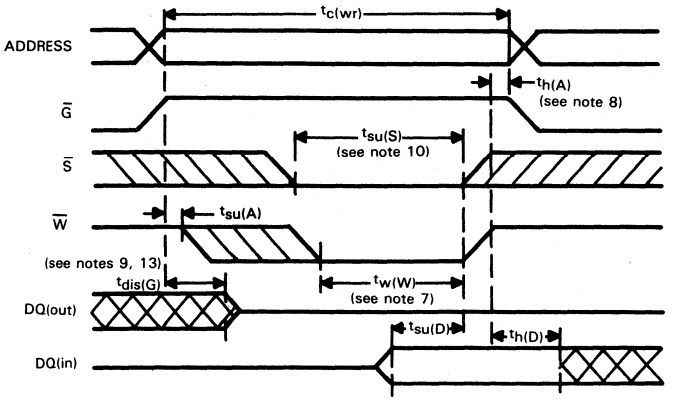
timing waveform of read cycle (see note 5)



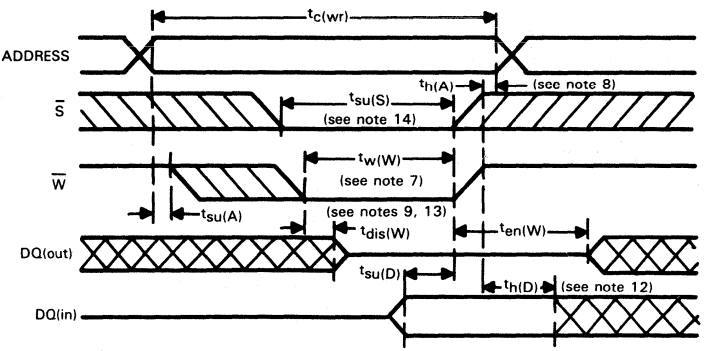
All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times equal 10 ns.

NOTE 5: $\overline{W}$ is high for Read Cycle.

timing waveform of write cycle no. 1 (see note 6)



timing waveform of write cycle no. 2 (see notes 6 and 11)



All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times equal 10 nanoseconds.

NOTES:
6. $\overline{W}$ must be high during all address transitions.
7. A write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.
8. $t_{h(A)}$ is measured from the earlier of $\overline{S}$ or $\overline{W}$ going high to the end of the write cycle.
9. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
10. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, output remains in a high impedance state.
11. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
12. If $\overline{S}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied.
13. Transition is measured ±200 mV from steady-state voltage.
14. If the $\overline{S}$ low transition occurs before the $\overline{W}$ low transition, then the data input signals of opposite phase to the outputs must not be applied for the duration of $t_{dis(W)}$ after the $\overline{W}$ low transition.

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TMS4044, TMS40L44
4096-WORD BY 1-BIT STATIC RAMS

DECEMBER 1977 – REVISED MAY 1982

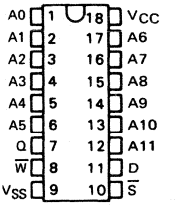
- **Single +5-V Supply (±10% Tolerance)**
- **High Density 300-mil (7.62 mm) 18-Pin Package**
- **Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)**
- **4 Performance Ranges:**

	ACCESS READ OR WRITE TIME (MAX)	CYCLE (MIN)
TMS4044-12, TMS40L44-12	120 ns	120 ns
TMS4044-20, TMS40L44-20	200 ns	200 ns
TMS4044-25, TMS40L44-25	250 ns	250 ns
TMS4044-45, TMS40L44-45	450 ns	450 ns

- **400-mV Guaranteed DC Noise Immunity with Standard TTL Loads – No Pull-Up Resistors Required**
- **Common I/O Capability**
- **3-State Outputs and Chip Select Control for OR-Tie Capability**
- **Fan-Out to 2 Series 74, 1 Series 74S, or 8 Series 74LS TTL Loads**
- **Low Power Dissipation**

	MAX (OPERATING)	MAX (STANDBY)
TMS4044	303 mW	84 mW
TMS40L44	220 mW	60 mW

TMS4044/TMS40L44 . . . NL PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0 – A11	Addresses
D	Data In
Q	Data Out
$\overline{S}$	Chip Select
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

This series of static random-access memories is organized as 4096 words of 1 bit. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74, 74S or 74LS TTL. No pull-up resistors are required. This 4K Static RAM series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. All versions are characterized to retain data at $V_{CC} = 2.4$ V to reduce power dissipation.

The TMS4044/40L44 series is offered in the 18-pin dual-in-line plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers. The series is guaranteed for operation from 0°C to 70°C.

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operation

addresses (A0-A11)

The twelve address inputs select one of the 4096 storage locations in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip select ($\overline{S}$)

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in and data-out terminals. When chip select is at a logic low level, both terminals are enabled. When chip select is high, data-in is inhibited and data-out is in the floating or high-impedance state.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in (D)

Data can be written into a selected device when the write enable input is low. The data-in terminal can be driven directly from standard TTL circuits.

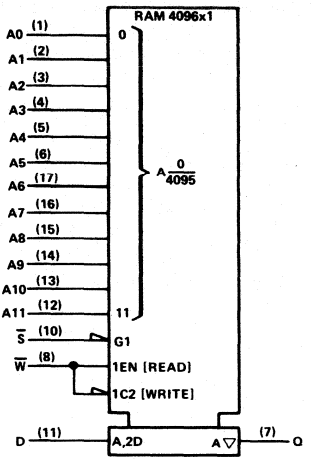
data-out (Q)

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates, one Series 74S TTL gate, or eight Series 74LS TTL gates. The output is in the high-impedance state when chip select ($\overline{S}$) is high or whenever a write operation is being performed, facilitating device operation in common I/O systems. Data-out is the same polarity as data-in.

standby operation

The standby mode, which will retain data while reducing power consumption, is attained by reducing the V_{CC} supply from 5 volts to 2.4 volts. When reducing supply voltage during the standby mode, $\overline{S}$ and $\overline{W}$ must be high to retain data. The V_{CC} transition rate should not exceed 26 mV/ms. During standby operation, data can not be read or written into the memory. When resuming normal operation, five cycle times must be allowed after normal supplies are returned for the memory to resume steady state operation conditions.

logic symbol†



FUNCTION TABLE

INPUTS		OUTPUT	MODE
$\overline{S}$	$\overline{W}$	Q	
H	X	HI-Z	DEVICE DISABLED
L	L	HI-Z	WRITE
L	H	DATA OUT	READ

†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage (any input) (see Note 1) . . . . . −1 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	TMS4044-12	Operating	4.5	5	5.5	V
	TMS40L44-12	Standby	2.4		5.5	
	TMS4044-20	Operating	4.5		5.5	
	TMS40L44-20	Standby	2.4		5.5	
	TMS4044-25 TMS40L44-25	Operating	4.5		5.5	
	TMS40L44-45	Standby	2.4		5.5	
	TMS4044-45	Operating	4.5		5.5	
Supply voltage, V_{SS}				0		V
High-level input voltage, V_{IH}			2		5.5	V
Low-level input voltage, V_{IL} (see Note 2)			−1		0.8	V
Operating free-air temperature, T_A			0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature ranges (unless otherwise noted)

	PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH}=-1.0$ mA	$V_{CC}=4.5$ V		2.4			V
V_{OL}	Low-level output voltage	$I_{OL}=3.2$ mA	$V_{CC}=4.5$ V				0.4	V
I_I	Input current	$V_I=0$ V to 5.5 V					10	μA
I_{OZ}	Off-state output current	$\overline{S}$ at 2 V or $\overline{W}$ at 0.8 V	$V_O=0$ V to 5.5 V				±10	μA
I_{CC}	Supply current from V_{CC}	$I_O=0$ mA, $T_A=0°C$ (worst case)	TMS40L44	$V_{CC}=MAX$		25	40	mA
				$V_{CC}=2.4$ V		15	25	
			TMS4044-12	$V_{CC}=MAX$		50	55	
			TMS4044-20 TMS4044-25	$V_{CC}=2.4$ V		25	35	
			TMS4044-45	$V_{CC}=MAX$		50	55	
C_i	Input capacitance	$V_I=0$ V, f = 1 MHz					8	pF
C_o	Output capacitance	$V_O=0$ V, f = 1 MHz					8	pF

†All typical values are at $V_{CC}=5$ V, $T_A=25°C$.

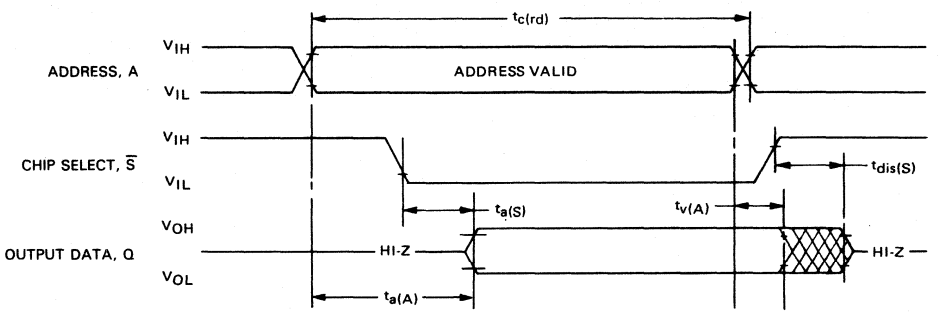
timing requirements over recommended supply voltage range, $T_A=0°C$ to 70°C, 1 Series 74 TTL load, $C_L=100$ pF

PARAMETER		TMS4044-12 TMS40L44-12		TMS4044-20 TMS40L44-20		TMS4044-25 TMS40L44-25		TMS4044-45 TMS40L44-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	120		200		250		450		ns
$t_{c(wr)}$	Write cycle time	120		200		250		450		ns
$t_{v(W)}$	Address valid to end of write	110		180		230		230		ns
$t_{w(W)}$	Write pulse width	60		60		75		200		ns
$t_{su(A)}$	Address set up time	0		0		0		0		ns
$t_{su(S)}$	Chip select set up time	60		60		75		200		ns
$t_{su(D)}$	Data set up time	50		60		75		200		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{h(A)}$	Address hold time	0		0		0		0		ns

switching characteristics over recommended voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

PARAMETER		TMS4044-12 TMS40L44-12		TMS4044-20 TMS40L44-20		TMS4044-25 TMS40L44-25		TMS4044-45 TMS40L44-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		120		200		250		450	ns
$t_{a(S)}$	Access time from chip select low		70		70		100		100	ns
$t_{a(W)}$	Access time from write enable high		70		70		100		100	ns
$t_{v(A)}$	Output data valid after address change	20		20		20		20		ns
$t_{dis(S)}$	Output disable time after chip select high		50		60		60		80	ns
$t_{dis(W)}$	Output disable time after write enable low		50		60		60		80	ns

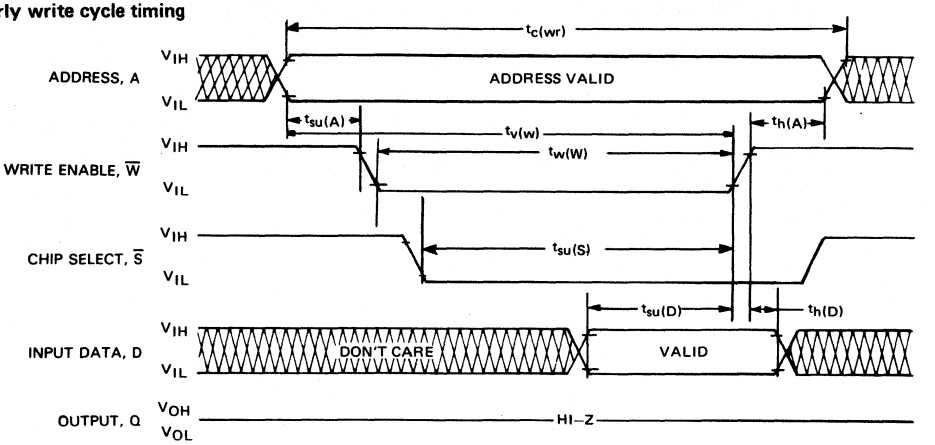
read cycle timing (see Note 3)



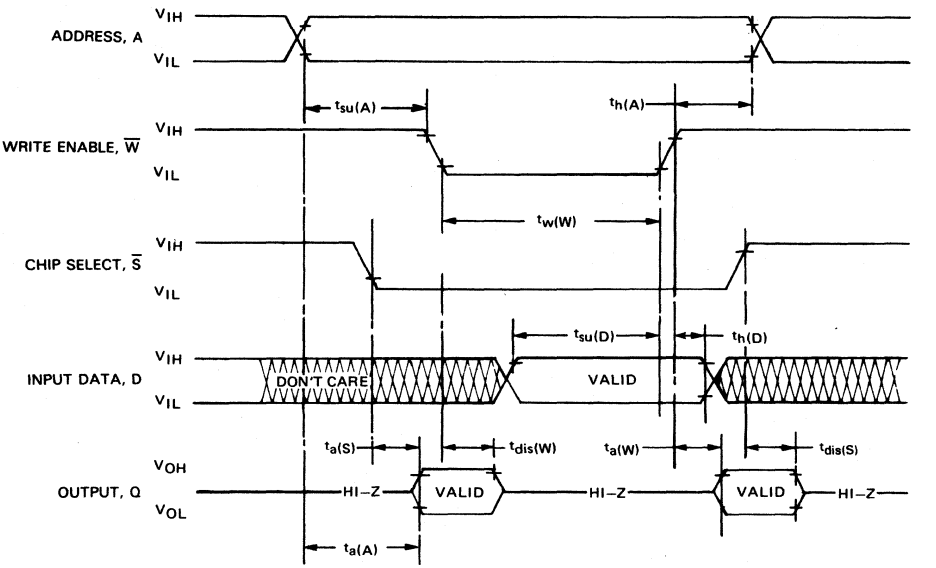
All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times = 10 ns.

NOTE 3. Write enable is high for a read cycle.

early write cycle timing



read-write cycle timing



Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

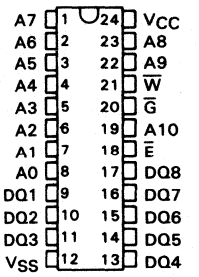
SMJ5517
2048-WORD BY 8-BIT STATIC RAM

DECEMBER 1983

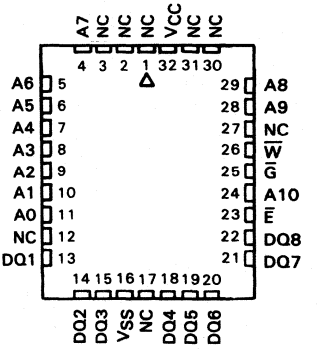
- 2K X 8 Organization, Common I/O
- Single +5-V Supply
- Fully Static Operation (No Clocks, No Refresh)
- JEDEC Standard Pinout
- 24-Pin 600-Mil (15,2 mm) Package Configuration
- Pin Compatible with TMS2516, TMS4016, MB8416, HM6116, and TC5517
- 8-Bit Output for Use in Microprocessor-Based Systems
- 3-State Outputs with $\overline{E}$ for OR-ties
- All Inputs and Outputs Fully TTL Compatible
- Fanout to One Series 54S/74S, Five Series 54LS/74LS or Twenty Series 54ALS/74ALS TTL Loads
- Complementary Silicon Gate MOS Technology with a Six Transistor Memory Cell
- Power Dissipation:
  - Operating — 150 mW Typical
  - Standby — 5 mW Typical
  - Data Retention — 50 μW Typical
- Performance Ranges:

	ACCESS TIME (MAX)
SMJ5517-15	150 ns
SMJ5517-20	200 ns

SMJ5517 . . . JD PACKAGE†
(TOP VIEW)



SMJ5517 . . . FG PACKAGE
(TOP VIEW)



description

The SMJ5517 static random-access memory is organized as 2048 words of 8-bits each. Fabricated using complementary silicon-gate MOS technology, the SMJ5517 operates at high speed and uses less power than conventional NMOS 2K x 8 static RAMs. It is fully compatible with Series 54/74, Series 54S/74S, or 54LS/74LS TTL. Its static design means that no refresh clocking circuitry is needed and timing requirements are simplified. Access time is equal to cycle time. A chip-enable control is provided for controlling the flow of data-in and data-out and another output enable function is included to allow faster access time.

PIN NOMENCLATURE	
A0-A10	Address
DQ1-DQ8	Data In/Data Out
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

The SMJ5517 static RAM has the same standard pinout as TI's compatible 16K SRAMs, and EPROMs. This makes the SMJ5517 plug-in compatible with the '4016 and the '2516. Few modifications, if any, are needed for other 16K

† Low cost J package available soon.

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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5-V SRAM or EPROM. This allows the microprocessor system designer complete flexibility in partitioning his memory board between read/write and nonvolatile storage. Of special importance is the data retention feature of the SMJ5517, as long as $V_{CC} \geq 2$ V, the device retains data indefinitely.

The SMJ5517 is offered in a 24-pin dual-in-line ceramic sidebraze package (JD suffix) and in a 32-pad leadless ceramic chip carrier (FG). The JD package is designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers, whereas the FG package is intended for surface mounting on solder pads on 0.050-inch (1,27 mm) centers. The FG package offers a three layer rectangular chip carrier with dimensions 0.450 × 0.550 × 0.100 (11,43 × 13,97 × 2,54).

operation

addresses (A0-A10)

The eleven address inputs select one of the 2048 8-bit words in the RAM. The address-inputs must be stable for the duration of a write cycle.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

output enable ($\overline{G}$)

The output-enable terminal affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

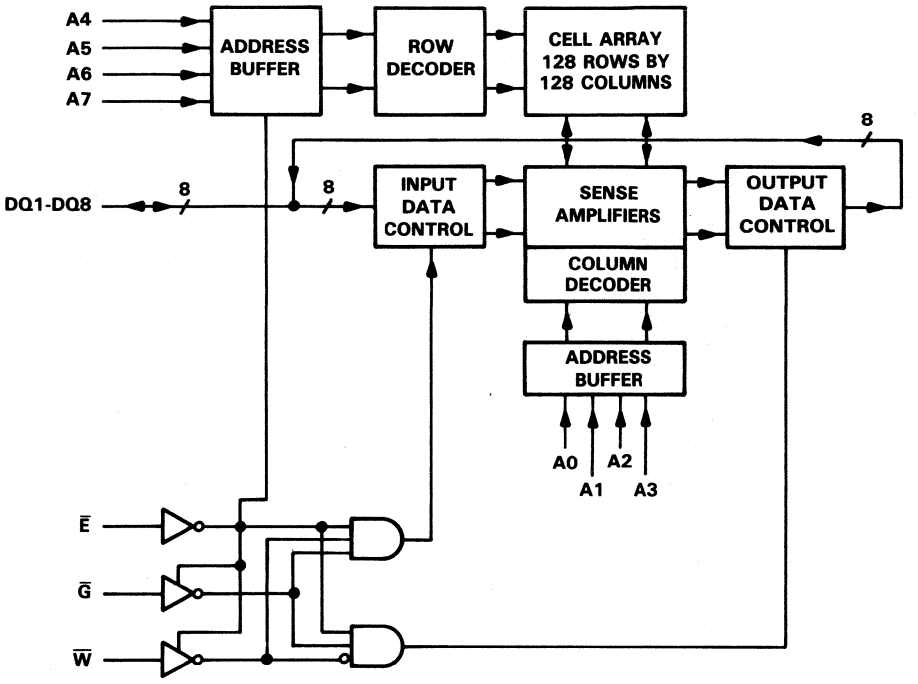
write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location.

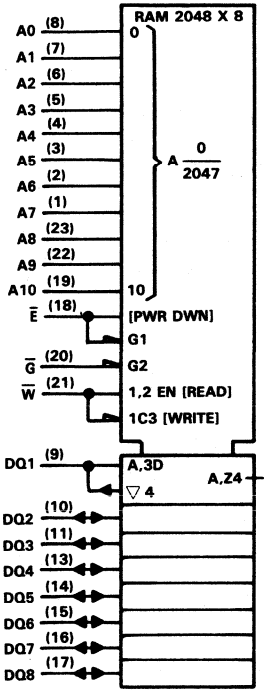
data-in/data-out (DQ1-DQ8)

Data can be written into a selected device when the write-enable input is low. The three-state output buffer provides direct TTL compatibility with a fan-out of one Series 54S/74S, five Series 54LS/74LS, or twenty Series 54ALS/74ALS TTL loads. The D/Q terminals are in the high-impedance state when output enable ($\overline{G}$) is high, chip enable ($\overline{E}$) is high, or whenever a write operation is being performed. Data-out is the same polarity as data-in.

functional block diagram



logic symbol†



FUNCTION TABLE

W̄	Ē	Ḡ	DQ1-DQ8	MODE
L	L	X	VALID DATA	WRITE
H	L	L	DATA OUTPUT	READ
X	H	X	HI-Z	POWER DOWN
H	L	H	HI-Z	OUTPUT DISABLED

† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage (any input) (see Note 1) . . . . . −1 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating case temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the V_{SS} terminal.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.2		$V_{CC}-0.2$	V
Low-level input voltage, V_{IL} (see Note 2)	$V_{SS}-0.2$		0.8	V
Operating case temperature, T_C	−55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −2 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.4	V
I_I	Input current	All inputs except DQ1-DQ8	V_I = 0 V to 5.5 V, V_{CC} = 5.5 V	−1		1	μA
		DQ1-DQ8 inputs only		−5		5	μA
I_{CC1}	Operating supply current from V_{CC}		V_{CC} = 5.5 V,		30	90	mA
I_{CC2}	Standby supply current from V_{CC}		I_O = 0, $\overline{E}$ = V_{IH} MIN			5	mA
I_{CC3}	Data retention supply current from V_{CC}		$\overline{E}$ = V_{CC} −0.2 V			100	μA
$V_{CC(DR)}$	V_{CC} required for data retention		$\overline{E}$ = $V_{CC(DR)}$ −0.2 V	2		5.5	V

† All typical values are at V_{CC} = 5 V, T_C = 25°C.

timing requirements over recommended supply voltage range and operating case temperature range†

PARAMETER		SMJ5517-15		SMJ5517-20		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	150		200		ns
$t_{c(W)}$	Write cycle time	150		200		ns
$t_{w(W)}$	Write pulse duration	90		120		ns
$t_{su(A)}$	Address setup time	10		10		ns
$t_{su(E)}$	Chip enable setup time	90		120		ns
$t_{su(D)}$	Data setup time	50		70		ns
$t_{h(A)}$	Address hold time	10		10		ns
$t_{h(D)}$	Data hold time	10		10		ns
t_{AVWH}	Address valid to write enable high	100		130		ns

† AC test conditions:
Input pulse levels: 0.8 V and 2.2 V
Input rise and fall times: t_r = t_f = 5 ns
Input and output timing reference levels: 0.8 v and 2.2 V
Output load: 1 TTL gate, C_L = 100 pF

switching characteristics over recommended supply voltage range and operating case temperature range†

PARAMETER		SMJ5517-15		SMJ5517-20		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200	ns
$t_{a(E)}$	Access time from chip enable low		150		200	ns
$t_{a(G)}$	Access time from output enable low		60		70	ns
$t_{v(A)}$	Output data valid after address change	10		10		ns
$t_{dis(E)}$	Output disable time after chip enable high		50		60	ns
$t_{dis(G)}$	Output disable time after output enable high		50		60	ns
$t_{dis(W)}$	Output disable time after write enable low		50		50	ns
$t_{en(E)}$	Output enable time after chip enable low	0		0		ns
$t_{en(G)}$	Output enable time after output enable low	0		0		ns
$t_{en(W)}$	Output enable time after write enable high	0		0		ns

† AC test conditions:
Input pulse levels: 0.8 V and 2.2 V
Input rise and fall times: $t_r = t_f = 5$ ns
Input and output timing reference levels: 0.8 V and 2.2 V
Output load: 1 TTL gate, $C_L = 100$ pF

capacitance over recommended supply voltage and operating case temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	$V_I = 0$ V, f = 1 MHz	5	10	pF
C_o	Output capacitance	$V_O = 0$ V, f = 1 MHz	5	10	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are $T_C = 25°C$ and nominal voltages.

PARAMETER MEASUREMENT INFORMATION

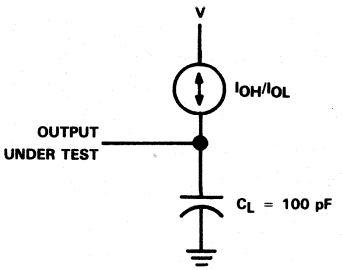
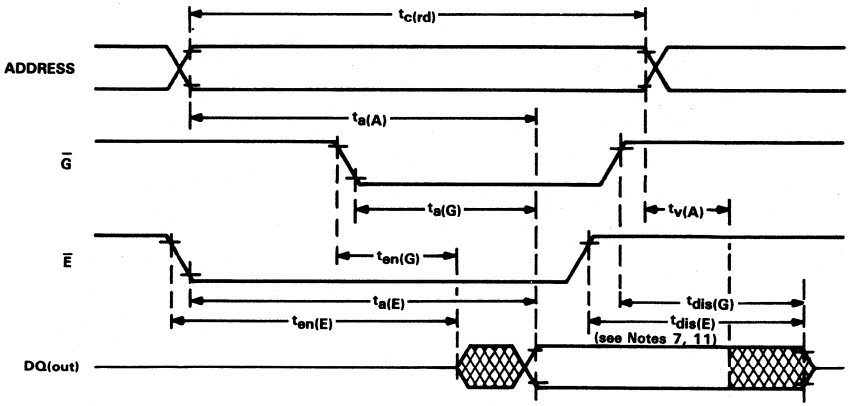


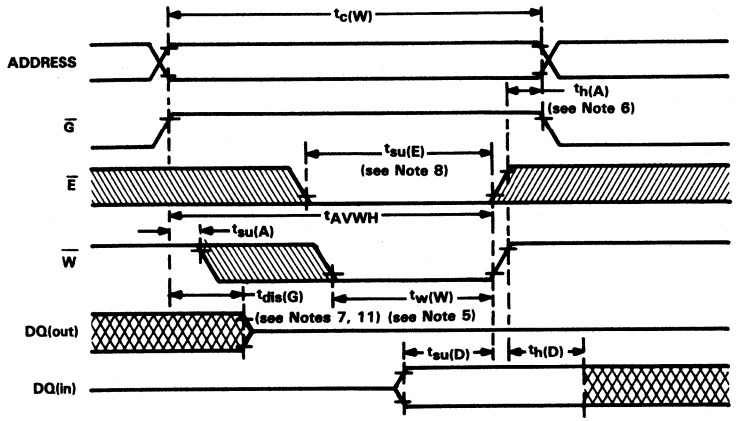
FIGURE 1 – EQUIVALENT LOAD CIRCUIT

timing waveform of read cycle (see note 3)

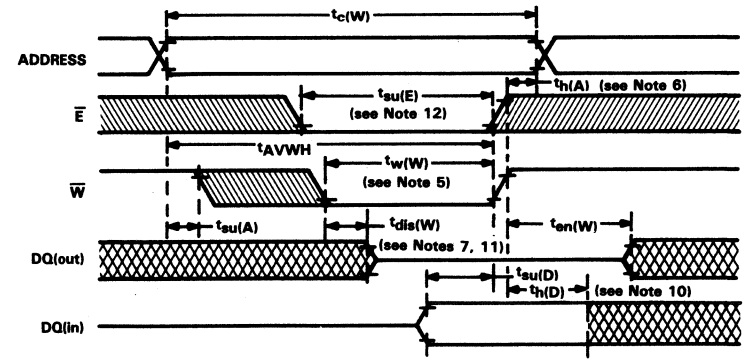


All timing reference points are 0.8 V and 2.2 V.
NOTE 3: $\overline{W}$ is high for Read Cycle.

timing waveform of write cycle no. 1 (see note 4)



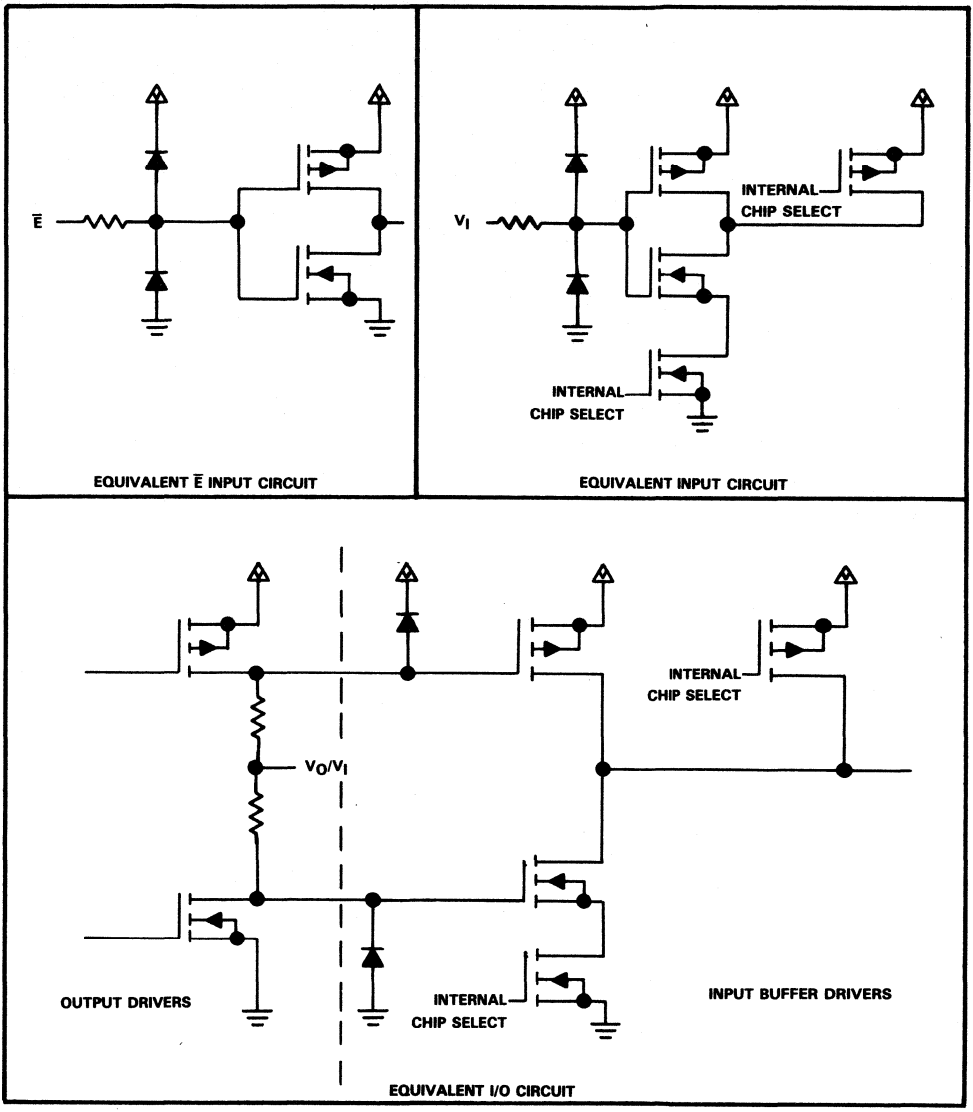
timing waveform of write cycle no. 2 (see notes 4 and 9)



All timing reference points are 0.8 V and 2.2 V.

NOTES:
4. $\overline{W}$ must be high during all address transitions.
5. A write occurs during the overlap of a low $\overline{E}$ and a low $\overline{W}$.
6. $t_{h(A)}$ is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of the write cycle.
7. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
8. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, output remains in a high impedance state.
9. $\overline{G}$ is continuously low ($\overline{G}$ = V_{IL}).
10. If $\overline{E}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied.
11. Transition is measured ±200 mV from steady-state voltage.
12. If the $\overline{E}$ low transition occurs before the $\overline{W}$ low transition, then the data input signals of opposite phase to the outputs must not be applied for the duration of $t_{dis(W)}$ after the $\overline{W}$ low transition.

schematics of inputs and outputs

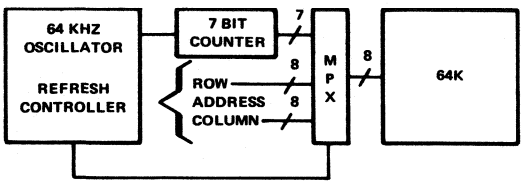


Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

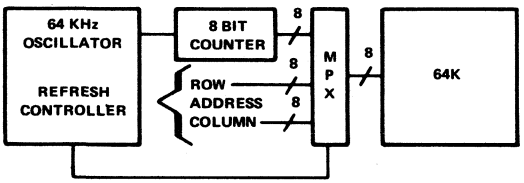
Applications Brief

64K DYNAMIC RAM REFRESH ANALYSIS
SYSTEM DESIGN CONSIDERATIONS

64K SYSTEM HARDWARE



128 CYCLE REFRESH



256 CYCLE REFRESH

- 8 bit address multiplexing and 8 bit address bus are needed for either 256 or 128 cycle refresh on 64K.
- 128 cycle 64K s require 1 less counter bit (7 vs. 8). This is, however, unlikely to be a practical saving since counters/multiplexers come in 4 and 8 bit multiples.
- 256 cycle/4 ms refresh approach allows the same oscillator timing (64 kHz) to be used when upgrading from 16K s (128 cycle/2 ms period).
- Systems designed for 256 cycle 64K s can easily use 128 cycle 64K s.

Compatibility among all 64K Dynamic RAM vendors can be achieved by designing to TI's 4164 64K x 1 Dynamic RAM. The TMS 4164 requires all 256 rows to be refreshed within 4 ms. Competitive 64K DRAMs which are not able to achieve the 256 cycle, 4 ms refresh rate require twice the number of sense amplifiers as the TMS 4164 and half the number of refresh addresses. A 64K DRAM which requires the 128 cycle, 2 ms refresh treats the 256 cycle, 4 ms refresh as two refresh events in 2 ms each.

Simply: 256 cycle in 4 ms = 2 (128 cycle in 2 ms)

The extra address bit, A7, during refresh is treated by these vendors as a don't care situation.

The TMS 4164 has the same refresh rate as the 4116, 16K x 1 Dynamic RAM, which requires 128 rows to be refreshed in 2 ms. Most 4116 based systems already contain the extra refresh counter bit required for upgrading to the 64K. Those implemented with the 74LS393, 8-bit counter already do.

For a given cycle time, say 280 ns, the 256 cycle 4 ms refresh architecture of the TMS 4164 requires the same refresh overhead as the 128 cycle 2 ms approach as can be seen by the following calculations:

$$\text{Refresh overhead} = \frac{\text{refresh cycles in given time}}{\text{available cycles in given time}} = \frac{256 \text{ cycles}}{4 \text{ ms}/280 \text{ ns per cycle}} = \frac{128 \text{ cycles}}{2 \text{ ms}/280 \text{ ns per cycle}} = 1.8\%$$

However, the TMS 4164 provides the user with the following advantages:

- Half the number of sense amplifiers, small chip size, low cost.
- Lower power yielding lower temperature and increased reliability.
- More chip area devoted to memory array allowing greater detectable cell charge and improved performance.

In summary, the TMS 4164 is compatible with 16K DRAMs and other 64K DRAMs since they are all refreshed at the same rate. An extra counter bit A7, introduced to the TMS 4164 during refresh will insure compatibility among all 64K DRAMs.

MOS Memory
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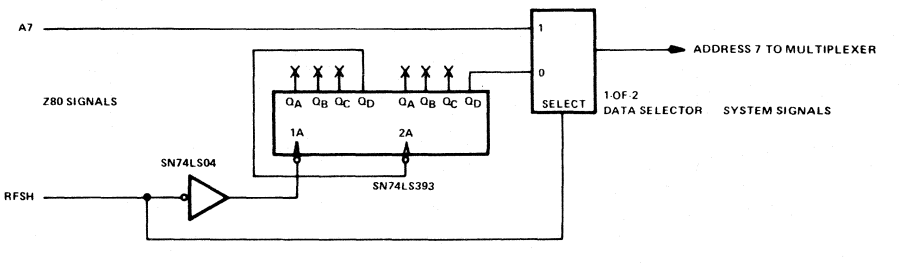
Applications Brief

256-CYCLE REFRESH CONVERSION



This may be implemented in discrete logic, with an SN74LS157 or other scheme.

CIRCUIT TO CONVERT Z80 128-CYCLE REFRESH TO 256-CYCLE REFRESH REQUIRED BY TMS 4164

Adding the circuit above to Z80-based systems increases availability and competitive pricing among those vendors who have announced 64K dynamic RAMs[1] including

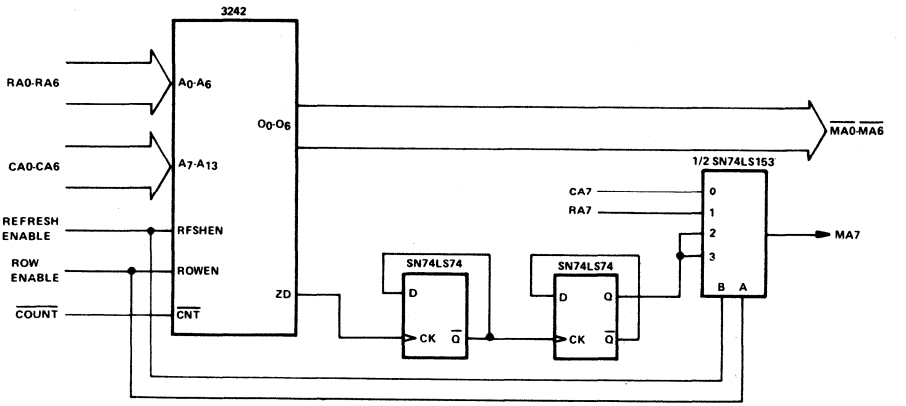
* TEXAS INSTRUMENTS
- Fairchild
- Inmos
- National
- Signetics

Z80 users who are considering an upgrade in dynamic memory from 16K to 64K have much to gain by modifying the Z80 128-cycle refresh. The circuit shown above converts the Z80 128-cycle refresh to the 256-cycle refresh required by TI's TMS 4164 64K dynamic RAM. Designing in the 256-cycle refresh results in broader choice of 64K dynamic memory available to the designer. Designing with only 128-cycle capability severely limits the potential sources for 64K dynamic RAMs.

Adding the circuit shown above to the Z80-based system also allows the designer to take advantage of the TMS 4164's low cost and low power dissipation that result from using only half as many sense amplifiers as the 128-cycle approach.

[1] Electronics, May 22, 1980

EXPANSION OF 3242 FOR 256-CYCLE REFRESH

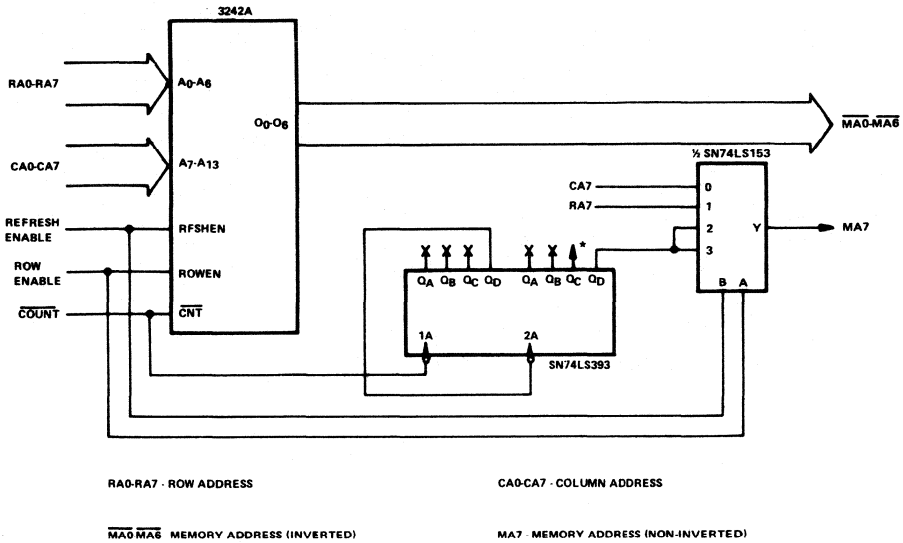


Adding the above circuit to those systems which utilize a 3242 allows the use of 256-cycle-refresh parts. The circuit on the following page may also be incorporated into designs using the 3242A where the zero-detect output is not available.

These designs are presented to demonstrate possible implementation, however, particular system requirements may suggest alternate circuits to optimize component layout.

NOTE: The SN74LS153 may be replaced with an SN74LS352 to obtain inverted signal for all memory addresses.

EXPANSION OF 3242A FOR 256-CYCLE REFRESH



★ This output may be used to implement 256-cycle refresh for 3232 devices in conjunction with the other half of the SN74LS153.

In summary, these circuits show how to convert a system to a design with maximum flexibility that can use either 128-cycle or 256-cycle 64K dynamic RAMs. Meeting this requirement allows the use of any 64K RAM which will ultimately result in the lowest cost and most reliable system.

MOS Memory
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Applications Brief

TMS4164A AND TMS4416
INPUT DIODE PROTECTION

The 64K DRAM family from Texas Instruments has departed from conventional input schemes for DRAMs to provide the user with improved ESD protection and input clamping diodes for negative undershoot. Both enhancements of device capability are possible due to the use by TI of a grounded epitaxial substrate in the manufacture of its 64K DRAMs. While the input circuit technique has provided the user with additional protection and ease of use, it may cause anomalous testing results for the unwary test engineer who tires to drive the inputs to large negative voltages.

Shown below is an equivalent circuit for the input circuitry of the TMS4164A and the TMS4416.

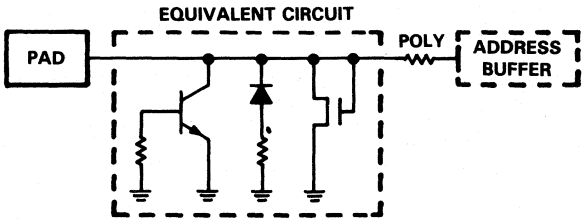


FIGURE 1 – EQUIVALENT INPUT CIRCUITRY

The diode and transistor clamping circuit is the essential element in protecting the device from electrostatic discharge (ESD) damage. Figure 2 shows the physical layout of this circuit.

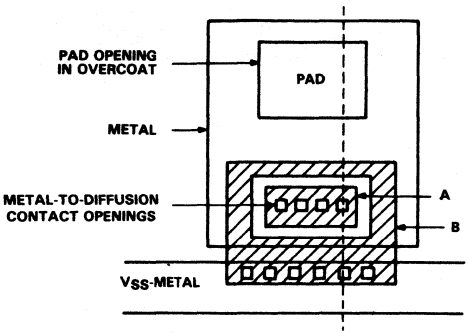


FIGURE 2A – DIODE AND TRANSISTOR CLAMPING CIRCUIT

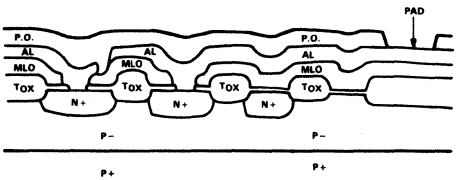


FIGURE 2B – CROSS SECTION OF CLAMPING CIRCUIT

The essential element of the circuit is the input diode (A), which is surrounded by a diffused guard ring (B) connected to V_{SS}. This circuit can be viewed as a combination of a lateral NPN transistor, a bipolar diode, and a thick field transistor – all occupying the same area and connected to the input pad. The P–/P+ substrate is both the base of the transistor and the anode of the diode. Both are connected to V_{SS} through the resistance of the substrate from the surface of the chip to the backside. During an ESD with positive voltage, the input diffused area goes into reverse-bias breakdown, which turns on the bipolar transistor, thus clamping the input voltage. The action of the transistor is identical to second breakdown observed in conventional bipolar transistors. Once the transistor turns on, it can sink a large amount of transient current which is evenly distributed over the area of the input diffusion (collector of the lateral transistor). This avoids localized heating from the energy in the ESD. Localized heating could destroy the integrity of the input diode. For ESD with negative voltage, the diode and the transistor act to clamp the input voltage. When the input voltage drops below –0.7 V, the input diffusion appears as a cathode for a diode tied through the substrate resistance to ground. It also acts as an emitter for the lateral NPN transistor. Both elements turn on and tend to uniformly source the current in the input diffusion.

The polysilicon resistor included in the input circuit serves to limit the amount of voltage that reaches the thin oxide associated with the address buffers and clock inputs. The dynamic impedance of the input clamping circuit is considerably lower than the resistance of the polysilicon resistor.

The input circuit also offers the advantage of clamping negative undershoots on the inputs during normal operation. While this provides advantage to the board and system designer, it can cause confusion for the test engineer unless he fully understands the limits of his tester. DRAMs have historically been specified with negative dc input voltages of –1 V. In addition, they are often tested/characterized to –3 V. This testing has been done to ensure that the devices will operate correctly with a negative input undershoot, which is transient. Such testing was required due to the inability of a MOSFET of reasonable size on the chip to clamp the negative-going input and due to the susceptibility of address input buffers on some MOS RAMs to negative input undershoots. The input clamping mechanism, provided on the TMS4164A and the TMS4416, can supply sufficient current to clamp the input transient.

Difficulty in testing the device with negative dc input voltages can occur due to the tester's output driver devices going into saturation when forward biasing the input diode. Also, most testers are unable to supply the large transient current requirement during reversal of bias on the input diode and transistor. Both effects will result in distortion of the tester's waveforms. What may appear to be poor setup and hold time margins of the device may actually be a tester's inability to supply the correct waveforms to the device at the proper time.

The improvement in both ESD protection and signal undershoot on system boards offered by the input circuit may be overlooked if erroneous conclusions are drawn from incoming testing with negative dc input voltages below –0.7 V.

TESTER LIMITATIONS WITH PROGRAMMED INPUT LOW LEVELS OF LESS THAN – 0.7 V

Driver distortion occurs when input low levels are programmed for values below –0.7 V. The input diode/lateral NPN transistor shares a common PN junction which becomes forward biased at –0.7 V and below. The transistor collector, which is tied to V_{SS}, carries most of the forward-bias current (see Figure 3).

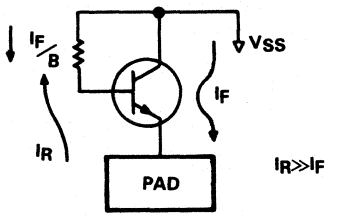
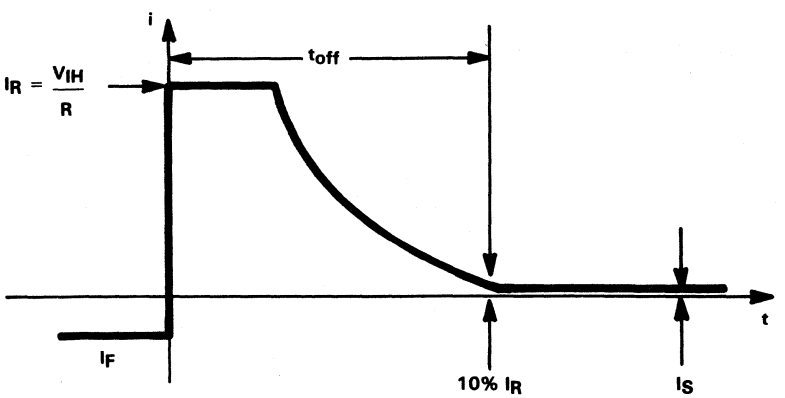


FIGURE 3 – FORWARD- TO REVERSE-BIAS CURRENT

The diode exhibits a classical forward- to reverse-bias recovery delay due to a momentarily large reverse current of amplitude limited only by the programmed reverse voltage V_{IH} and driver output impedance R, i.e., the input approximates a momentary short circuit. An initially large short-circuit current plateau ($I_R = V_{IH}/R$) subsequently relaxes to the normal dc reverse-bias current I_S (see Figure 4). The time from the positive transition edge, corresponding to t = 0 in Figure 4, to the point where the reverse current surge relaxes to 10% of the plateau value is the diode recovery time (t_{off}).



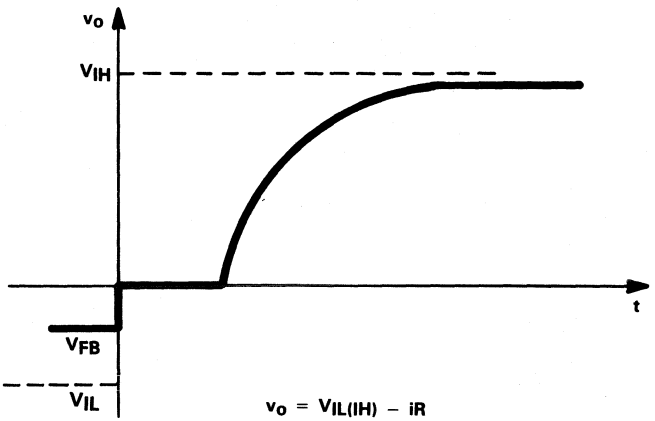
R: Driver impedance
V_{IH}: Address input high-level (reverse-bias)

FIGURE 4 – FORWARD- TO REVERSE-BIAS RECOVERY CURRENT

Figure 5 shows how the driver output waveform is altered. During forward bias, the transistor clips the negative level at V_{FB} (in the range -0.7 V to -1.4 V) with the V_{IL} level programmed over the range of -0.7 V to -6 V. During the initial reverse bias, the driver output voltage v_o is given by the programmed V_{IH} level minus the iR drop across the driver output impedance, i.e.,

$$v_o = V_{IH} - iR$$

During the current plateau, the v_o value is essentially 0 V. The driver output voltage then recovers to the programmed value as the diode reverse current relaxes to the dc reverse-bias level I_S. In effect, the t_{off} value is a measure of the time that the output waveform is distorted if the unwary engineer programs V_{IL} values significantly below -0.7 V.



$v_o = V_{IL(IH)} - iR$
V_{FB}: Forward-bias diode drop
V_{IL}: Address input low-level (forward-bias)

FIGURE 5 – ADDRESS DRIVER OUTPUT VOLTAGE

The following equation derived from diode switching theory serves to estimate the magnitude of the t_{off} values for input levels below -1 V.

$$t_{off} = 40\ [r - [r/(r+1)]^2]\ \text{ns}$$
$$\text{where } r = -(V_{IL} + 1)/V_{IH}$$
$$\text{and } V_{IL} < -1\ \text{V}$$

The coefficient 40 ns is a characteristic of the diode structure and physical parameters of the material. For example, $V_{IL} = -3$ V and $V_{IH} = +3$ V give $t_{off} = 20$ ns. This estimate is not accurate at very small forward-bias values, because it ignores the rise time of the driver's positive transition edge. As long as the predicted value is greater than or equal to the edge transition time, the estimate is good. It is assumed that driver output impedance has the same value R at both upper and lower levels, V_{IH} and V_{IL}.

The distortion in driver waveform, shown in Figure 5, increases as the driver input low level is progressively driven more negative. Depending on driver output impedence, only slight distortion is observed in the positive transition for input levels near -0.7 V to -1 V. This irregularity corresponds to the onset of the recovery phenomenon short-circuiting the output of the driver. Significant distortion occurs at large negative values of V_{IL}, and the test engineer must be aware of this phenomenon to prevent erroneous conclusions as to the performance of the device.

The input transistor provides great advantage to device use in a system environment. In a system, the negative undershoot of an address line is caused by transient transmission-line reflections (undershoot of negative-edge transitions). Here the input transistor clips much of the swing below -0.7 V on the address line. Positive-edge transition from a settled negative address low level, which gives rise to the forward-to reverse-bias recovery delay, does not occur in the typical system environment.

Applications Brief

TMS4164 AND TMS4416 INTERLOCK CLOCK

The TMS4164 (64K × 1) and TMS4416 (16K × 4) dynamic RAMs use a novel interlocked clock to yield enhanced immunity to process variations, temperature, and voltage induced parametric changes. The basic concept of an interlock clock structure is to provide a synchronous timing operation that eliminates race conditions. As an aid to understanding the interlock clock, an overview of the memory control structure and its functions will be presented first.

The TMS4164 (Figure 1) and TMS4416 (Figure 2) need a minimum of 16 address bits to address all of their 64K memory locations (2^{16} = 65,536). Instead of physically using 16 address pins, the DRAMS only use 8 address pins and receive the addresses in two parts of 8 bits each (8 (row) and 6 (column) in the case of the TMS4416). The first 8 addresses are called the row addresses; once stable on the address pins, they are latched by the low going edge of the row address strobe ($\overline{RAS}$) input. The 8 column address bits are then set up on the 8 address pins and latched by the low going edge of the column address strobe ($\overline{CAS}$) input. The TMS4416 only uses 6 of the column address lines, disregarding A0 and A7 (These will be utilized in next generation parts providing an address for 64K × 4 memories). This sharing of address lines is known as multiplexing which keeps the number of pins on a package to a minimum.

The TMS4164 and TMS4416 use a square array of memory cells consisting of 256 rows and 256 columns which is divided into an upper and lower half. A word line (which corresponds to a row) is connected to the transfer gates of 256 cells that comprise a row of memory. The transfer gates control access to the data stored on the memory cell capacitor. The bit line (which corresponds to a half of a column) has for each half of the array 128 memory cells and 1 dummy cell connected to it via the transfer gates. Located physically between the two halves of the memory array are 256 sense amps whose inputs connect to the bit lines from each half of the array. The dummy cell provides the reference (V_{REF}) to a sense amp to determine the state of the memory cell.

On an access cycle, the row decoders drive the selected word line high turning on all 256 transfer gates in the selected row and connect 1 memory cell to each bit line. Concurrently, dummy enable (DE) decodes and drives the transfer gates of one of the rows of dummy cells, and connects 1 dummy cell to each bit line on the opposite side of the sense amps. The dummy selection uses RA7 so that the row of dummy cells selected is on the opposite side of the sense amp from the selected row of memory cells. Connecting the memory and dummy cells to their respective bit lines causes a differential voltage to be established at the inputs of the sense amps. This differential voltage is then detected by the sense amps whose outputs will change to reflect the detected state of the memory cells. After sensing is completed, the output of the sense amp is driven back onto the bit lines to refresh the memory cells. Signal restoration is necessary because an access results in a destructive read (the memory cells no longer contain valid data after the access). This is due to the large bit line capacitance (≈600 fF) and the relatively small capacitance of the cell (50 fF). Connecting the cell to the bit line depletes the cell charge, and makes refresh necessary to ensure valid data retention. This restoration is transparent to the user but should not be confused with providing external refresh. After sensing is completed, the data on the bit lines can now be selected by the column decoders. The column decoders select 4 of the 256 sense amps using A0-A5 (TMS4164) and A1-A6 (TMS4416) for the selection. On the TMS4164, these 4 bits are further decoded by a 1 of 4 decoder using A6 and A7 (the 4 bit output of the TMS4416 eliminates the need for the 1 of 4 decoder). This 1 of 4 selector acts as a bidirectional switch for data transfer to or from the sense amps. Now that the basic blocks and functions of a DRAM have been described, a detailed look at the interlock scheme will be presented.

A simplified logic representation of the clock structure is shown in Figures 1 and 2. The clock interlock points are shown as inverting input NAND gates. The inputs represent timing events that must be complete before the output of the inverting input NAND gate can trigger a third event; this system provides interlocking. Approximately 60-100 clock signals are generated in a DRAM to control the various functions (address latching, decode timing, sensing, data transfers within the device, etc.); approximately 15 of these have been represented. The following discussion briefly shows the operation of the TMS4164 and TMS4416 DRAMs.

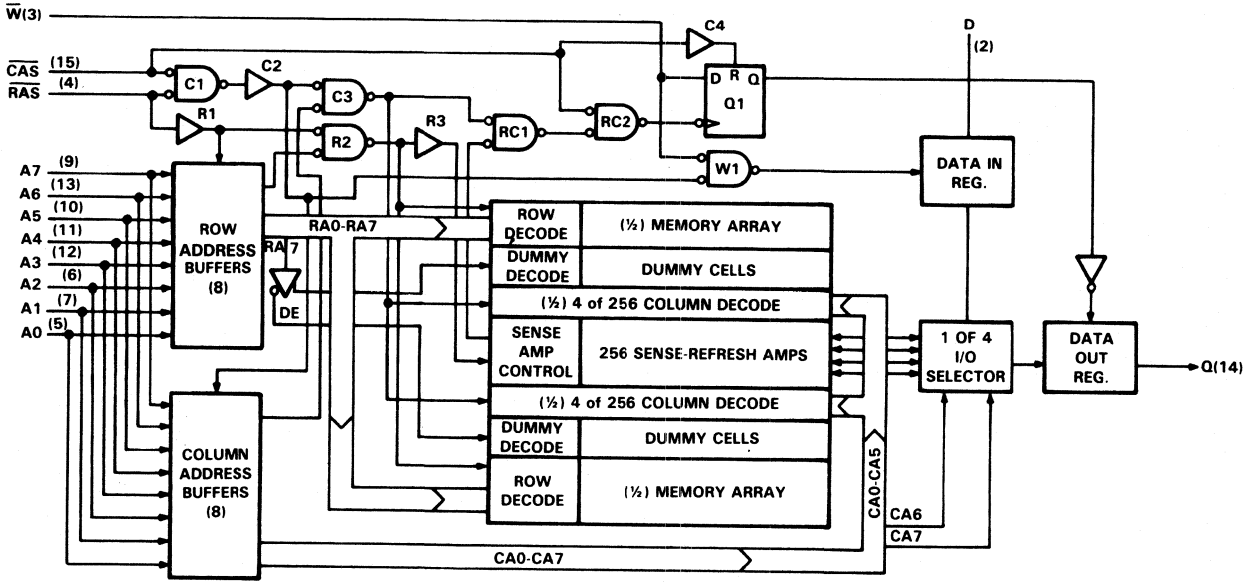


FIGURE 1 — TMS4164 BLOCK DIAGRAM

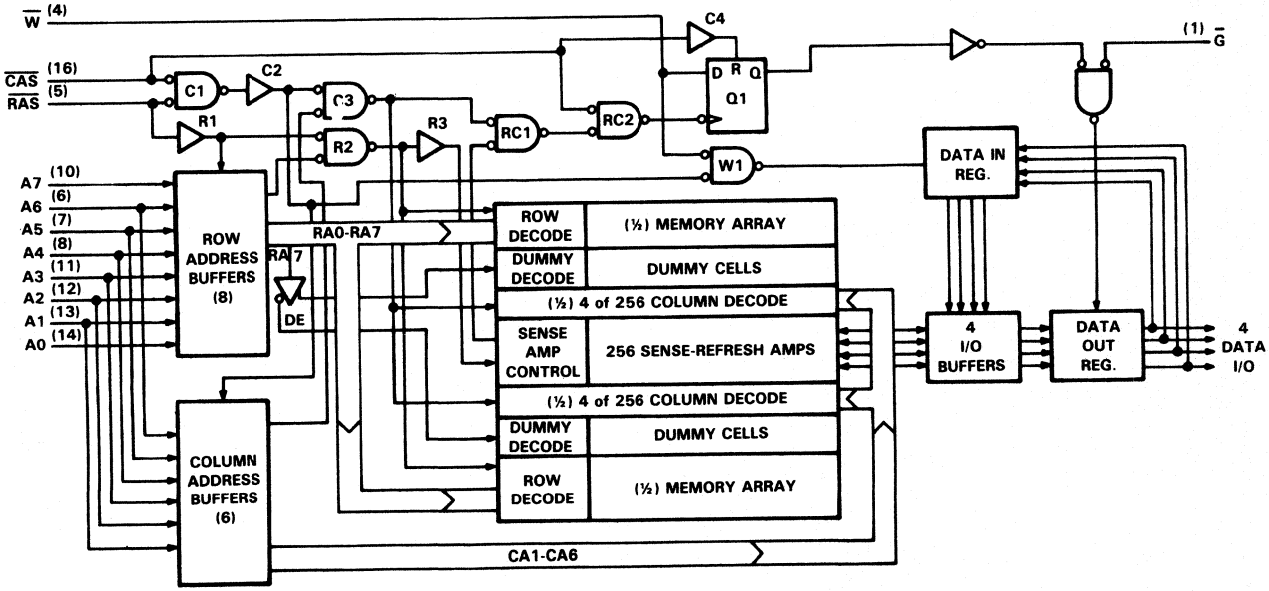


FIGURE 2 – TMS4416 BLOCK DIAGRAM

The falling edge of $\overline{RAS}$ causes R1 to latch the row addresses into the row address buffers and enables interlock point R2. The row addresses are then amplified and drive the row decoders for row selection. When RA0-RA7 are valid, the row address buffers output a signal to interlock point R2. A delay stage within R2 allows the row decoders time to complete their decoding before the output of R2 goes low. R2 going low enables the row decoders to drive the selected word line high. Interlock R2 ensures two things: the row addresses are valid, and decoding is complete before the selected word line is activated. Address RA7 causes dummy enable (DE) to select the row of dummy cells on the opposite side of the array from the selected row of memory cells. After row and dummy selection is completed, the decoders then drive the appropriate word lines high, connecting the memory and dummy cells to their corresponding bit lines. The differential voltage at the inputs of the sense amp is sensed, amplified, and driven back onto the bit lines; this refreshes the memory cells in the selected row. The sense amp control then outputs a signal to interlock RC1 that indicates sensing is complete.

A high logic level on $\overline{CAS}$ holds the reset on Q1 active and forces the Q output of the data out buffer into a high-impedance state. A logic low level on $\overline{CAS}$ removes the reset to allow clocking.

The falling edge of $\overline{CAS}$ causes interlock C1 to go low (assuming $\overline{RAS}$ low) driving C2 low to latch the column addresses into the column address buffers. Interlock C1 ensures that the $\overline{CAS}$ cycle is inactive until $\overline{RAS}$ is low. The column addresses are then amplified and drive the column decoders for column selection. With CA0-CA7 valid, the column address buffers output a signal to interlock point C3. A delay stage within C3 allows the column decoders time to complete their decoding before the output of C3 goes low. C3 going low enables the column decoders to access the selected columns (4). Interlock C3 ensures two things: the column addresses are valid, and decoding is complete before the selected columns are accessed. After selection is completed, data can now either be input or output depending on the $\overline{W}$ signal timing. Interlocks RC1 and RC2 ensure that the sense amps are active and the proper column is selected before a read or write can take place.

In the case of a read or read-modify-write cycle, the high logic level on the write line ($\overline{W}$) prevents any transfer into the data in register by keeping the output of W1 high. The presence of $\overline{CAS}$ low and the output of RC1 low allows RC2's output to go low; this clocks the level of $\overline{W}$ into register Q1. Only in the case of an early write ($\overline{W}$ low prior to $\overline{CAS}$ low), when the output of Q1 is not clocked to a logic one, will the data out register be maintained in the high-impedance state. In any read cycle, the output of Q1 is a logic one and the data out register is enabled although data will not be valid until $\overline{RAS}$ and $\overline{CAS}$ access times are both satisfied.

In a write cycle, the low logic level on $\overline{W}$ allows the output of W1 to go low which latches the data present at D (thus the latter of either $\overline{CAS}$ or $\overline{W}$ going low latches the data). The logic level at the output of the data out register will remain until $\overline{CAS}$ returns to a high level.(When $\overline{CAS}$ is high, the output will go to a high-impedance state.) Data out reflects the data read from the cell rather than the new data that is written for read-modify-write cycles.

The $\overline{RAS}$ low time following sensing complete, is used to restore data to the memory cells currently selected by the word line (restoration after the desctuctive read). Any data that is changed by a write cycle causes alterations of the sense amplifier which then stores the new data in the memory cells. When $\overline{RAS}$ goes high, the word line is turned off and the cells now hold the data restored from the sense amps. $\overline{RAS}$ going high initializes a precharge state used to equalize the bit lines by charging them to full V_{DD} potential. Precharge is necessary to ensure the charge on the bit lines is equal on both sides of the sense amp. Another access cycle may begin once the precharge time has been met.

The representation used in Figures 1 and 2 is a simplified logic diagram which does not depict all points of signal interlocking. It does however demonstrate the principle of an interlocked clock scheme. The signal generation and timing becomes very critical as device delays decrease. In many dynamic RAMs there are over 100 timing signals used to control internal operations, and these timing signals are generated using delay chains without interlocking. The signal skew resulting from non-interlocked timing increases device sensitivity to operating conditions and process variations. Although the interlock clock is transparent to the user, its incorporation on the TMS4164 and TMS4416 offers greater component reliability and avoids timing race conditions inherent in previous generation DRAMs.

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INTRODUCTION TO SURFACE MOUNT TECHNOLOGY

ABSTRACT

The demand for high-density, cost-effective printed circuit boards has prompted the electronics industry to seek alternative methods to traditional plated-through-hole technology. One such alternative is surface mounting, a technology traditionally used in hybrid fabrication. The advantages of surface mounting are numerous but the bottom line is that it is cost effective and will begin to displace plated-through-hole technology as the availability of surface-mount components increases.

Texas Instruments is fully supporting the growth of the surface-mount industry with its line of plastic leaded chip carriers. An introduction to the surface-mount technology will be given in this application report.

INTRODUCTION

The post molded leaded chip carrier (PLCC) was developed by Texas Instruments in 1980 to improve the packing density of ICs on printed circuit (PC) boards and overcome some of the size constraints normally caused by dual-in-line (DIP) packages. The PLCC was also designed to be used under the same environmental conditions as the DIP without any reliability degradation. The PLCC occupies approximately 40% to 60% of the PC board area of an equivalent DIP, and requires no through holes (surface mount), therefore, it lowers the cost on PC boards. Unlike some surface-mounted packages, TI's PLCC requires no special PC board material considerations. The design of the lead provides compliance allowing the use of any commercial substrate. Digital, Linear, Gate Array, and MOS devices will be offered in 18-, 20-, 28-, 44-, 52-, 68-, and 84-pin packages through TI.

Package Outline

The mechanical data for the PLCCs is given in Figures 1 and 2; their thermal properties are listed in Table I. The following general statements apply to the packages:

1. Each of the chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high humidity conditions.
2. These packages are intended for surface mounting on solder pads with 1,27-mm (0.050-inch) centers. The leads require no additional cleaning or processing when used in soldered assembly.
3. All dimensions shown are metric units (millimeters), with English units (inches) shown parenthetically. Inch dimensions govern.
4. Lead spacing shall be measured within the zones specified.
5. Tolerances are noncumulative.
6. Lead material CD-155. T60 (Copper Alloy).
7. Dimple in top of package denotes pin 1.

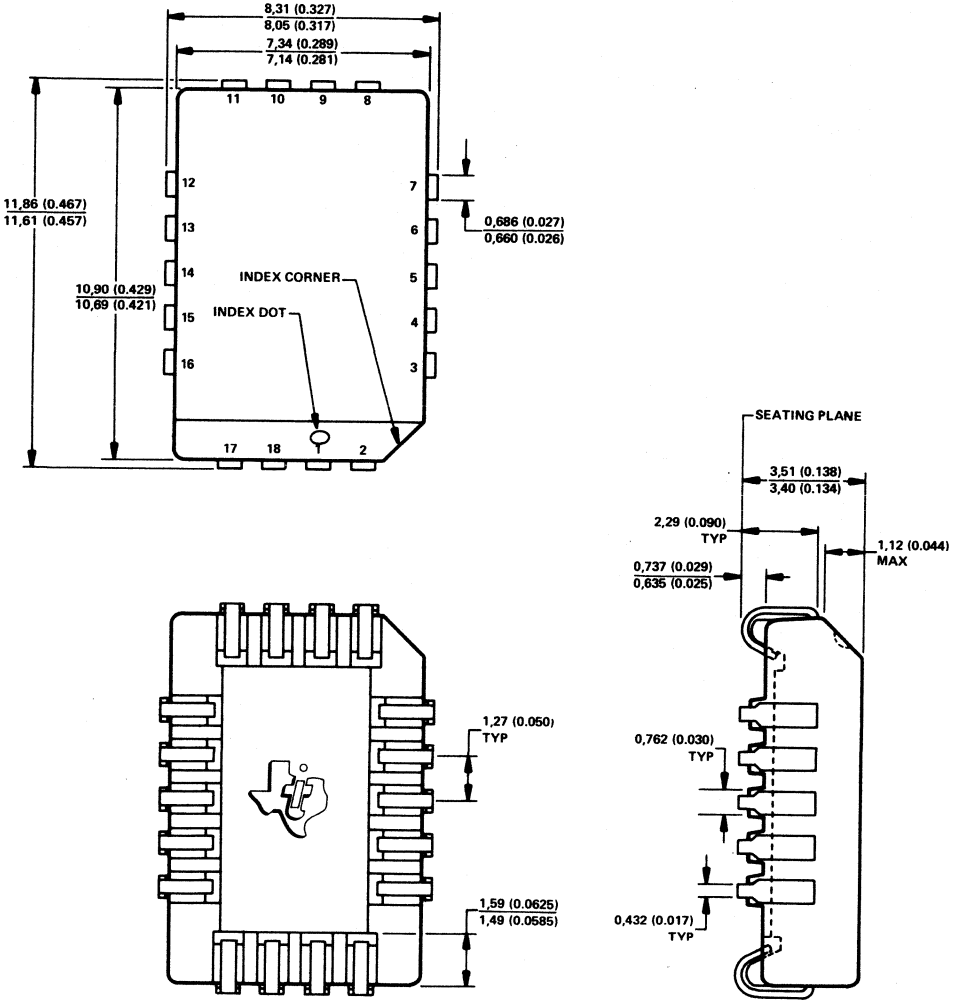
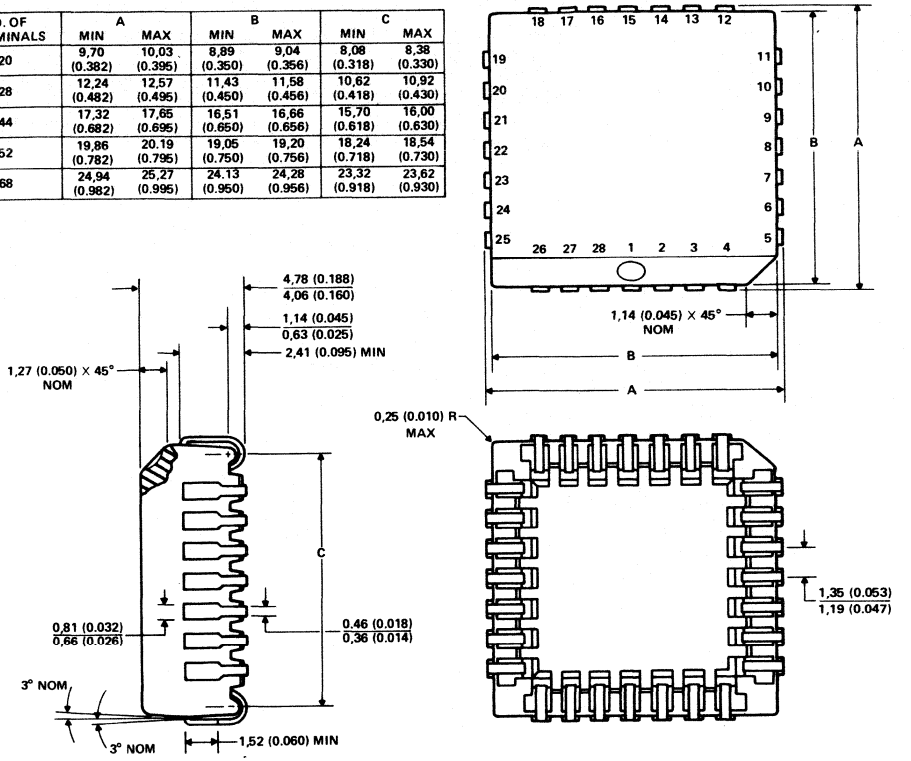


Figure 1. Plastic Chip Carrier Package (FP Suffix)

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,70 (0.382)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	12,24 (0.482)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)
44	17,32 (0.682)	17,65 (0.695)	16,51 (0.650)	16,66 (0.656)	15,70 (0.618)	16,00 (0.630)
52	19,86 (0.782)	20.19 (0.795)	19,05 (0.750)	19,20 (0.756)	18,24 (0.718)	18,54 (0.730)
68	24,94 (0.982)	25,27 (0.995)	24,13 (0.950)	24,28 (0.956)	23,32 (0.918)	23,62 (0.930)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

Figure 2. FN Plastic Chip Carrier Package

Table I. Thermal Properties, of Plastic Chip Carriers

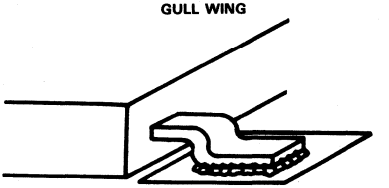
NO. OF LEADS	PACKAGE DESIGNATION	θJA (° C/N)	θJC (° C/W)
18	FP	85.4	13.8
20	FN	113.6	37.1
28	FN	76.8	32.2
44	FN	68.0	20.3
68	FN	45.7	11.4

J-Lead Advantage

Texas Instruments PLCC packages are constructed with the J-lead structure due to its superior performance when mounted on a wide spectrum of substrates ranging from ceramic to epoxy-glass. This is possible due to the compliancy of the J-lead which compensates for the possible thermal mismatch between plastic packages and mounting substrates.

More care must be taken when using ceramic leadless chip carriers mounted on nonceramic substrates in order to prevent solder joint fracturing under thermal cycling. The J-lead also offers advantages over plastic surface-mount packages using different lead structures. Figure 3 gives a comparison of the J-lead used on the PLCC to the "gull wing" commonly used on small-outline integrated circuits (SOICs) and "quad packs."

GULL WING



DEVICE AREA (16 L-PIN SOIC) = 111,6 mm^2 (0.173 in^2)

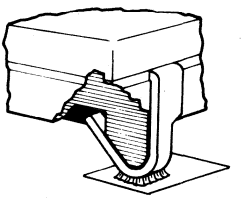
ADVANTAGES

- PROVEN PROCESS
- POSITIVE SOLDER "WITNESS"
- EASY AUTO-POSITIONING
- NESTED STACKING (PERIPHERAL)

DISADVANTAGES

- EXTENDS X-Y SIZE
- LEADS SUBJECT TO DAMAGE
- HIGH PIN COUNT PACKAGES IMPRACTICAL

J-LEAD



DEVICE AREA (18-PIN PLCC) = 98,6 mm^2 (0.153 in^2)

ADVANTAGES

- PROVEN PROCESS
- LEADS ARE COMPLIANT, USEABLE WITH PC BOARD AND CERAMIC SUBSTRATES
- MINIMUM X-Y SIZE, MAXIMUM BOARD DENSITY
- EASY AUTO POSITIONING
- LEADS WELL PROTECTED
- EASY REPLACEMENT
- SOCKETING EASY
- JEDEC STANDARDS EXIST
- STAND-OFF FROM THE BOARD ALLOWS EASY CLEANING
- LARGEST LINE OF AVAILABLE PACKAGES: FROM 18 TO 68 LEADS. HIGHER PIN COUNTS UNDER DEVELOPMENT

DISADVANTAGES

- TOTAL PACKAGE-HEIGHT THICKER THAN SOIC
- INFRARED (IR) REFLOW DIFFICULT

Figure 3. Gull Wing Vs. J-Lead

Area Savings with PLCC

The PC board area savings that can be realized with the PLCC is best demonstrated by a comparison of two Texas Instruments one megabyte memory boards (see Figure 4). The DIP board is eight layers, measuring 279,4 mm (11 inches) by 355,6 mm (14 inches) with 226 ICs. The PLCC board is four layers, measuring 165,1 mm (6.5 inches) by 243,84 mm (9.6 inches) also with 226 ICs. The savings that can be realized with the PLCC board amounts to 60% less board area at an overall cost savings of approximately 55%. This illustrates the viability of surface mount as a low cost means of improving circuit board density while reducing PC layout complexity.

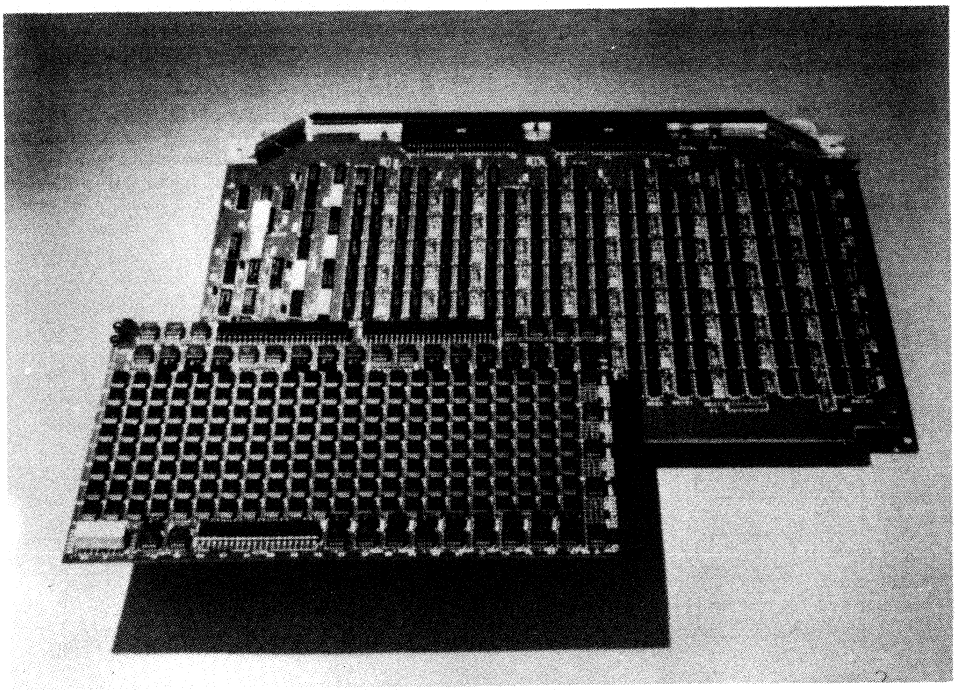


Figure 4. PLCC and DIP One Megabyte Memory Expansion Boards

Surface Mount Component Availability

Most IC manufacturers are presently producing surface-mount components for a large part of their product line. The devices available range from the sophisticated VLSI to the discrete transistor. Non-integrated circuit components ranging from chip resistors and capacitors to surface-mount connectors are also being produced in volume by major manufacturers. As the demand for surface-mount components increases, most products now produced for standard through-hole technology will also be available in surface mount. As of the printing of this application report TI produces over 700 ICs in surface mount packages.

Surface mounting consists of five basic steps:

1. PC board design
2. Solder paste application
3. Component mounting
4. Oven drying (optional)
5. Solder reflow

A brief description of each step will be given; detailed descriptions of the various steps can be obtained by component and equipment suppliers and from numerous technical articles on surface mounting.

PC Board Design

To produce reliable surface-mount PC boards the designer has to pay particular attention to IC solder pad (also termed footprint) layout. Not providing adequate footprint area and proper orientation will generally yield poor solder joints and lack of self-centering during reflow. Figure 5 shows the recommended footprints for the 18-pin PLCC. When laying out the IC footprints, as a general rule the footprint should extend approximately 10-15 mils past the outer edge of the PLCC lead. This provides a good solder fillet that will extend up the outer edge of the PLCC lead to yield a reliable solder joint that is easily inspected. The 70-80 mil length of the footprint should be a minimum, however a longer footprint can be used. It is recommended that the dimensions A and B never be less than the minimum width or length of the IC.

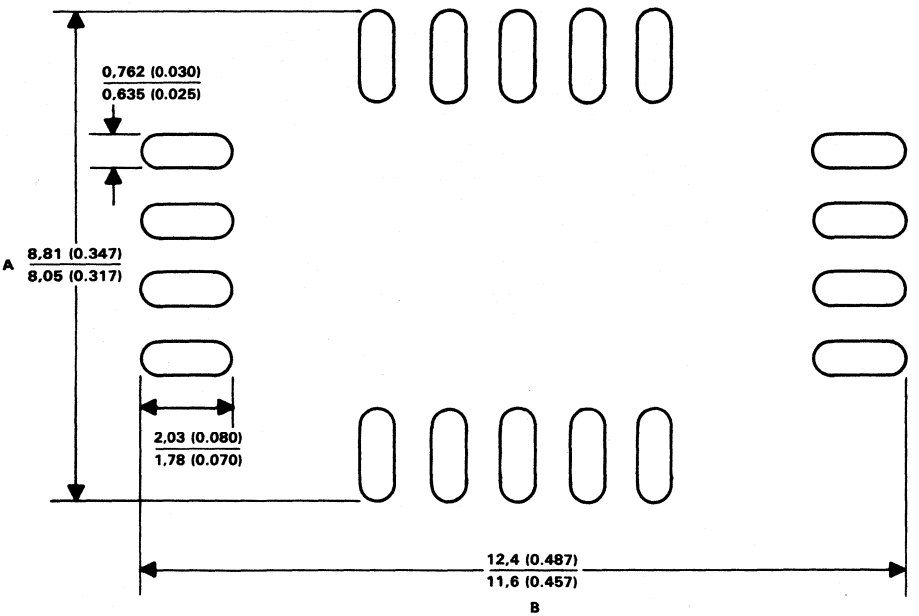


Figure 5. 18-Pin PLCC Footprint

Solder Paste Application

Solder paste can be applied using several methods: screening through a stencil or stainless steel mesh, pneumatic dispensing or by hand application with a syringe. Texas Instruments recommends screening through a stainless steel screen. The screen mesh must be chosen in accordance with the mesh of the solder paste to provide an adequate emulsion of the solder paste and to prevent screen clogging. In general an 80-100 mesh screen should be used with 200 mesh or finer solder paste particle. There are a number of factors that need to be considered when selecting a solder paste, a few key factors are as follows:

1. Particle size
2. Particle shape
3. Percentage of metal content
4. Temperature range

Component Placement

The components can be placed via several different modes into the still moist solder paste. In a production environment, the components are most efficiently placed with an automatic pick-and-place machine to achieve both speed and accuracy. Presently, pick-and-place machines can place between 600 and 600,000 components per hour and are priced accordingly. In a research and development environment, hand placement can be adequate due to the forgiving nature of surface mounting. When a component is placed off center it will tend to self-align during reflow due to the surface tension of the molten solder. Naturally there are limits to the amount of misalignment that can be corrected. Two important aspects of self-alignment are provision of adequate solder pad area, and proper placement of the solder pads with respect to the component.

Oven Drying

As solder pastes have evolved over the past several years, the drying process following component placement is not always necessary. In the past, drying was necessary to drive out the solvents in the solder paste. If the solvents were not driven out, the formation of solder balls was frequent due to the out gassing of the solvents prior to reflow. Today manufacturers of solder pastes report that drying is no longer necessary when using many of the new solder paste formulations. As a wide variety of solder pastes exists, it is necessary to consult the manufacturer before determining if drying is necessary in your process.

Solder Reflow

While several methods of solder reflow are available, vapor phase soldering has been the most successful and is becoming the industry standard.

Two types of vapor phase systems are the batch and the in-line. The batch system is a two-vapor system that uses a fluoroinert liquid such as FC-70 for the primary vapor and a clorofluorocarbon such as trichlorotrifluoroethane (R113) as the secondary liquid (see Figure 6). The secondary liquid has a lower boiling point (47.6°C) than the primary liquid (215°C) thus acting as a blanket to prevent loss of the expensive primary liquid. The in-line system (see Figure 7) is a single-vapor system using only a primary vapor (such as FC-70). The batch system is the forerunner of the in-line and is more suited to development and small production where the in-line is tailored to a mass production atmosphere requiring good throughput and minimal operating expense. Although the two systems are targeted to different markets their basic operation is the same. Both are capable of single and double sided surface mount.

Batch System Operation

The PC board complete with components is placed on an elevator and lowered into the secondary vapor. The elevator ascent-descent rate and dwell in the two vapor zones can be preset via the vapor phase machine front panel. The descent rate and hold time in the secondary zone should be set so as not to unnecessarily disrupt the secondary vapor blanket or cause defluxing of the solder paste. Lowering the board into the 215°C primary zone causes the solder to reflow. A dwell time of 10-30 seconds in the primary zone is generally sufficient for most PC boards. The dwell time in the primary zone is a function of the PC board mass. Once the solder is reflowed, the PC board is raised back into the secondary zone where the molten solder is allowed to solidify. In the batch system it is necessary to pay particular attention to the ascent-descent rate of the elevator as the disruption of the two-vapor zones will cause unnecessary loss of the expensive primary liquid.

In-Line System Operation

The operation of the in-line system is similar to that of the batch system except that there are no secondary vapor or dwell times with which to contend. The PC board is placed on a conveyor belt that transports it through the system at a constant speed. Passing through the vapor zone the solder becomes molten and solidifies as it moves toward the systems exit. Where the ascent-descent rate and dwell time are critical to the batch system, the conveyor speed is critical to the in-line system. The speed at which the conveyor should be set is also a function of the PC board mass.

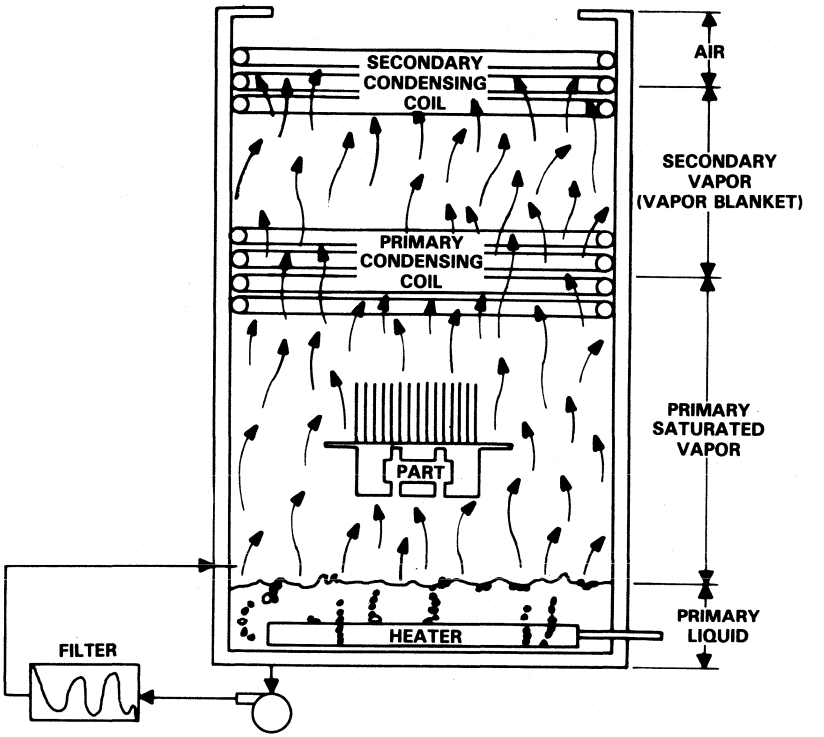


Figure 6. Vapor Phase Reflow System with Secondary Vapor Blanket

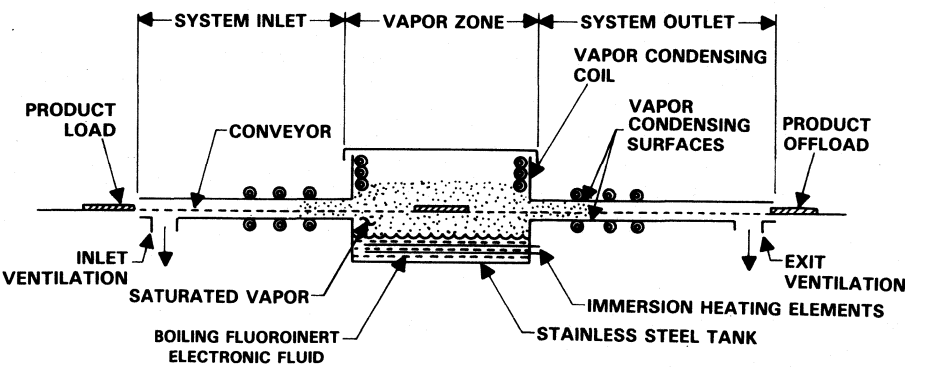


Figure 7. In-Line Single Vapor Heating System Schematic

Cleanup

Following the soldering process, it is necessary to remove the flux residues. These residues can be removed by traditional cleanup methods if the components have approximately 5 mils clearance to the PC board. One benefit of the PLCC with its J-leads is that it provides approximately 29 mils of clearance. Special soaking, agitation, or other methods will be necessary to provide adequate cleanup for components with less that 5 mils of clearance.

CONCLUSION

A brief overview of surface-mount technology has been given showing its advantages over standard plated-through-hole technology. Surface mounting is a cost-effective, sensible solution to the ever increasing demand for denser circuit boards. Detailed information about surface mounting is available from most major component and equipment manufacturers and through numerous technical articles on the subject. As the electronics industry strives to implement more functions in a given area, Texas Instruments believes surface mounting will become the predominant mounting technology of the future.

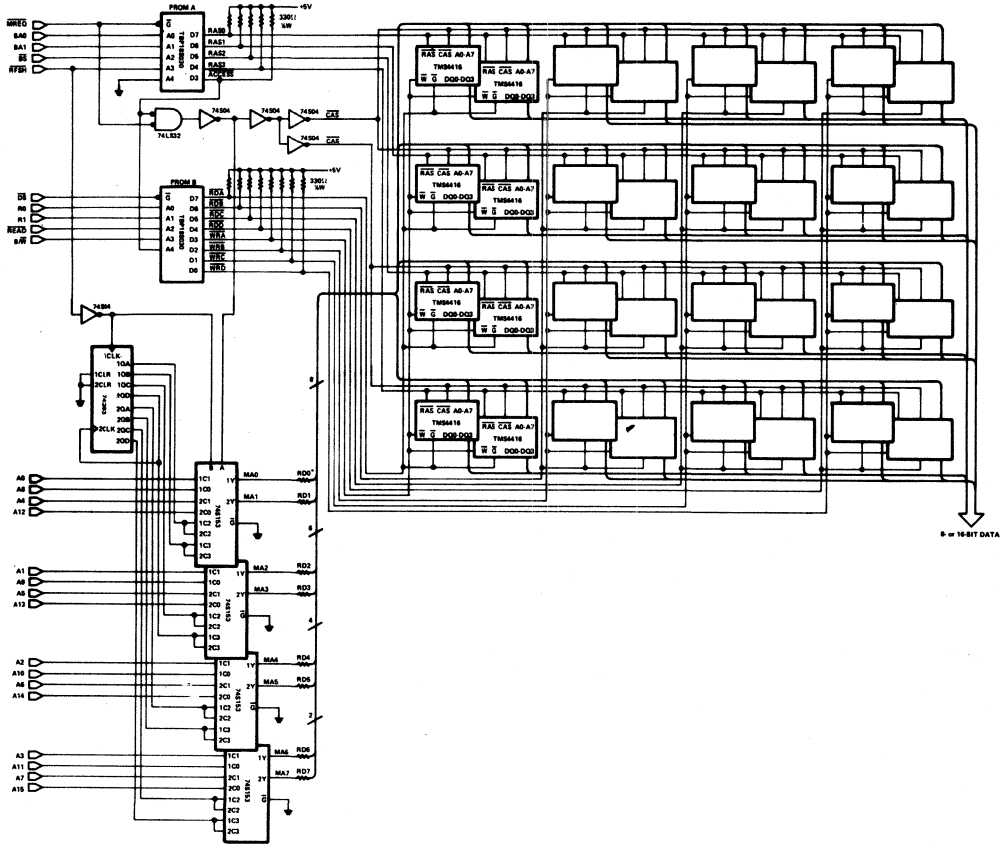
MOS Memory
Applications Engineering

Applications Brief

TTL DRIVERS FOR THE TMS4416-15

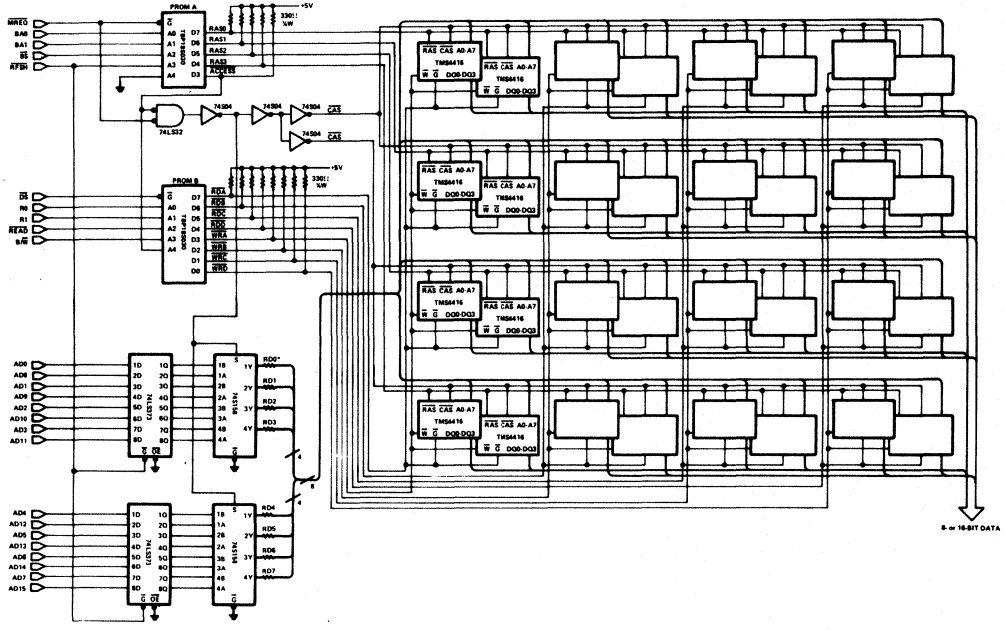
Some form of drive circuitry is needed when DRAMs are used with processors, such as the Z-80 or Z-8000. One possible solution involves the use of a precision delay line; however, a more cost-effective and efficient approach uses TTL devices as drivers. Two versions of TTL driver circuits are shown in Figures 1 and 2. The first figure shows the drive circuit for a memory array using TMS4416-15 DRAMs and the Z-80 processor; Figure 2 shows the same array configured for use with the Z-8000 processor. Both circuits are designed to drive 256K bytes of memory arranged in either 8- or 16-bit words. They provide all DRAM control signals, address multiplexing, and refresh address generation. The circuits shown for the Z-80 and the Z-8000 use the hidden refresh provided by these devices so that refresh/access arbitration is not necessary. Time delays were selected to provide maximum performance from the TMS4416-15 with off-the-shelf components. (Enhanced operation could be obtained by hand selecting components for single applications.) A comparison of the two circuits will reveal the differences between the two. The following description applies to both circuits.

The memory array is arranged as 4 banks of 8 TMS4416s. Two TBP18S030 PROMs decode and generate the control signals for the drive circuit. BA0 and BA1 are used to select which bank of memory will be accessed. $\overline{\text{MREQ}}$ and $\overline{\text{ACCESS}}$ are NORed and then delayed by 3 inverters to provide a $\overline{\text{CAS}}$ signal. The MUX signal that is used to switch the 74S153 multiplexers and propagate the column address to the memories is taken from the output of the first inverter in the $\overline{\text{CAS}}$ delay. $\overline{\text{CAS}}$ is connected to all the devices in the array. (Since $\overline{\text{RAS}}$ acts as a chip enable, $\overline{\text{CAS}}$ will only activate the memories in the bank that has $\overline{\text{RAS}}$ active; this keeps the power consumption of the array lower than using $\overline{\text{CAS}}$ as select logic.) Two $\overline{\text{CAS}}$ drivers are used to reduce the effects of the capacitive load of the DRAM $\overline{\text{CAS}}$ inputs. (This also improves drive characteristics and reduces noise.) Series damping resistors have been added to reduce ringing on the address lines. These resistors should be between 15 and 68 ohms, depending on the circuit board layout, and can be determined by examining the address waveforms with an oscilloscope and selecting a value that produces the cleanest signal. The desired 8- or 16-bit data word from the active bank is selected using R0, R1, and the $\overline{\text{READ}}$ line. R0 and R1 can be address lines from the Z-8001 or they can be generated from memory mapping logic. If the $\overline{\text{READ}}$ input is low during an access cycle, the output enable of the TMS4416 will be activated ($\overline{\text{RDA}}$-$\overline{\text{RDD}}$); a high input to $\overline{\text{READ}}$ will select a write output ($\overline{\text{WRA}}$-$\overline{\text{WRD}}$). Using this matrix, the memory can be divided into sixteen 16K × 8 or eight 16K × 16 blocks. The desired word width of the data output will be dependent on the microprocessor being used. For an 8-bit data bus the two data busses shown in the diagram would be connected in parallel. Since the Z-80 only directly accesses 64K of memory, bank select logic must be included in this memory system to provide higher order address lines. The design of the bank select circuitry has been left up to the user, but might include memory mapping or other logic.



* RD0–RD7 are determined empirically, see text.

FIGURE 1 - TMS4416 DRIVE CIRCUIT FOR THE Z-80 PROCESSOR



* RD0–RD7 are determined empirically, see text.

FIGURE 2 - TMS4416 DRIVE CIRCUIT FOR THE Z-8000

An external refresh counter has been added to the drive circuit for the Z-80 since the Z-80 internal refresh counter does not support 256 cycle refresh. (Application Brief DR-7 shows a circuit to add the extra refresh address bits similar to the implementation used here.) As the Z-8000 provides 9-refresh-address bits, its internal refresh counter was used.

A description of the signals used in both circuits previously illustrated is given in Table 1. Due to slight differences in the signals available from the Z-80 and Z-8000 processors, a slight modification of the interface between the processor and the TTL drive circuits shown will be required. The differences in the interface are shown in Figure 3. The $\overline{DS}$ signal is generated from the Z-80's $\overline{RD}$ and $\overline{WR}$ lines. The B/$\overline{W}$ input should be tied to a 5-10 kilohm pullup resistor. The $\overline{RFSH}$ signal can be decoded from the status lines of the Z-8000 as shown with the 74S138; however, it could also be done with other types of logic if desired. The address of the Z-8000A is only guaranteed valid for 35 ns so the address latches are necessary when using DRAMs with this microprocessor. $\overline{MREQ}$ is used to enable the 74LS373 transparent latches for both memory accesses and refresh cycles.

TABLE 1 – SIGNAL DESCRIPTION

SIGNAL NAME	DESCRIPTION
$\overline{MREQ}$	From the Z-80 or Z-8000, indicates address valid
BA0, BA1	Address for $\overline{RAS}$ selection, decoded from high order addresses.
$\overline{BS}$	Board select to designate DRAM access, decoded from high order addresses.
$\overline{RFSH}$	Z-80 output or decoded from the Z-8000 status outputs. Signals a refresh cycle.
$\overline{DS}$	Z-8000 output indicating data valid on the multiplexed address/data lines.
R0, R1	Address for read or write selection, decoded from high order addresses.
$\overline{READ}$	If low, indicates a memory read and if high, indicates a memory write.
B/$\overline{W}$	Indicates if the Z-8000 is doing a 8-or 16-bit memory access.
A0-A15	Z-80 address outputs
AD0-AD15	Z-8000 multiplexed address/data lines

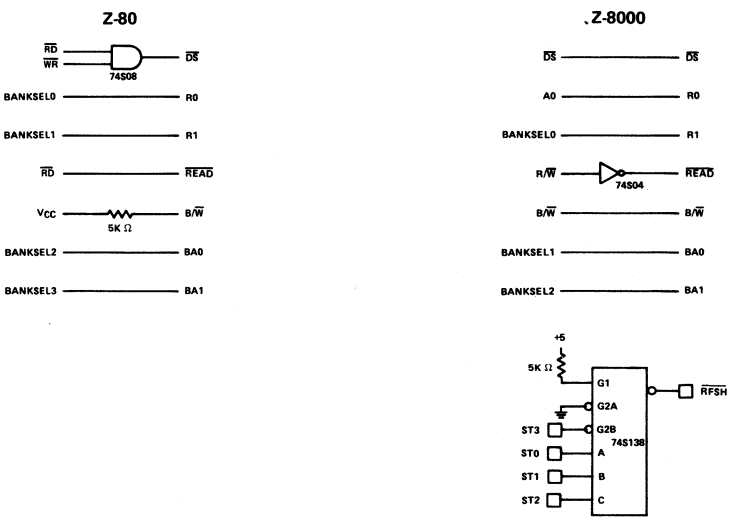


FIGURE 3 – INTERFACE CIRCUITRY DIFFERENCES

Tables 2 and 3 list the data for the PROMs to provide the control signals. Both the binary and hexadecimal programming data have been supplied.

TABLE 2 – PROM A PROGRAM

PIN NAME	A3	A2	A1	A0	D7	D6	D5	D4	D3	HEX
FIGURE NAME	$\overline{RFSH}$	$\overline{BS}$	BA1	BA0	$\overline{RAS0}$	$\overline{RAS1}$	$\overline{RAS2}$	$\overline{RAS3}$	ACCESS	
	0	X	X	X	0	0	0	0	1	0F
	1	0	0	0	0	1	1	1	0	77
	1	0	0	1	1	0	1		0	B7
	1	0	1	0	1	1	0	1	0	D7
	1	0	1	1	1	1	1	0	0	E7
	1	1	0	0	1	1	1	1	1	FF
	1	1	0	1	1	1	1	1	1	FF
	1	1	1	0	1	1	1	1	1	FF
	1	1	1	1	1	1	1	1	1	FF

TABLE 3 – PROM B PROGRAM

PIN NAME	$\overline{G}$	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	HEX
FIGURE NAME	$\overline{DS}$	B/$\overline{W}$	$\overline{READ}$	R1	R0	$\overline{RDA}$	$\overline{RDB}$	$\overline{RDC}$	$\overline{RDD}$	$\overline{WRA}$	$\overline{WRB}$	$\overline{WRC}$	$\overline{WRD}$	
	0	0	0	0	0	0	0	1	1	1	1	1	1	3F
	0	0	0	0	1	0	0	1	1	1	1	1	1	3F
	0	0	0	1	0	1	1	0	0	1	1	1	1	CF
	0	0	0	1	1	1	1	0	0	1	1	1	1	CF
	0	0	1	0	0	1	1	1	1	0	0	1	1	F3
	0	0	1	0	1	1	1	1	1	0	0	1	1	F3
	0	0	1	1	0	1	1	1	1	1	1	0	0	FC
	0	0	1	1	1	1	1	1	1	1	1	0	0	FC
	0	1	0	0	0	0	1	1	1	1	1	1	1	7F
	0	1	0	0	1	1	0	1	1	1	1	1	1	BF
	0	1	0	1	0	1	1	0	1	1	1	1	1	DF
	0	1	0	1	1	1	1	1	0	1	1	1	1	EF
	0	1	1	0	0	1	1	1	1	0	1	1	1	F7
	0	1	1	0	1	1	1	1	1	1	0	1	1	FB
	0	1	1	1	0	1	1	1	1	1	1	0	1	FD
	0	1	1	1	1	1	1	1	1	1	1	1	0	FE
	1	X	X	X	X	1	1	1	1	1	1	1	1	FF

The TTL drive circuits previously described allow the TMS4416-15 to operate at maximum speed. Although there are many ways to provide the necessary control signals for DRAMs, the drive circuits described will provide insight into the control logic that is necessary to use dynamic RAMs. TTL circuitry was selected in order to avoid the cost of a precision delay line.

TMS4416/7220 GRAPHICS

As the increased activity in computer graphics grows, the need for dedicated graphics peripherals and video memory becomes apparent. The NEC 7220 is currently a good answer for a high resolution single chip graphics controller. The 7220 provides all of the necessary graphics primatives for line, arc, and rectangle drawing, as well as area fill routines. Signal timings are easily adapted with external logic to provide the proper memory and video timings, with programmable features allowing the user to do in software what has typically been implemented in hardware. To take advantage of the 7220's wide spectrum of operation requires a memory that is also well adapted to graphics applications. The TMS4416 16K × 4 dynamic RAM provides such a memory, with modularity and bandwidth advantages over 64K × 1 memories. The architecture of the TMS4416 provides an output enable function (relieving the need for databus buffers), faster access times and a 4X bandwidth improvement over X1 devices of the same speed. Although 64K × 1 nibble mode parts out perform standard 64K × 1s, they can not match the bandwidth of the TMS4416 and they require more memory control circuitry to perform the same function. The modularity of the TMS4416 offers efficient memory usage in many applications and is well suited for both single and multiplane memory systems.

This application report describes a design coupling the 7220 and the TMS4416 in a single plane, bit mapped graphics system. The main objective is to provide a detailed example of the necessary memory interface. While the design does not use all of the capabilities of the 7220 (DMA, Zoom, Light Pen, etc.) it does provide an easily adaptable example that can be tailored to many applications. This particular system can be switched between a 512 × 240 noninterlaced and 512 × 480 interlaced display by changing a single 7220 parameter byte. To simplify the host interface an existing Z80A based computer was used to communicate to the 7220 in a Multibus* system, with all the programming done in BASIC.

To evaluate the design, calculations of the memory and video requirements will be given with a brief discussion of key points of interest. Measured drawing times for an arc and area fill are included to provide some feel for the drawing speed of the 7220.

Referring to the schematic (Figure 1), the graphics board can be divided into five functional blocks: Multibus* interface, 7220, memory control, display memory, and video output circuitry. Four of the blocks will be discussed while a detailed understanding of the 7220 is left to the reader (NEC provides a 7220 Design Manual which is essential to understand 7220 operation).

A simple Multibus interface has been implemented for control of the graphics system. The low order eight bits of the data bus are buffered with a 74LS640 transceiver. This transceiver is controlled by $\overline{\text{IORC}}$ and output Y0 of the 74LS138 (board select logic). The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals are derived from $\overline{\text{IORC}}$ and $\overline{\text{IOWC}}$ in conjunction with the board select. The $\overline{\text{XACK}}$ signal, required to terminate all I/O operations is generated by using the board select to enable a 74LS241 whose input is tied to ground. The Multibus signal timings were sufficient to meet the 7220 specifications without the use of complicated logic.

The memory array is made up of four TMS4416s providing 262,144 pixels. With the $\overline{\text{CAS}}$ circuitry shown, the memory space can be upgraded to sixteen TMS4416s for 1,048,576 pixels which allows the maximum display resolution (1024 × 1024) of the 7220 to be implemented. The TMS4416 offers improved modularity over the 64K × 1 (which relates to less wasted memory space) and is well adapted for multiplane memory systems. A four plane color system of 512 × 512 display resolution requires sixteen 64K DRAMs. For the TMS4416 application, the memory breaks into four physically separate planes which are simultaneously accessed once per display cycle. With 64K × 1s, the four memory planes reside in the same physical memory, and require four separate accesses to memory per display cycle. This significantly reduces the obtainable bandwidth and also requires the addition of complex control circuitry. The output enable function and common I/O of the TMS4416 alleviate the need for databus buffering further reducing the circuit component count.

The memory control timing is generated by dividing the dot clock with a 74S163 and using the appropriate outputs to clock several 74LS74s for proper placement of the memory control signals. This approach may seem complicated, however it allows maximum flexibility in generating the control signals by the choice of the clock connections. The falling edge of ALE takes $\overline{\text{RAS}}$ low, latches the memory addresses and enables the 74LS74s in the memory control circuitry (see Figure 2). On the next rising edge of 2 × WCLK (edge A), MUX goes low switching the memory addresses from row to column via two 74S157s. The row addresses correspond to 7220 addresses AD-0 through AD-7 and the column addresses correspond to AD-8 through AD-13. The next rising edge of clock A (edge B) takes $\overline{\text{CASSTB}}$ low. $\overline{\text{CASSTB}}$ is then used in conjunction with AD-14 and AD-15 to derive four $\overline{\text{CAS}}$ signals through a 74LS139 for easy memory expansion. It is necessary to select the memory with $\overline{\text{CAS}}$ instead of $\overline{\text{RAS}}$, because the 7220 does not provide a status indicating the type of memory operation to be performed (display, refresh, or RMW). (Normally $\overline{\text{RAS}}$ is used for memory selection to reduce system power consumption and noise induced by $\overline{\text{RAS}}$ switching currents.) The rising edge of clock C (edge C) after $\overline{\text{CAS}}$, takes the memory output enable ($\overline{\text{G}}$) signal low. The $\overline{\text{G}}$ signal is controlled such that it is only active on display and RMW cycles; for refresh cycles, $\overline{\text{G}}$ is held high by the 7220 $\overline{\text{DBIN}}$ and BLANK signals. Generating four $\overline{\text{CAS}}$ signals and a single $\overline{\text{G}}$ signal

*Trademark of Intel Corporation.

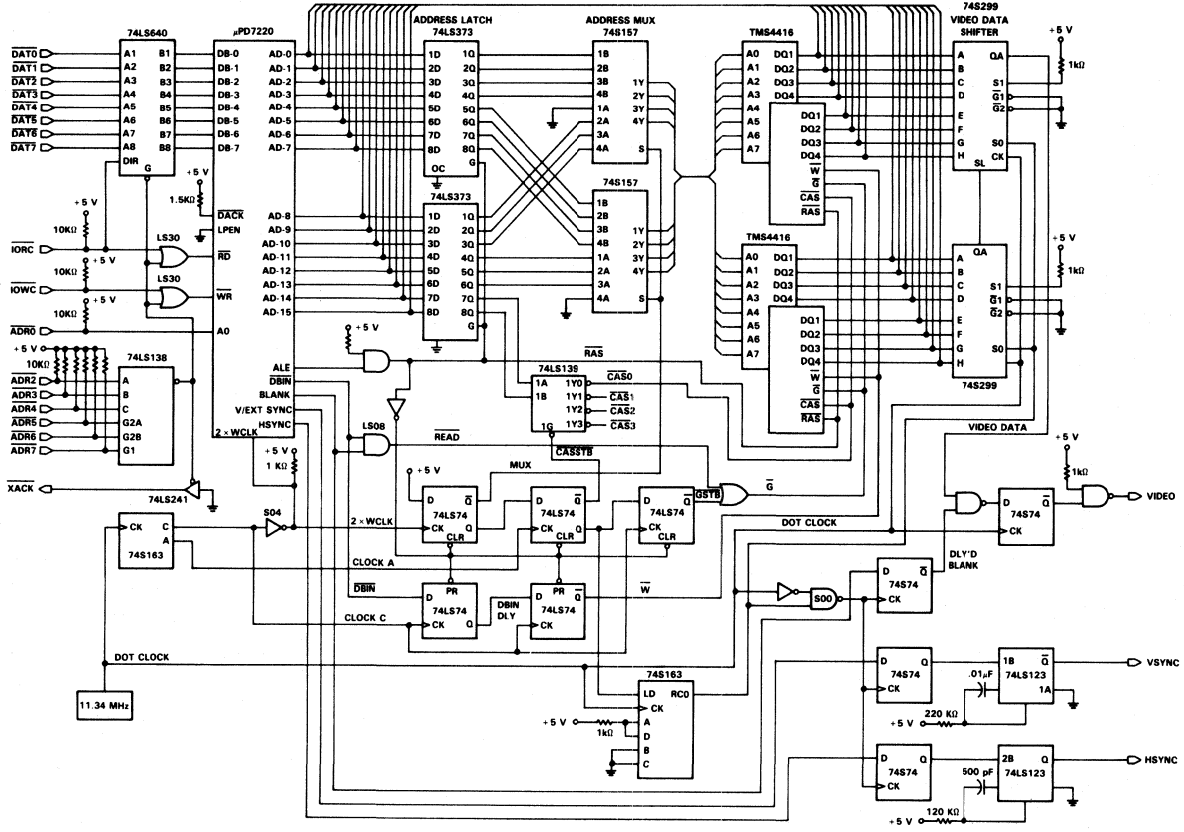


Figure 1. TMS4416/7220 Interface

allows the use of multiple rows of memory since both $\overline{CAS}$ and $\overline{G}$ have to be low for the TMS4416 outputs to be active (see TMS4416 operation, 1982 MOS Memory Data Book). The cycle is terminated by the rising edge of ALE (edge G).

On RMW cycles, the 7220 uses the $\overline{DBIN}$ signal to gate data from the memory onto the bus signifying the read operation. The rising edge of $\overline{DBIN}$ is then used to disable the $\overline{G}$ signal terminating the read portion of the cycle (see Figure 3). The 7220 does not provide a separate write signal so the memory control circuit must use the presence of $\overline{DBIN}$ to generate the write signal. This is accomplished by shifting $\overline{DBIN}$ two clock C cycles (edge E) with two 74LS74s. Again the rising edge of ALE terminates the memory cycle (edge G).

The 7220 runs at a relatively slow clock speed (1.4 MHz) in this design allowing the use of Low Power Schottky components for most of the memory control circuitry. The necessary memory calculations given below show the actual margins and also provide an easy means for determining the maximum speed of the design with Schottky components. The critical memory timings to be covered are: $\overline{RAS}$ precharge, row address setup and hold, $\overline{CAS}$ access, data valid to write enable time and refresh interval.

$\overline{RAS}$ Precharge Time

$$t_{RP} = t_{RW} - t_{S(74LS08)}$$

where: t_{RW} = ALE width (MIN, 7220 Spec.)
t_S = Skew between t_{PHL} and t_{PLH}, 74LS08

thus: $t_{RP} = [1/3(705) - 10]$ ns
$= 225$ ns

Row Address Setup Time

$$t_{ASR} = 1/2(t_{CLK}) - t_{AD} - t_{PLH(74LS373)} - t_{PLH(74S157)} + t_{RF} - t_{PHL(74LS08)}$$

where: t_{CLK} = 2 × WCLK cycle time
t_{AD} = Address/data delay from 2 × CCLK (MAX, 7220 Spec.)
t_{RF} = ALE delay from 2 × CCLK (MIN, 7220 Spec.)

thus: $t_{ASR} = [1/2(705) - 130 - 18 - 7.5 + 20 + 4]$ ns
$= 221$ ns

Row Address Hold Time

$$t_{RAH} = 1/2(t_{CLK}) - t_{PHL(74LS08)} + t_{PLH(74LS74)} + t_{PHL(74S157)}$$

thus: $t_{RAH} = [1/2(705) - 20 + 6 + 6]$ ns
$= 344.5$ ns

$\overline{CAS}$ Access Time

A. Display

$$t_{CAC} = 7(t_{DCLK}) - t_{PLH(74S163)} - t_{PHL(74LS74)} - t_{PHL(74LS139)} - t_{su(74S299)}$$

where: t_{DCLK} = Dot clock cycle time

thus: $t_{CAC} = [7(88) - 15 - 40 - 33 - 7]$ ns
$= 521$ ns

B. RMW cycles

$$t_{CAC} = 5.5(t_{CLKA}) - t_{PHL(74S04)} - t_{PHL(74LS74)} - t_{PHL(74LS139)} - t_{DIS}$$

where: t_{CLKA} = Clock A cycle
t_{DIS} = Input data setup to 2 × CCLK (MIN, 7220 Spec)

thus: $t_{CAC} = [5.5(176) - 5 - 40 - 33 - 40]$ ns
$= 850$ ns

Data Valid to Write Enable

$$t_{DS} = 1/2(t_{CLK}) - t_{AD} - t_{PLH(74S04)} + t_{PLH(74LS74)}$$

thus: $t_{DS} = [1/2(705) - 5 - 130 + 6]$ ns
$= 223.5$ ns

Refresh Interval

For this circuit the least significant address lines correspond to the DRAM row addresses which are incremented every display cycle. This provides a refresh rate given by:

$$\text{Refresh Interval} = (256/\text{number of display words}) \times \text{line time} = (256/32) \times 63.5\ \mu s = .5\ ms$$

Therefore the memory is refreshed by normal display accesses and the 7220 refresh feature is not needed for this design.

A comparison of the previous calculations to the DRAM specification indicates there are no memory speed restrictions for the design. To attain the maximum speed of this particular design, Schottky components may be substituted and the appropriate parameters placed into the above equations to determine the maximum dot clock frequency. By using high performance logic, a dot clock rate of approximately 22 MHz can be used.

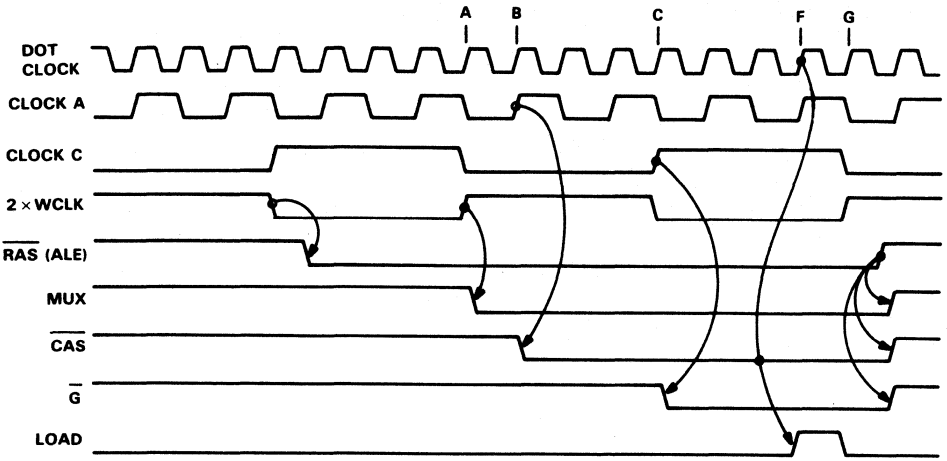


Figure 2. Display And Refresh Cycle Timing

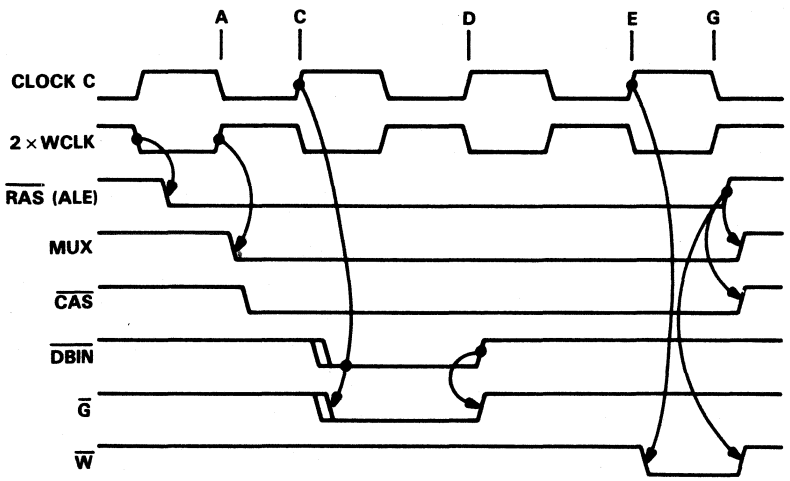


Figure 3. RMW Cycle Timing

The video output circuitry closely resembles that provided in the 7220 Design Manual. The major difference being the manner in which the 74S299 load pulse is generated. It was decided to use the ripple carry out of a 74S163 instead of gating the clock outputs together. The $\overline{CAS}$ signal enables the 74S163 and six dot clocks later (edge F) the ripple carry out will go high (see Figure 2) providing a video load pulse at the end of the display cycle (edge G). This reduces hardware and provides an easy means for varying the position of the load pulse within the memory cycle if necessary. Some applications may require the video load pulse to occur earlier in the display cycle which is accomplished by changing the input strapping of the 74S163. A video load pulse will occur on every memory access; however, on refresh and RMW cycles, the display is blanked preventing any disturbance of the display. Since the first word of video information on each horizontal scan is not valid until the end of the first display cycle, video unblanking must be delayed for one display cycle. This is accomplished by clocking the 7220 BLANK signal with the NAND result of the inverted dot clock and ripple carry out through a 74S74. The video is then synchronized with the dot clock and output to the monitor. A 74LS123 is used to provide the proper horizontal and vertical drive signals to the monitor. Although the 7220 can be programmed for the horizontal sync width and the vertical sync width, some monitors require long drive times that can only be implemented with external logic.

Providing the correct video information to the monitor requires several calculations to determine the necessary parameters that must be supplied to the 7220 upon initialization. The 7220 Design Manual goes through detailed calculations for determining these parameters when the designer is in the specification stage of a design. For this design the monitor specifications and dot clock rate were assumed and the other parameters derived accordingly. The necessary specifications and calculations are given below.

Horizontal frequency = 15.75 kHz
Vertical frequency = 60 Hz
Horizontal blanking = 11 μs nominal
Vertical blanking = 900 μs nominal
Dot clock = 11.34 MHz
$2 \times$WCLK = 1.42 MHz (Dot clock/8)
Word time = 1.41 μs [2(1/2 $\times$ WCLK)]
Line time = 63.5 μs (1/Horizontal frequency)
Pixel time = 88.18 ns (1/Dot clock)

From the line time and pixel time, the total number of pixels per horizontal scan can be calculated.

$$\begin{aligned} \text{Pixels} &= t_{LINE}/t_{PIXEL} \\ &= 63.5\ \mu s/88.18\ ns \\ &= 720 \end{aligned}$$

The total number of words per horizontal scan is given by:

$$\begin{aligned} WT &= \text{Pixels}/16 \\ &= 720/16 \\ &= 45 \end{aligned}$$

(Since the 7220 uses a 16-bit word)

The total word count is then divided between displayed words and blanked words. For the monitor used, the only restriction on the horizontal parameters is that the sum of horizontal front porch, back porch and sync be approximately equal to the nominal horizontal blanking time (11 μs). The horizontal drive to the monitor is set by the 74LS123. A horizontal resolution of 512 pixels would require 32 display words and leave 13 words for horizontal blanking. Setting Horizontal Back Porch (HBP) = 5, Horizontal Front Porch (HFP) = 5, and Horizontal Sync (HS) = 3 meets all 7220 constraints except for light pen use (requires HFP > 6 words), and also satisfies the monitor horizontal blanking time.

$$\begin{aligned} \text{Horizontal blank} &= 13 \times 1.41\ \mu s \\ &= 18.33\ \mu s \end{aligned}$$

Calculations to determine the vertical blanking parameter must also be made.

$$\begin{aligned} \text{Total number of lines} &= (1/\text{vertical frequency})/\text{line time} \\ &= (1/60)/63.5\ \mu s \\ &= 262.3\ \text{(use 263)} \end{aligned}$$

The total number of lines is also broken into active and blanked lines. In this application it was desired to neglect aspect ratios and display as much on the screen as possible and stay within the monitor specifications. For this reason, it was decided to display 240 lines and blank 23 lines for 512×240 noninterlaced and 512×480 interlaced display resolution. Again the vertical drive is set by a 74LS123 and there are no restrictions placed on the breakdown of the vertical blank parameters by the monitor or the 7220, allowing random division of the 23 blanked lines. The following parameters were chosen: Vertical Back Porch (VBP) = 3 lines, Vertical Front Porch (VFP) = 2 lines, and Vertical Sync (VS) = 18 lines.

$$\begin{aligned} \text{Vertical blank} &= \text{Blanked lines} \times \text{one line time} \\ &= 23 \times 63.5\ \mu s \\ &= 1.46\ ms \end{aligned}$$

Several points of interest relating to the choice of the horizontal and vertical parameters are given in the following paragraphs.

A. Dynamic RAM refresh, if necessary, is only done during horizontal and vertical sync which needs to be long enough to allow sufficient memory refresh.

B. If dynamic RAM refresh is enabled, then drawing can only be done during front and back porch times. This can degrade drawing time significantly if these times are short.

C. To maximize the drawing time and reduce wasted cycles, the horizontal parameters should be chosen in accordance with memory refresh requirements. When memory refresh is needed, the horizontal front and back porch parameters should be selected as multiples of 2 word times (one RMW cycle equals 2 word times) if possible.

Example: For HBP = 5, two RMW cycles (4 word times) would be performed and one cycle (1 word time) would be wasted. Choosing HBP equal to four or six eliminates the one wasted state. Of course, minimum 7220 requirements must be met also.

The parameters for this design were choosen for no refresh operation and to support as many 7220 operating modes as possible. Table I gives a quick summary of the video parameters.

These parameters can then be translated into a format needed to program the 7220 (see Table II). Writing these commands and parameters to the correct 7220 address location (A0 = 0, Parameter into FIFO; A0 = 1, Command into FIFO) results in setting the video control commands, ends idle mode and unblanks the display. Upon initialization, the 7220 can then be programmed for drawing using the various graphics primatives. The 7220 Design Manual contains numerous examples illustrating the necessary steps for drawing. To switch to 512×480 interlaced mode parameter P1 of the Reset command needs to be changed to 1B hex (see Table II) and the Cursor and Character Characteristics (CCHAR) command needs to be set appropriately (Blink Rate parameter greater than zero).

Table I. Video Parameters

Parameter	Value	Parameter	Value
Active Words	32	Active Lines	240
Blanked Words	13	Blanked Lines	23
HS	3	VS	18
HBP	5	VBP	3
HFP	5	VFP	2

Table II. 7220 Initialization Data

Commands And Parameters	Address A0	Data (Hex)	Function
Reset	1	00	Reset to idle state
P1	0	12*	
P2	0	1E	Active words-2
P3	0	42	HS-1, VS low bits
P4	0	12	VS high bits, HFP-1
P5	0	04	HBP-1
P6	0	02	VFP
P7	0	F0	Active display lines
P8	0	0C	VBP
VSYNC	1	6F	Master video sync
START	1	6B	End idle mode

*Set for graphics mode, noninterlaced, no refresh, drawing during retrace only; for interlaced operation P1 = 1B (hex).

To illustrate the drawing speed of the 7220, drawing times for arc and area fill routines with and without memory refresh were measured. The 7220 also provides Flash Mode drawing where drawing is done during display and retrace. While this yields extremely fast drawing times there is considerable disturbance to the display when drawing is in progress. The drawing time results are shown in Table III.

This Application Report has demonstrated how a designer might incorporate the TMS4416 into a graphics system with the 7220. No attempt has been made to detail the interface or communication between the host processor and the 7220 as so many variants exist (see 7220 Design Manual). The TMS4416 requires minimal circuitry to generate a dense, low cost, high performance memory array for the 7220.

MOS Memory
Applications Engineering

Table III. Drawing Times

Routine	Pixels Drawn	Refresh	No Refresh	Flash Mode
Arc Radius = 96	69	1,079 μs	704 μs	191.8 μs
Area Fill x = 400 y = 200	80,000	926.9 ms	686 ms	227.4 ms

Applications Brief

TMS4416/TMS4500A EVALUATION BOARD

This application note illustrates memory system implementation using the TMS4416/TMS4500A evaluation board (Photo shown in Figure 1). The board measures 3'' X 5.5'' and is populated with a TMS4500A DRAM controller and 16 TMS4416s (16K X 4 Dynamic RAMs); this system provides for 128K bytes of static appearing memory and requires a single 5-volt supply. The interconnection bus at the board edge and the flexibility of the TMS4500A makes the board adaptive to almost any system. This board was developed by Texas Instruments to allow construction of several processor systems without redesign of the memory section for each system. It is beyond the scope of this article to cover every microprocessor interface, although several popular microprocessor interfaces are covered in the TMS4500A User's Manual.

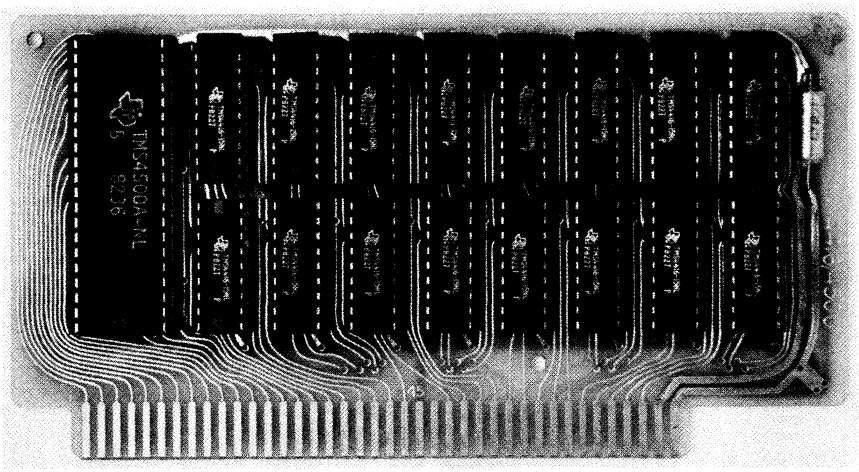


FIGURE 1 – TMS4416/TMS4500A EVALUATION BOARD

The TMS4416/TMS4500A board is arranged as two rows of 8 devices (see Figure 2). Row 0 and Row 1 are selected by the $\overline{RAS0}$ and $\overline{RAS1}$ signals, respectively. The board is then subdivided into four blocks of 32K bytes that are controlled by the $\overline{WR1}$-$\overline{WR4}$ and $\overline{RD1}$-$\overline{RD4}$ signals. The strapping of $\overline{WR1}$-$\overline{WR4}$ and $\overline{RD1}$-$\overline{RD4}$ allows the board to be configured as 32K X 32 bits, 64K X 16 bits, or 128K X 8 bits. Table 1 shows the typical strapping needed for the various word widths. Several examples of how the $\overline{WR}$ and $\overline{RD}$ signals can be used will show the versatility of the TMS4416/TMS4500A board.

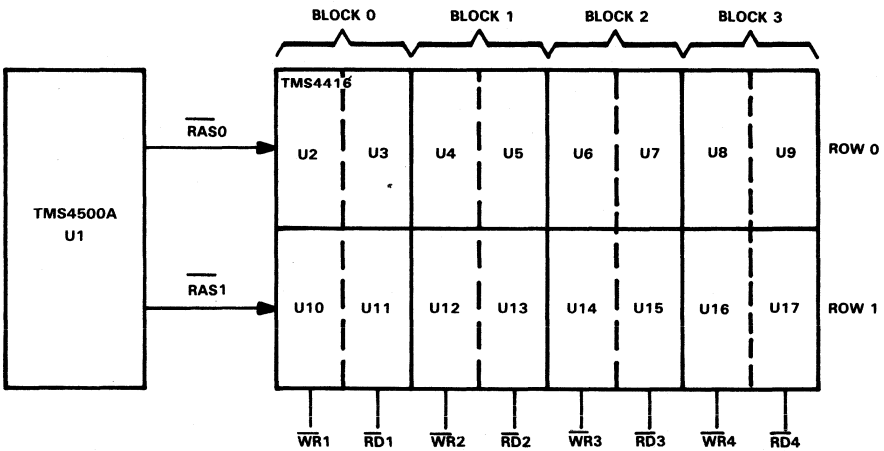


FIGURE 2 – TMS4416/TMS4500A BOARD LAYOUT

TABLE 1 – READ AND WRITE SIGNAL STRAPPING CONFIGURATION

CONFIGURATION	SIGNAL STRAPPING	TYPE OF CONTROL
128K X 8	$\overline{SWR1} = \overline{WR1}$, $\overline{SWR2} = \overline{WR2}$, $\overline{SWR3} = \overline{WR3}$, $\overline{SWR4} = \overline{WR4}$ $\overline{SRD1} = \overline{RD1}$, $\overline{SRD2} = \overline{RD2}$, $\overline{SRD3} = \overline{RD3}$, $\overline{SRD4} = \overline{RD4}$	Separate Control
64K X 16	$\overline{SWR1} = \overline{WR1} = \overline{WR2}$, $\overline{SWR2} = \overline{WR3} = \overline{WR4}$ $\overline{SRD1} = \overline{RD1} = \overline{RD2}$, $\overline{SRD2} = \overline{RD3} = \overline{RD4}$	Combined Pairs
32K X 32	$\overline{SWR1} = \overline{WR1} = \overline{WR2} = \overline{WR3} = \overline{WR4}$ $\overline{SRD1} = \overline{RD1} = \overline{RD2} = \overline{RD3} = \overline{RD4}$	All Combined

NOTES:
1. $\overline{WRX}$ = Write signal for any block.
2. $\overline{RDX}$ = Read signal for any block.
3. $\overline{SWRX}$ = User supplied system write signal.
4. $\overline{SRDX}$ = User supplied system read signal.

The REN1 input on the TMS4500A selects which row of devices is selected by controlling the $\overline{RAS}$ (Row Address Strobe) signals (REN1 low selects $\overline{RAS0}$, REN1 high selects $\overline{RAS1}$). When a row of memory is accessed ($\overline{RAS0}$ low or $\overline{RAS1}$ low), all the devices in that row are active which allows the user to manipulate each half-block within a row separately or collectively. As an example, strapping $\overline{WR1}$-$\overline{WR4}$ and $\overline{RD1}$-$\overline{RD4}$ for 64K X 16 operation as shown in Table 1 combines the 32-bit data bus to form two 16-bit data busses that can be used in 16-bit systems as shown in Figure 3. The I/O function is controlled by the combination of $\overline{WR1}$-$\overline{WR2}$, $\overline{RD1}$-$\overline{RD2}$ (Blocks 1 and 2) and $\overline{WR3}$-$\overline{WR4}$, $\overline{RD3}$-$\overline{RD4}$ (Blocks 3 and 4). It is then possible to read and/or write to each block by appropriate control of the $\overline{WR}$ and $\overline{RD}$ signals.

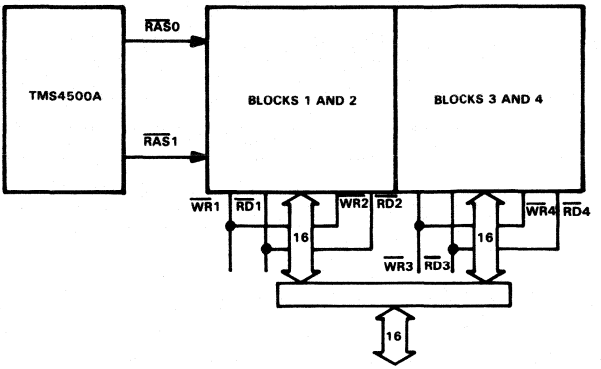


FIGURE 3 – 64K X 16 CONFIGURATION

Another example takes advantage of having a 32-bit word available but only an 8-bit data bus. To take advantage of this, a 74LS139 selects the $\overline{WR}$ and $\overline{RD}$ signals and D0-D7 of each block are tied together to form an 8-bit bus (See Figure 4). A write cycle enables 1G allowing the 1A and 1B signals to select the block to be written to. A read cycle enables 2G allowing the 2A and 2B signals to select which block will be read. On a read cycle, the 2A and 2B signals can be sequenced, causing successive activation of the $\overline{RD}$ lines to rapidly access all 32 bits over the 8-bit bus (See Figure 5). This configuration makes full use of the output enable ($\overline{G}$) function on the TMS4416 to decrease memory access times. Similarly the WR lines can be manipulated to accomplish fast writes into the DRAM array.

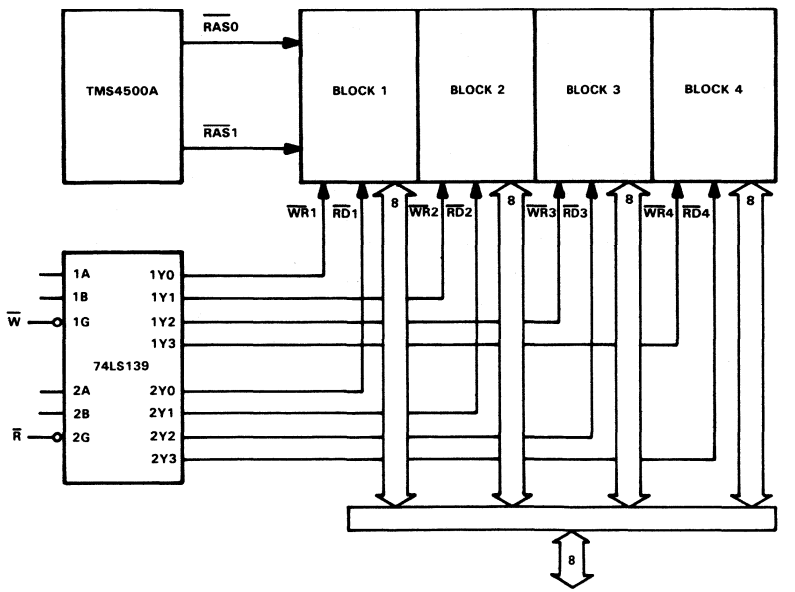


FIGURE 4 – 128K X 8 FAST ACCESS CONFIGURATION

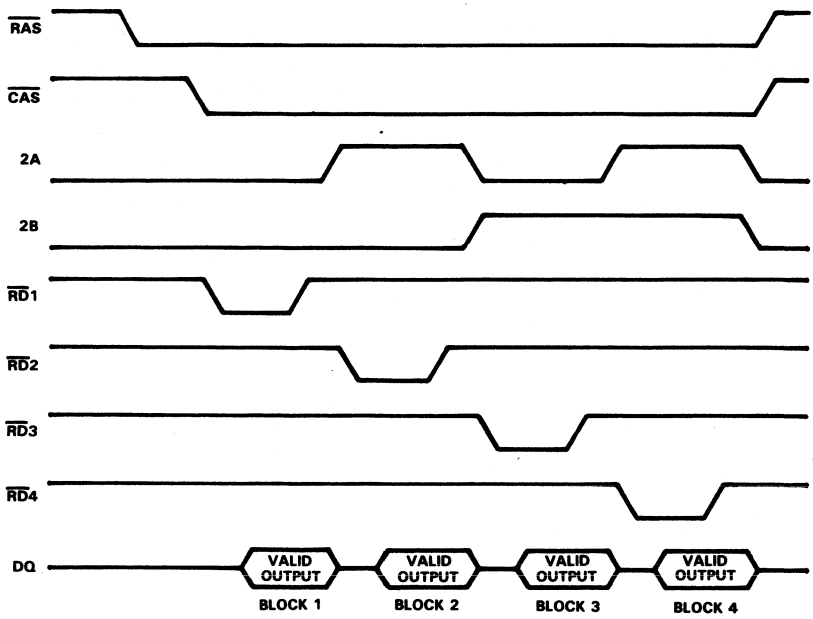


FIGURE 5 – FAST ACCESS READ TIMING

The upgrade to next generation parts and expanded memory requirements are also taken into account on the TMS4416/TMS4500A board. When 64K X 4 parts become available, they will be pin-compatible with the 16K X 4, allowing the user to upgrade his board to 512K bytes of memory with no added interfacing. The TMS4416 disregards two of the column addresses supplied to it from the TMS4500A (CA0, CA7) which are not needed to address its 16K of memory. These two extra address lines will be used to complete the addressing needed for the 64K X 4 making upgrade a matter of installing the new devices.

The TMS4416/TMS4500A memory board demonstrates the use of a versatile, and expandable memory suitable for most any system.

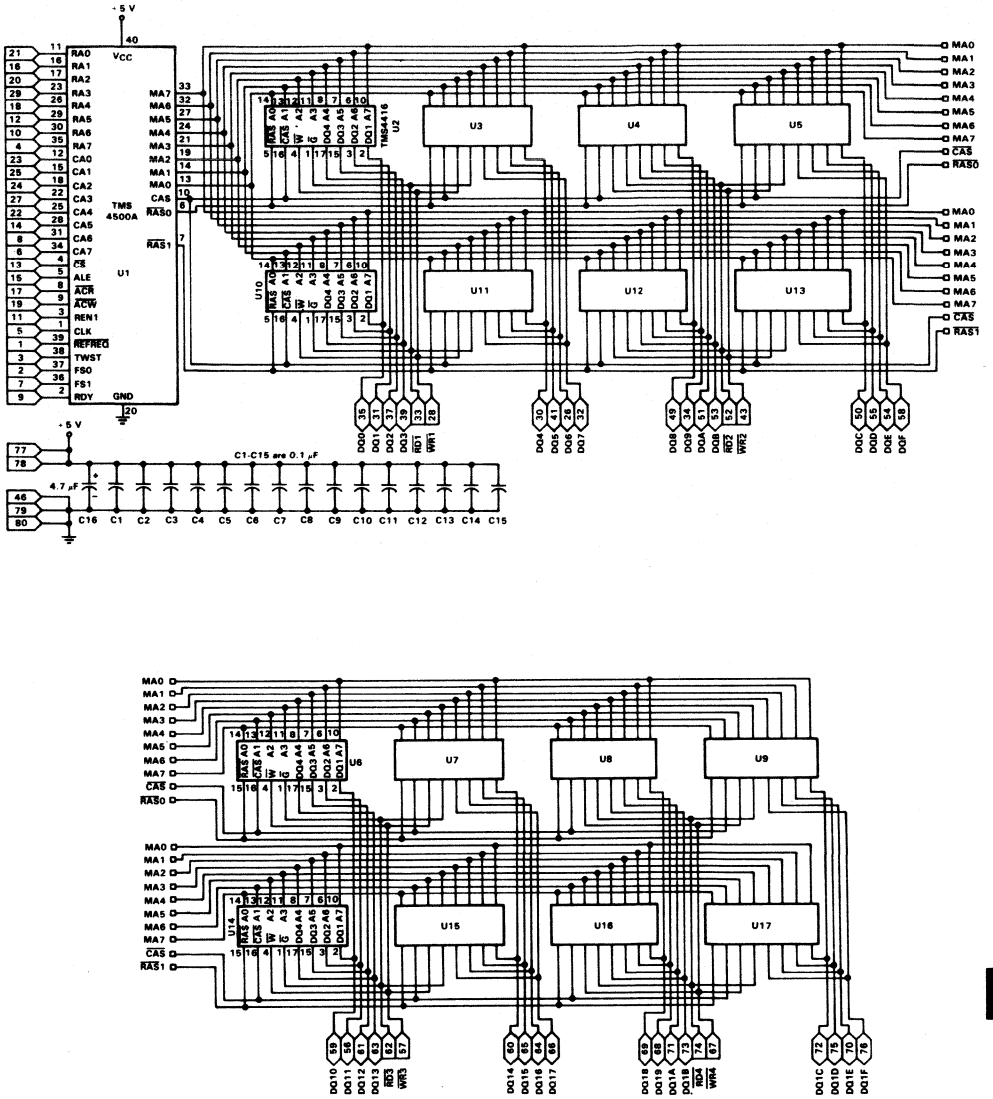


FIGURE 6 — TMS4416/TMS4500A BOARD SCHEMATIC

Applications Brief

TMS4500A
ALE AND $\overline{ACX}$ TIMING

This application brief describes the timing diagrams for several configurations that can be achieved with the TMS4500A by controlling ALE and $\overline{ACX}$. ($\overline{ACX}$ refers to either $\overline{ACR}$ or $\overline{ACW}$.) Example timing diagrams are given that illustrate the pertinent edge timings of ALE and $\overline{ACX}$ and their impact on system timing requirements.

The timing diagram given in Figure 1 shows ALE leading $\overline{ACX}$. The falling edge of ALE latches the $\overline{CS}$, REN1, RA0-RA7, and CA0-CA7 inputs (not shown in the diagram); if $\overline{CS}$ is valid, $\overline{RAS}$ will go low $t_{AEL-REL}$ after ALE low. $\overline{ACX}$ going low has two functions: the MA0-MA7 outputs are switched from the row addresses to the column addresses, and $\overline{CAS}$ will go low when these addresses become valid. The access time of the TMS4500A (ALE low to $\overline{CAS}$ low) is specified as $t_{AEL-CEL}$ providing $\overline{ACX}$ goes low less than $t_{AEL-CEL} - t_{ACL-CEL}$ after ALE. If this condition is not met then the access time increases and $\overline{CAS}$ low is measured from the low-going edge of $\overline{ACX}$ instead of ALE ($t_{ACL-CEL}$). The rising edge of ALE brings $\overline{RAS}$ high and causes the inputs at RA0-RA7 to be output as addresses on MA0-MA7. (Input latches for RA0-RA7 are transparent latches.) The rising edge of $\overline{ACX}$ brings $\overline{CAS}$ high and terminates the memory access cycle. The edge placements of ALE and $\overline{ACX}$ can vary from this example giving rise to $\overline{RAS}$ and $\overline{CAS}$ timings not explicitly shown in the MOS Memory Data Book as explained below.

Figure 2 illustrates the case where ALE overlaps $\overline{ACX}$. In this case, the falling edges of ALE and $\overline{ACX}$ have the same function as explained in the first example although the rising edges take on a little different function. Referring to Figure 2, it can be seen that the rising edge of $\overline{RAS}$, $\overline{CAS}$, and the switching of MA0-MA7 are controlled by the rising edge of $\overline{ACX}$. The rising edge of ALE has no control in this example. Because $\overline{ACX}$ brings $\overline{RAS}$ high, the precharge time (t_{RP}) required by DRAMs is initiated from the rising edge of $\overline{ACX}$ and terminated by the subsequent falling edge of ALE. This timing can be helpful in a system that cannot meet $\overline{RAS}$ precharge time initiated from ALE.

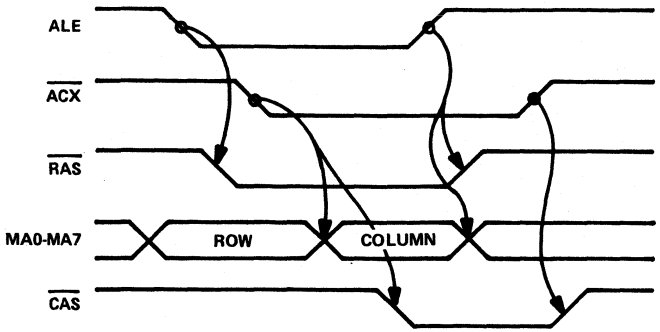


FIGURE 1 – ALE LEADING $\overline{ACX}$

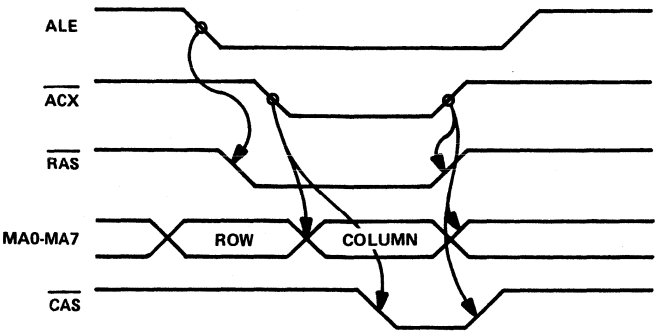


FIGURE 2 – ALE OVERLAPPING $\overline{ACX}$

The next example shows $\overline{ACX}$ prior to or coincident with ALE (see Figure 3). When $\overline{ACX}$ falls prior to or coincident with ALE, the falling edges of $\overline{RAS}$, $\overline{CAS}$, and the switching of MA0-MA7 are controlled by the falling edge of ALE. In this case, the TMS4500A provides several of the memory timing signals. First, the row address hold time ($\overline{RAS}$ low to MA0-MA7 switching) is guaranteed to be a minimum of 30 ns ($t_{REL-MAX}$); this value satisfies the row address hold times (t_{RAH}) of TMS4164/TMS4416 (-15 and -20) DRAMs. Secondly, ALE low to $\overline{CAS}$ low ($t_{AEL-CEL}$) is within a guaranteed maximum. The rising edges of ALE and $\overline{ACX}$ have the same functions as described in the second example. In many applications, ALE and $\overline{ACX}$ can be tied together to take advantage of this "automatic timing feature" of the TMS4500A.

Figure 4 illustrates the case where $\overline{ACX}$ overlaps ALE. In this case, the falling edges of ALE and $\overline{ACX}$ have the same function as described in the third example: that is, ALE controlling $\overline{RAS}$, $\overline{CAS}$, and the switching of MA0-MA7. The rising edges of ALE and $\overline{ACX}$ have the same function as described in the first example: that is, ALE controlling $\overline{RAS}$ and the switching of MA0-MA7 while $\overline{ACX}$ controls $\overline{CAS}$.

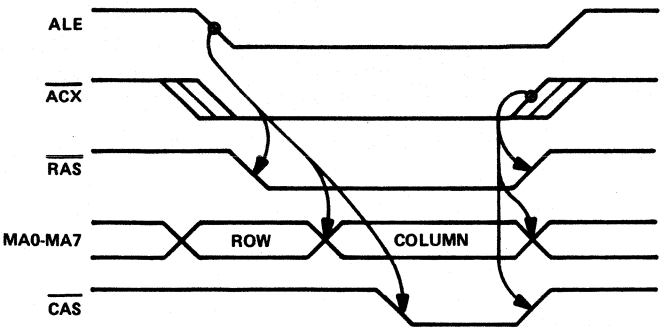


FIGURE 3 – $\overline{ACX}$ PRIOR TO OR COINCIDENT WITH ALE

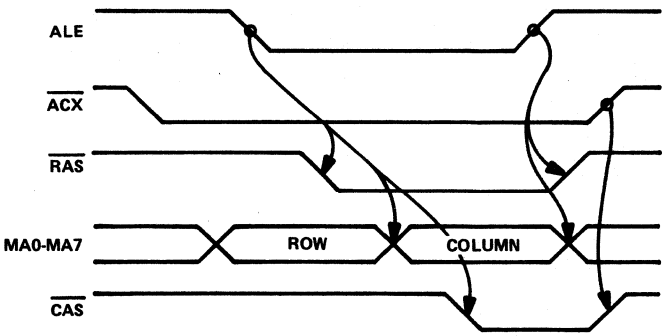


FIGURE 4 – $\overline{ACX}$ OVERLAPPING $\overline{ALE}$

Figures 1 and 4 show the case where ALE rises prior to $\overline{ACX}$; in this case the TMS4500A can be used to perform hidden refresh (see Figure 5). The hidden refresh feature currently implemented on several DRAMs allows refresh to be performed while data out of the DRAM is still valid. This is accomplished by holding $\overline{CAS}$ low, supplying a refresh address, then strobing $\overline{RAS}$. The timing sequence required to accomplish this with the TMS4500A is as follows. During a memory access if refresh request (REFREQ) goes low, a hidden refresh may be performed by holding ACX low and bringing ALE high. The TMS4500A does refresh arbitration on the falling edge of the clock (edge A); with $\overline{REFREQ}$ acknowledged and ALE high, a refresh will be granted. The refresh address will then be present at MA0-MA7 and $\overline{RAS}$ will go low $t_{CH\text{-}RRL}$ after the next rising edge of CLK (edge B). $\overline{RAS}$ will remain low for one or two clock cycles (one cycle for three-cycle refresh and two cycles for four-cycle refresh) and go high $t_{CH\text{-}RRH}$ after the rising edge of CLK (edge D). $\overline{ACX}$ going high brings $\overline{CAS}$ high as previously explained. When operating in this mode, it is necessary to pay particular attention to the timing of ALE high to CLK low in order to meet DRAM $\overline{RAS}$ precharge times.

The ALE high to CLK low time is given by:

$$t_{AEH\text{-}CL} = t_{RP} - t_{w(CL)} - t_{CH\text{-}RRL} + t_{AEH\text{-}REH} + t_{t(REH)}$$

where $t_{AEH\text{-}CL}$ = ALE high to CLK low

t_{RP} = memory precharge time (from DRAM spec.)

$t_{w(CL)}$ = CLK low time

$t_{CH\text{-}RRL}$ = CLK high to refresh $\overline{RAS}$ starting low*

$t_{AEH\text{-}REH}$ = ALE high to $\overline{RAS}$ starting high

$t_{t(REH)}$ = $\overline{RAS}$ rise time

*Multiply by a skew factor (0.9) because the maximum skew between starting high and starting low edges are required.

Given this equation, the timing of ALE can be obtained to meet the memory precharge times when operating the TMS4500A in this mode.

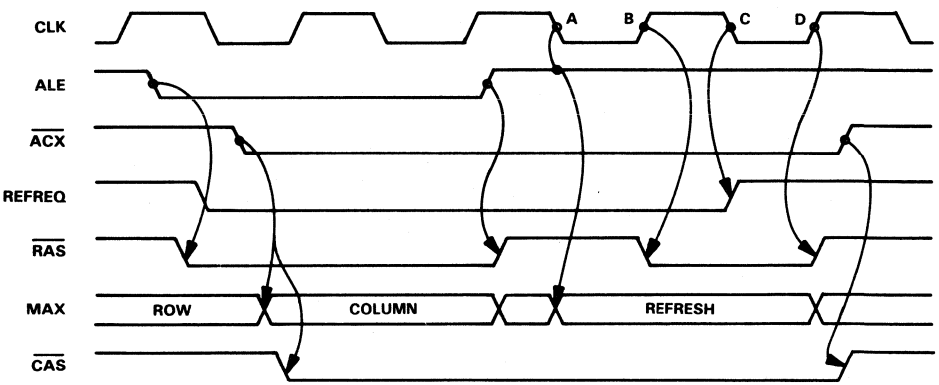
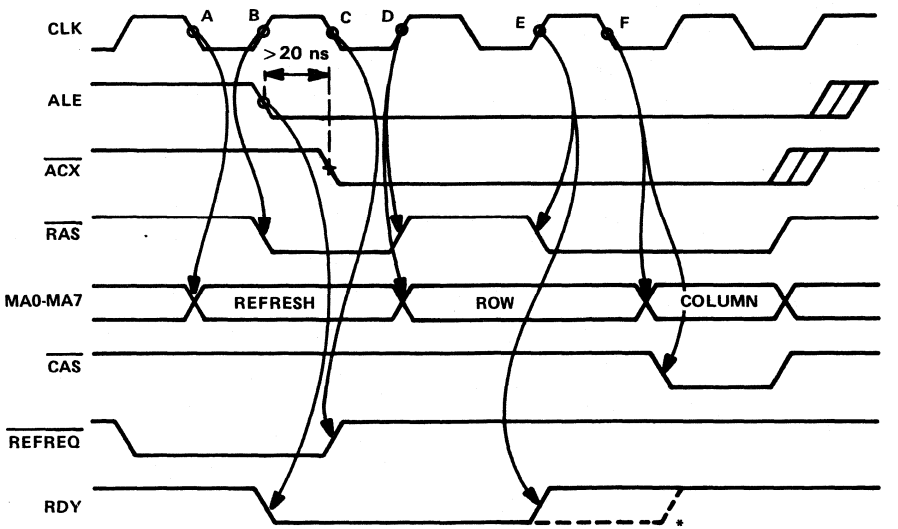


FIGURE 5 — REFRESH AFTER ACCESS (HIDDEN REFRESH)

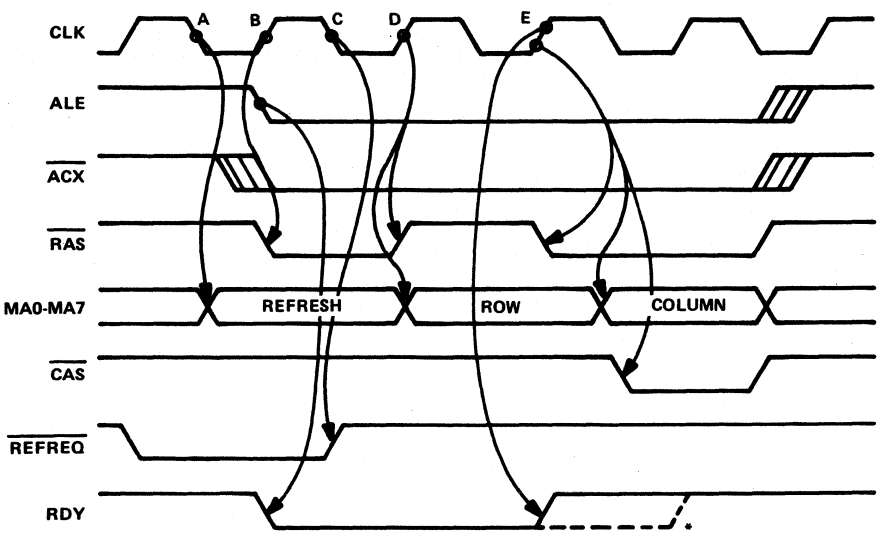
Figures 6 and 7 show how the edge timings of ALE and $\overline{ACX}$ described in the previous examples affect the $\overline{RAS}$ and $\overline{CAS}$ timings on access grant cycles. An access grant cycle occurs when ALE goes low during a refresh cycle. In this case the timing of ALE low to $\overline{ACX}$ low determines the timing of $\overline{RAS}$ and $\overline{CAS}$ low with respect to CLK. If $\overline{ACX}$ falls more than 20 ns after ALE during a refresh cycle, the TMS4500A will follow the timing shown in Figure 6. If $\overline{ACX}$ falls prior to or less than 2 ns after ALE during a refresh cycle, the TMS4500A will follow the timing shown in Figure 7. The difference between the two timing diagrams is the $\overline{CAS}$ timing with respect to CLK. On access grant cycles, the falling edge of ALE causes the RDY signal to go low; RDY low is generally used to hold off the processor until the refresh cycle is complete. The refresh timings of $\overline{RAS}$, $\overline{CAS}$, and MA0-MA7 are identical to the fifth example with respect to CLK edges A, B, C, and D. CLK edge E in Figures 6 and 7 terminates the refresh cycle and initiates the access grant cycle by bringing the RDY signal high and the $\overline{RAS}$ signal low.[1] In Figure 6 ($\overline{ACX}$ falling more than 20 ns after ALE), the $\overline{CAS}$ signal is timed from the subsequent falling edge of CLK after the access grant cycle is initiated (CLK F) and will go low $t_{CL\text{-}CEL}$ later. In Figure 7 ($\overline{ACX}$ falling prior to or less than 2 ns after ALE), the $\overline{CAS}$ signal is timed from the rising edge of CLK that initiated the access grant cycle (CLK E) and will go low $t_{CH\text{-}CEL}$ later. This diagram shows that $\overline{CAS}$ will fall approximately one-half CLK cycle earlier in Figure 7 than $\overline{CAS}$ in Figure 6; this timing arrangement decreases the access time after refresh. In both of these access grant examples, the cycle is terminated by the low-to-high transition of ALE and $\overline{ACX}$ as described above.



* Timing of RDY for TWST = 1 is shown by dashed lines.

FIGURE 6 — ACCESS GRANT (ALE LEADING OR OVERLAPPING $\overline{ACX}$)

[1] When operating with no wait states (TWST = 0), the timing is as described. When operating with wait states (TWST = 1), the RDY signal is extended low for one more CLK cycle as shown in the drawing by the dashed line.



* Timing of RDY for TWST = 1 is shown by dashed lines.

FIGURE 7 – ACCESS GRANT ($\overline{ACX}$ PRIOR TO, COINCIDENT, OR OVERLAPPING ALE)

The examples given have shown how the edge timings of ALE and $\overline{ACX}$ of the TMS4500A effect the $\overline{RAS}$, $\overline{CAS}$, and MA0-MA7 outputs. Table 1 provides a quick reference and summary showing which input controls which output(s) for the example timing diagrams given in Figures 1 through 4.

TABLE 1 – ALE AND $\overline{ACX}$ FUNCTIONS

TIMING DIAGRAM	SIGNAL TRANSITIONS						
	RAS↓	RAS↑	CAS↓	CAS↑	MA0-MA7 ROW TO COL.	MA0-MA7 COL. TO ROW	CAS↓ ACCESS GRANTS
	ACTUATING SIGNALS						
Figure 1 ALE Leading $\overline{ACX}$	ALE↓	ALE↑	$\overline{ACX}$↓	$\overline{ACX}$↑	$\overline{ACX}$↓	ALE↑	CLK↓ (Fig. 6)
Figure 2 ALE Overlapping $\overline{ACX}$	ALE↓	$\overline{ACX}$↑	$\overline{ACX}$↓	$\overline{ACX}$↑	$\overline{ACX}$↓	$\overline{ACX}$↑	CLK↓ (Fig. 6)
Figure 3 $\overline{ACX}$ Prior To Or Coincident With ALE	ALE↓	$\overline{ACX}$↑	ALE↓	$\overline{ACX}$↑	ALE↓	$\overline{ACX}$↑	CLK↑ (Fig. 7)
Figure 4 $\overline{ACX}$ Overlapping ALE	ALE↓	ALE↑	ALE↓	$\overline{ACX}$↑	ALE↓	ALE↑	CLK↑ (Fig. 7)

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Applications Brief

TMS4500A DRAM CONTROLLER CONFIGURED FOR THE TMS99000 SERIES 16-BIT MICROPROCESSORS

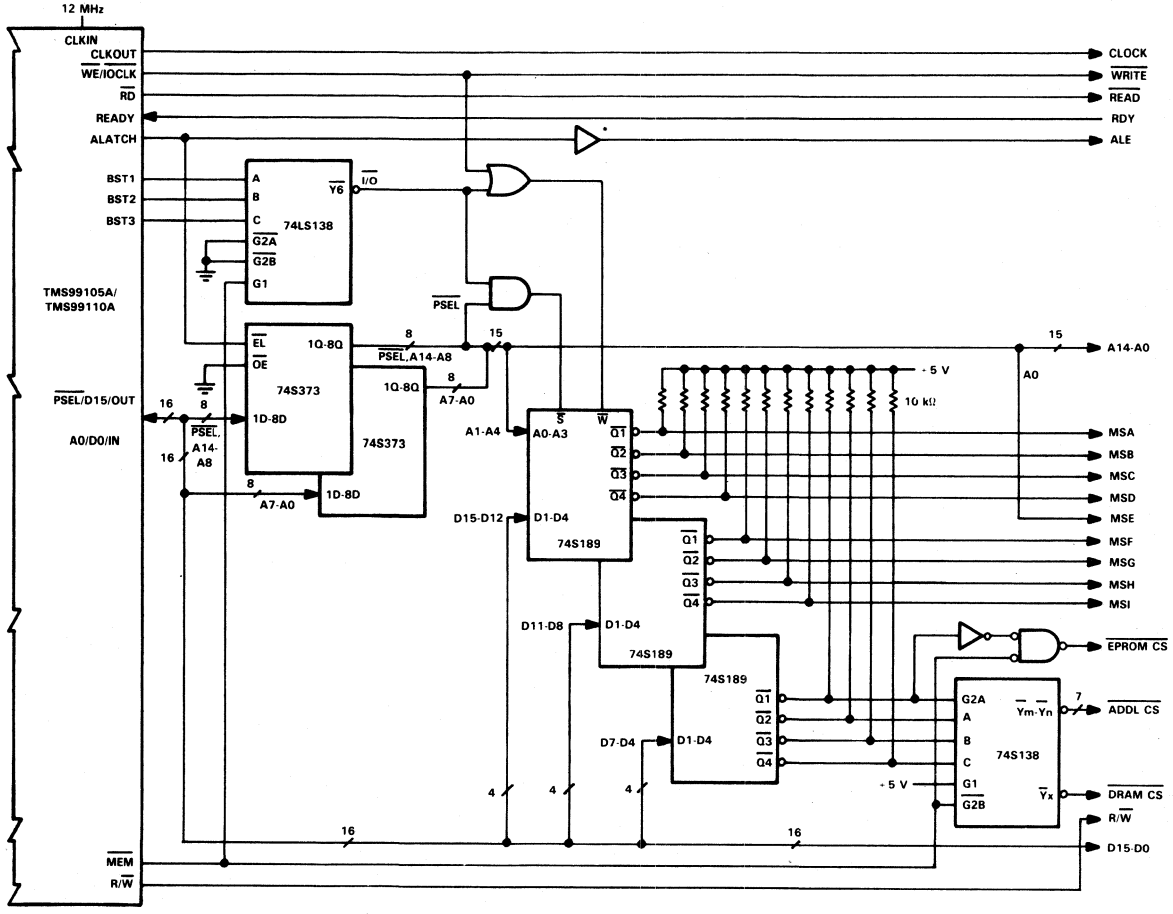
The TMS4500A dynamic RAM controller can be used in various configurations with TMS99000 series 16-bit microprocessors.[1] A medium-speed version and its timing diagram are shown in Figures 1 and 2, respectively. A high-speed version and its timing diagram are shown in Figures 3 and 4, respectively. Two memory configurations are also shown: a bulk memory configuration and a modular array. The bulk memory configuration uses 32 TMS4164 dynamic RAMs arranged as 128K of 16-bit words (see Figure 5). The modular memory array is comprised of 16 TMS4416 16K X 4 dynamic RAMs arranged as 64K of 16-bit words (see Figure 6). The modular array can be reduced in 16K word increments to a system that is 16K words deep for less memory-intensive applications. In addition, signals have also been provided to increase the memory depth to 128K words. In the paragraphs that follow, a description of both speed versions will precede a six-point analysis of the design criteria presented in the "TMS4500A Dynamic RAM Controller Users Manual." Both versions will be analyzed to ensure a proper match of timing signals between processor and memory.

The 15 address lines (A0-A14) and $\overline{\text{PSEL}}$ are latched by two 74S373 8-bit data latches as shown in Figure 1.[2] Latched addresses A1-A4 are used to address three 16 X 4 bipolar RAMs in order to generate eight higher-order memory address lines. These RAMs are used as a memory mapping function to increase the memory space of the TMS99000. Four of the higher order address lines are decoded into chip selects for all memory-mapped devices. On powerup and reset, the TMS99000 fetches the reset trap vector located at memory address 0000_H. Since $\overline{\text{PSEL}}$ is forced high for this fetch, the three memory-map RAMs are deselected, allowing their outputs to be pulled high by the 10k pullup resistors. This deselects the memory decoder and enables EPROM. Part of the reset service routine residing in EPROM should include instructions to load the memory mapper. The memory mapper is addressed using the I/O interface of the TMS99000 that has both serial and parallel bit manipulation capabilities.

Address lines A1-A4 are used to address the memory-map RAMs. A0 is set to a one for parallel I/O transfers (see TMS99000 Data Book). Additional I/O ports could be addressed by using the $\overline{\text{Y6}}$ output (I/O transfer) of the bus status decoder to enable an I/O decoder connected to the address latch outputs. Because of the large memory address space provided by the memory mapper, however, it was felt that all additional I/O ports could be memory-mapped.

1 All references to the TMS99000 apply to both the TMS99105A and TMS99110A microprocessors.

2 It should be noted that the TMS99000 uses the convention that A0 to A14 represent the most to least significant address bits, respectively.



* See Text

FIGURE 1 — TMS99105A/TMS99110A AND MEMORY MAPPING CIRCUITRY (3 MHz VERSION)

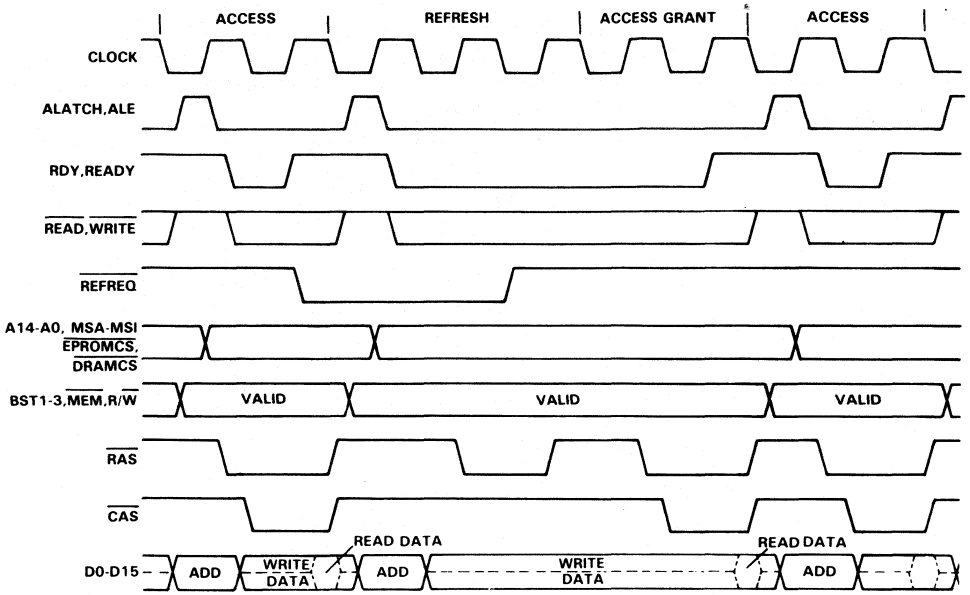


FIGURE 2 — TIMING DIAGRAM FOR TMS99105A OR TMS99110A AND TMS4500A INTERFACE (3 MHz VERSION)

In the high-speed version, the 74LS610 memory mapper has been added to replace the function of the 74S189 bipolar RAMs. Also, additional logic has been incorporated to allow the TMS99000 control signals to access dynamic memory at the higher speed. ALATCH is gated with a D-type flip-flop that allows ALE to fall after the falling edge of CLOCK following ALATCH going low. This allows the DRAMs to meet their specified $\overline{RAS}$ precharge time. A schottky flip-flop and a low-power schottky inverter are used to ensure that ALE falls at least 10 ns after CLOCK does. Since the TMS4500A will not generate READY in time for the TMS99000, this signal must be generated externally. This is done by detecting $\overline{SLOMEM}$ and using it to force READY low. $\overline{SLOMEM}$ is sampled by the TMS99000 READY input only when ALE is high so as to prevent placing the TMS99000 in an endless wait state. Once READY has initially gone low, it is kept low on DRAM memory cycles by RDY from the TMS4500A. It is finally returned high on the rising edge of CLOCK following RDY returning high. This will insert two wait states into each dynamic memory access cycle and one wait state for other slow memory (such as EPROM) cycles. If high speed static memory is used in the system, it should use $\overline{SLOMEM}$ = logic 1 status as a chip select.

Next, in order to use the TMS4500A as an interface between dynamic memory and any processor, the following specifications should be checked:

1. Refresh time
2. Memory precharge time
3. ALE to CLK relationship
4. Row address setup and hold times
5. Data valid to write enable time
6. Read access time.

First, the specifications for the medium-speed version will be checked to determine the memory speed, strap selection, and any logic modifications that might be necessary. For this example, assume that the TMS99000 has an input CLKIN frequency of 12 MHz (CLKOUT = 3 MHz).

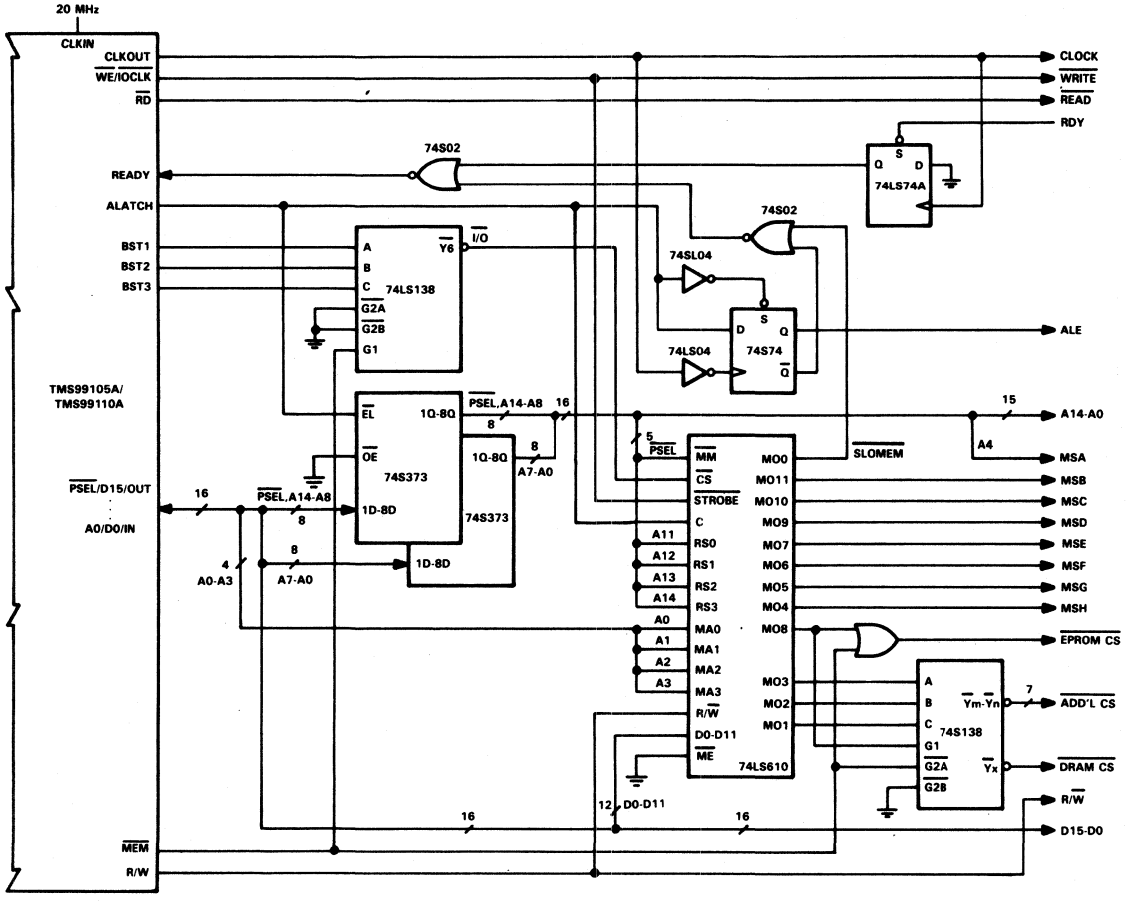


FIGURE 3 — TMS99105A/TMS99110A AND MEMORY MAPPING CIRCUITRY (5 MHz VERSION)

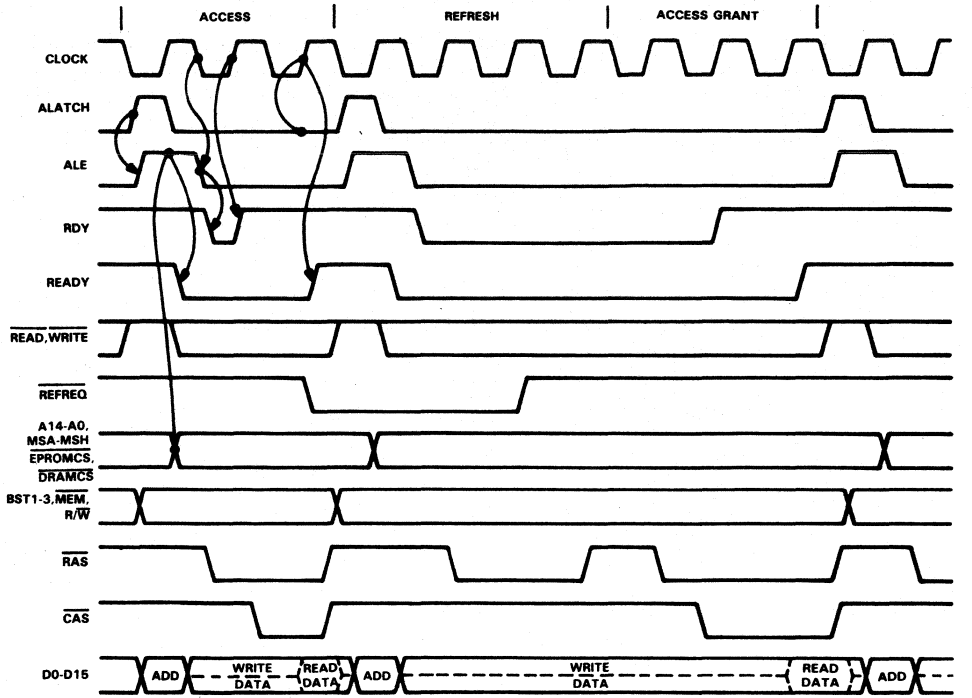


FIGURE 4 – TIMING DIAGRAM FOR TMS99105A OR TMS99110A AND TMS4500A INTERFACE (5 MHz VERSION)

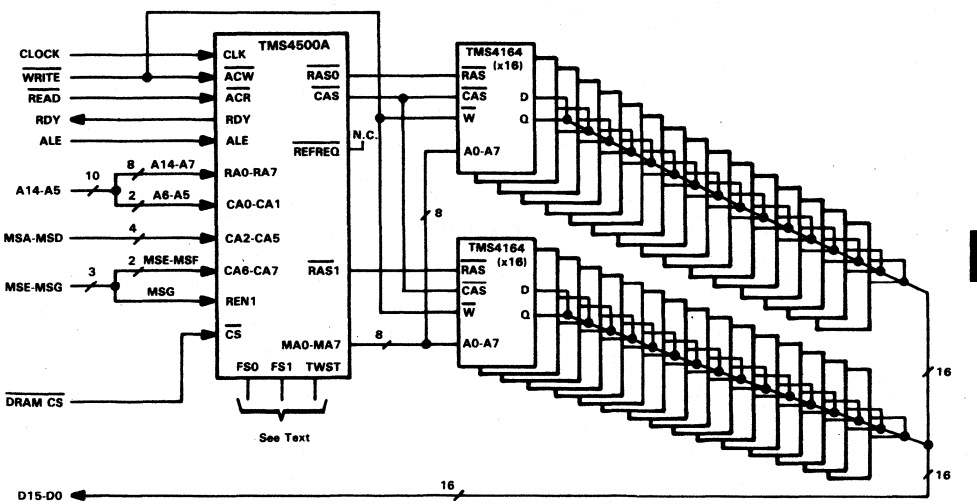
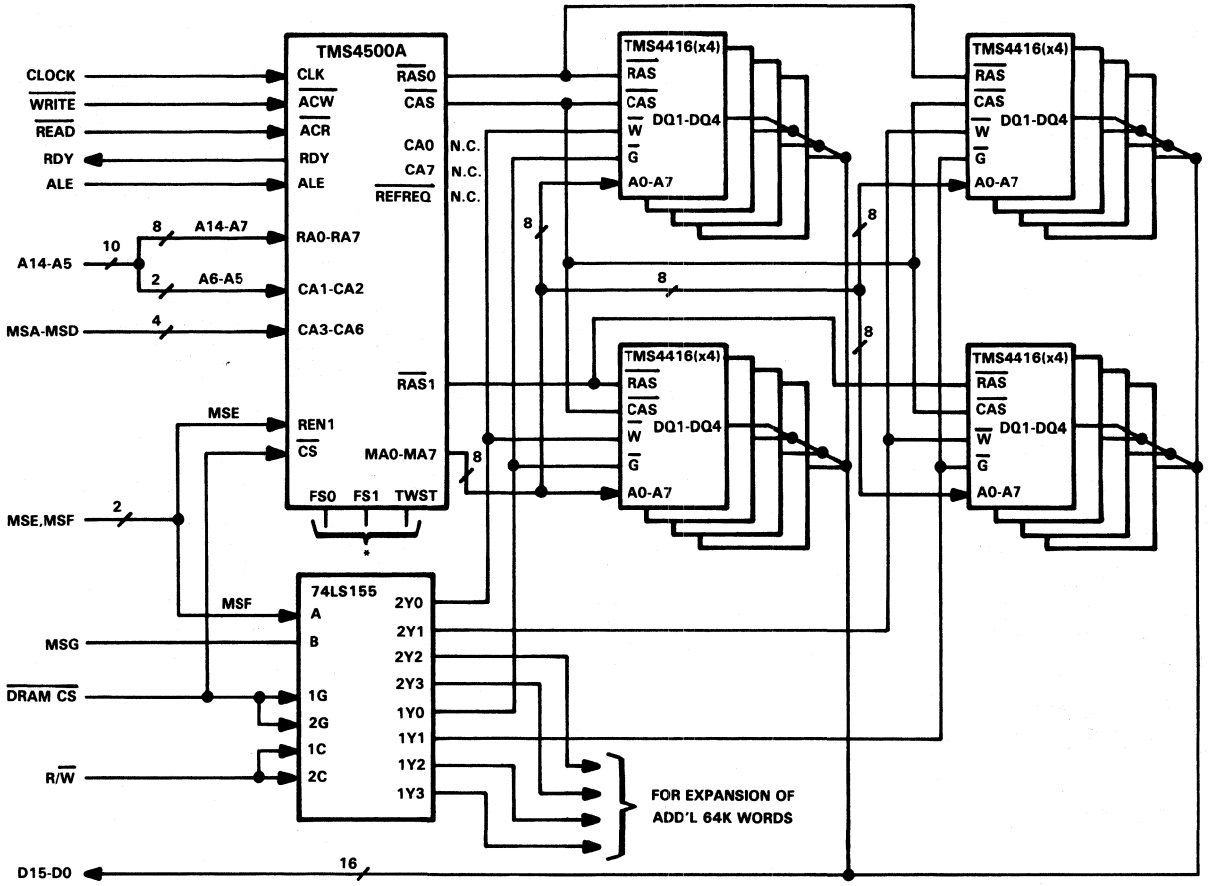


FIGURE 5 – TMS4500A AND 128K WORD DYNAMIC MEMORY USING TMS4164s



* See Table 1 for Strap Configuration.

FIGURE 6 — TMS4500A AND 64K WORD OF MODULAR DYNAMIC MEMORY USING TMS4416s

1. **Refresh Time**

TABLE 1 — STRAP CONFIGURATION

STRAP INPUT MODES			WAIT STATES FOR MEMORY ACCESS	REFRESH RATE	MINIMUM CLK FREQ. (MHz)	REFRESH FREQ. (kHz)	CLOCK CYCLES FOR EACH REFRESH
TWST	FS1	FS0					
L	L	L†	0	EXTERNAL	—	REFREQ	4
L	L	H	0	CLK ÷ 31	1,984	64 — 95†	3
L	H	L	0	CLK ÷ 46	2,944	64 — 85‡	3
L	H	H	0	CLK ÷ 61	3,904	64 — 82§	4
H	L	L	1	CLK ÷ 46	2,944	64 — 85‡	3
H	L	H	1	CLK ÷ 61	3,904	64 — 80‡	4
H	H	L	1	CLK ÷ 76	4,864	64 — 77‡	4
H	H	H	1	CLK ÷ 91	5,824	64 — 88+	4

† This strap configuration resets the Refresh Timer circuitry.
‡ Upper figure in refresh frequency is the frequency that is produced if the minimum CLK frequency of the next select state is used.
§ Refresh frequency if CLK frequency is 5 MHz.
+ Refresh frequency if CLK frequency is 8 MHz.

From Table 1 of the TMS4500A data sheet, there are two strap selections that would be appropriate for a 3 MHz clock frequency. One selection inserts a wait state on every memory access while the other does not. Assuming that no wait states will be necessary, select the strap input: FS0 = TWST = 0 and FS1 = 1. This will yield a refresh rate of (3 MHz)/46 or approximately 65 kHz. Each refresh will take 3 clock cycles.

2. **Memory Precharge Time ($\overline{RAS}$ precharge)**

The memory precharge time must be calculated for access, refresh, and access grant memory cycles to ensure the minimum $\overline{RAS}$ precharge time is satisfied.

a. Access Cycles

The precharge time on access cycles is given by:

$$t_{RP} = t_{c2}/4 + t_{d1} + t_{AEL\text{-}REL}^{*} - t_{d7} - t_{ACH\text{-}REH} - t_{t(REH)}$$

where
- t_{RP} = $\overline{RAS}$ precharge time
- t_{c2} = CLKOUT period
- t_{d1} = Delay from ALATCH low from reference line (MAX, 99000 Spec.)
- = $t_{c2}/4 + 10$
- $t_{AEL\text{-}REL}$ = Time delay, ALE low to $\overline{RAS}$ starting low (MAX, 4500A-20 Spec.*)
- t_{d7} = $\overline{WE}$, $\overline{RD}$ control release delay (MAX, 99000 Spec.)
- $t_{ACH\text{-}REH}$ = Time delay, ACX high to $\overline{RAS}$ starting high (MAX, 4500A-20 Spec.)
- $t_{t(REH)}$ = $\overline{RAS}$ rise time (MAX, 4500A-20 Spec.)

thus t_{RP} = (333/4 + 333/4 + 10 + 36 — 30 — 40 — 20) ns
= 123 ns $\overline{RAS}$ precharge time.

* This value should otherwise be a minimum value; however as all propagation delays on a given chip will tend to track each other, the maximum value is multiplied by a skew factor to reflect variations in same-chip propagation delays. The skew factor used here is 0.9. All values (followed by an asterisk) are obtained by multiplying the specified maximum value by 0.9.

b. Access Grant Cycles

The precharge time for access grant cycles is given by:

	t_{RP}	=	$t_{c2} + t_{CH\text{-}REL}^{*} - t_{CH\text{-}RRH} - t_{t(REH)}$
where	$t_{CH\text{-}REL}$	=	Time delay, CLK high to access $\overline{RAS}$ starting low (MAX, 4500A-20 Spec.*)
	$t_{CH\text{-}RRH}$	=	Time delay, CLK high to refresh $\overline{RAS}$ starting high (MAX, 4500A-20 Spec.)
thus	t_{RP}	=	(333 + 63 − 45 − 20) ns = 331 ns $\overline{RAS}$ precharge time

c. Refresh Cycles

The precharge time for refresh cycles is given by:

	t_{RP}	=	$1.5\ (t_{c2}) + t_{CH\text{-}RRL}^{*} - t_{d7} - t_{ACH\text{-}REH} - t_{t(REH)}$
where	$t_{CH\text{-}RRL}$	=	Time delay, CLK high to refresh $\overline{RAS}$ starting low (MAX, 4500A-20 Spec.*)
thus	t_{RP}	=	[1.5(333) + 54 − 30 − 40 − 20] ns = 464 ns $\overline{RAS}$ precharge time

3. ALE to CLK Relationship

ALE low transition must not occur within 10 ns of the CLK low transition. Since the TMS99000 strobes ALATCH low on the rising CLKOUT edge, this criterion is satisfied.

4. Row Address Setup and Hold Times

The row address, column address, REN1 and $\overline{CS}$ inputs must all be set up and stable no later than 10 ns prior to the falling edge of ALE. The latest of these signals will be $\overline{CS}$ which must propagate through all of the memory decode logic. The row address setup time for the 4500A then is given by:

	$t_{AV\text{-}AEL}$	=	$t_{d2}^{*} + t_{wH3} - t_{d3} - t_{p('S373)} - t_{p('S189)} - t_{p('S138)}$
where	$t_{AV\text{-}AEL}$	=	Setup time, row, column, REN1, $\overline{CS}$ valid to ALE starting low (MIN, 4500A-20 Spec.)
	t_{d2}	=	Delay to ALATCH high from reference line (MAX, 99000 Spec.*)
	t_{wH3}	=	ALATCH pulse width high (MIN, 99000 Spec.)
	t_{d3}	=	Delay to address valid from reference line (MAX, 99000 Spec.)
	$t_{p('S373)}$	=	Propagation delay, data input to output (MAX, 74S373 Spec.)
	$t_{p('S189)}$	=	Propagation delay, address input to output (MAX, 74S189 Spec.)
	$t_{p('S138)}$	=	Propagation delay, select input to output (MAX, 74S138 Spec.)
thus	$t_{AV\text{-}AEL}$	=	[13.5 + (333/4 − 15) − 15 − 13 − 35 − 12] ns
		=	6.8 ns setup time from $\overline{CS}$ to ALE starting low.

The setup time from row address valid (at the DRAMs) to $\overline{RAS}$ starting low must also be considered. This is given by:

	$t_{su(AR)}$	=	$t_{d1} + t_{AEL\text{-}REL}^{*} - t_{d3} - t_{p('S373)} - t_{p('S189)} - t_{RAV\text{-}MAV}$
where	$t_{su(AR)}$	=	Setup time, row address valid to $\overline{RAS}$ starting low
	t_{d1}	=	Delay to ALATCH low from reference line (MIN, 99000 Spec.)
	$t_{AEL\text{-}REL}$	=	Time delay, ALE low to $\overline{RAS}$ starting low (MAX, 4500A-20 Spec.*)
	t_{d3}	=	Delay to address valid from reference line (MAX, 99000 Spec.)

* Multiply the specified maximum value by 0.9.

	$t_{p('S373)}$	=	Propagation delay, data input to output (MAX, 74S373 Spec.)
	$t_{p('S189)}$	=	Propagation delay, address input to output (MAX, 74S189 Spec.)
	$t_{RAV-MAV}$	=	Time delay, row address valid to memory address valid (MAX, 4500A-20 Spec.)
thus	$t_{su(AR)}$	=	[(333/4 + 10) + 36 − 15 − 13 − 35 − 55] ns
		=	16 ns row address setup time for the DRAMs.

The row address hold time is guaranteed by the TMS4500A for −12, −15, and −20 speed range devices.

5. Data Valid to Write Enable

Since $\overline{CAS}$ is initiated by the write enable signal, all write cycles are necessarily early write cycles. Therefore, we will calculate the setup time for data valid to $\overline{CAS}$ starting low which is given by:

	$t_{su(D)}$	=	$t_{AEL-CEL} + t_{d9} - t_{d1} - t_{d8}$
where	$t_{su(D)}$	=	Setup time, write data valid to $\overline{CAS}$ starting low
	$t_{AEL-CEL}$	=	Time delay, ALE low to $\overline{CAS}$ starting low (MIN, 4500A-20 Spec.)
	t_{d9}	=	Delay to $\overline{WE}$ from reference line (MAX, 99000 Spec.*)
	t_{d1}	=	Delay to ALATCH low from reference line (MAX, 99000 Spec.)
	t_{d8}	=	Delay from ALATCH low to valid write data (MAX, 99000 Spec.)
thus	$t_{su(D)}$	=	[75 + (333/4 + 18) − (333/4 + 20) − 35] ns
		=	38 ns setup time from data valid to $\overline{CAS}$ starting low.

6. Read Access Time

The maximum access time allowable from $\overline{CAS}$ to data valid on memory read cycles is given by:

	$t_{a(C)}$	=	$t_{c2} - t_{c2}/4 - t_{d1} - t_{AEL-CEL} - t_{su2}$
where	$t_{a(C)}$	=	Access time from $\overline{CAS}$ to data valid
	t_{c2}	=	CLKOUT period
	$t_{c2}/4$	=	Delay from CLKOUT falling to reference line (99000 Spec.)
	t_{d1}	=	Delay from reference line to ALATCH low (MAX, 99000 Spec.)
	$t_{AEL-CEL}$	=	Time delay, ALE low to $\overline{CAS}$ starting low (MAX, 4500A-20 Spec.)
	$t_{t(CEL)}$	=	$\overline{CAS}$ fall time (MAX, 4500A-20 Spec.)
	t_{su2}	=	Data setup time (to CLKOUT falling) (MIN, 99000 Spec.)
thus	$t_{a(C)}$	=	[333 − 333/4 − (333/4 + 20) + 20) − 200 − 25 − 25] ns
		=	−103 ns

Now that the six specifications on the design criteria checklist have been examined, the values obtained can be compared to those required for the TMS4164. This comparison shows that three criteria constrain design and memory selection. These criteria are $\overline{RAS}$ precharge, $\overline{CS}$ valid to ALE starting low, and read access from $\overline{CAS}$. The $\overline{RAS}$ precharge time of 123 ns means that only −20, −15, or −12 speed range devices may be used. Next, 3.2 ns of delay must be added to the ALE signal to ensure that $\overline{CS}$ is valid 10 ns before ALE starts low. This delay is achieved by inserting a buffer between ALATCH and ALE. Finally, a negative access time from $\overline{CAS}$ requires that a wait state must be inserted on each memory access cycle. By adding one CLKOUT period (set TWST = 1, FS0 = FS1 = 0) to the calculated memory access requirement, the read access cycle time (from $\overline{CAS}$) with one wait state inserted is given by:

* Multiply the specified maximum value by 0.9.

$t_{a(C)}$ = $(-103 + t_{c2} - t_{p(BFR)})$ ns

where $t_{p(BFR)}$ = Buffer propagation delay, input to output of the ALE buffer. (MAX, Spec.)

Using the worst case $\overline{CAS}$ access time for TMS4164-15 DRAMs ($t_{a(c)}$ = 100 ns), the maximum allowable propagation delay for the buffer can be determined:

$t_{p(BFR)}$ = $(-103 + t_{c2} + t_{a(c)})$ ns
= $(-103 + 333 - 100)$ ns
= 130 ns

This value must be greater than the maximum propagation delay for the ALE buffer.

The specifications for the high-speed version will be evaluated next. In this version, ALE is extended to meet the $\overline{RAS}$ precharge requirement for −15 devices. This also gives sufficient address setup time to use the 74LS610 memory mapper. The memory mapper performs essentially the same function as the bipolar RAM array in the previous example, but incorporates the control signals that are necessary on-chip. For more information regarding the 74LS610, refer to TI Application Brief entitled "Memory Mapping Using the SN54/74LS610 Thru SN54/74LS613 Memory Mapper." For the following example, assume that the TMS99000 has an input CLKIN frequency of 20 MHz (CLKOUT = 5 MHz).

1. Refresh Time

From Table 1 of the TMS4500A data sheet, the strap selection should be FS0 = 0, FS1 = TWST = 1. This will yield a refresh rate of 66 MHz and each refresh cycle will take 4 clock cycles. Also, the TMS4500A will insert one wait state on each access cycle. As was mentioned earlier, the external logic will insert two wait states on each access cycle with the assistance of the RDY signal from the TMS4500A.

2. Memory Precharge Time ($\overline{RAS}$ precharge)

a. Access Cycles
The precharge time on access cycles is given by:

t_{RP} = $t_{c2} + t_{p('LS04)} + t_{p('S74)} + t_{AEL-REL}^{*} - t_{d7} - t_{ACH-REH} - t_{t(REH)}$

where t_{c2} = 200 ns

$t_{p('LS04)}$ = Propagation delay, input to output (MIN, 74LS04 Spec.)

$t_{p('S74)}$ = Propagation delay, clock to Q output (MIN, 74S74 Spec.)

thus t_{RP} = (200 + 6 + 4 + 36 − 30 − 40 − 20)ns
= 156 ns $\overline{RAS}$ precharge time.

b. Access Grant Cycles

t_{RP} = $t_{c2} = t_{CH-REL}^{*} - t_{CH-RRH} - t_{t(REH)}$

thus t_{RP} = (200 + 63 − 45 − 20) ns
= 198 ns $\overline{RAS}$ precharge time.

c. Refresh Cycles

t_{RP} = $1.5[t_{c2}] + t_{CH-RRL}^{*} - t_{d7} - t_{ACH-REH} - t_{t(REH)}$

thus t_{RP} = [1.5(200) + 54 − 30 − 40 − 20] ns
= 264 ns $\overline{RAS}$ precharge time.

3. ALE to CLK Relationship

As mentioned previously, a schottky flip-flop and low-power schottky inverter are used to clock ALE so that a minimum of 10 ns delay is guaranteed from CLK low to ALE low.

* Multiply the specified maximum value by 0.9.

4. Row Address Setup and Hold Times

$t_{AV\text{-}AEL} = t_{c2} + t_{p('LS04)} + t_{p('S74)} - t_{c2}/4 - t_{d3} - t_{AVQV1}$

thus $t_{AV\text{-}AEL} = (200 + 6 + 4 - 50 - 15 - 70)$ ns
$=$ 75 ns setup time from $\overline{CS}$ to ALE starting low.

Also, $t_{su(AR)} = t_{c2} + t_{p('LS04)} + t_{p('S74)} + t_{AEL\text{-}REL}{}^{*} - t_{c2}/4 - t_{d3} - t_{AVQV1} - t_{RAV\text{-}MAV}$

thus $t_{su(AR)} = (200 + 6 + 4 + 36 - 50 - 15 - 70 - 50)$ ns
$=$ 61 ns row address setup time for the DRAMs.

5. Data Valid to Write Enable

Since data is valid before ALE falls, the data setup time is guaranteed.

6. Read Access Time

Assuming two wait states are generated for each access cycle:

$t_{a(C)} = 2[t_{c2}] - t_{p('LS04)}\dagger - t_{p('S74)}\dagger - t_{AEL\text{-}CEL} - t_{t(CEL)} - t_{su2}$

† Maximum values are used for propagation delays $t_{p('LS04)}$ and $t_{p('S74)}$ to satisfy worst-case design requirements.

thus $t_{a(C)} = [2(200) - 15 - 9 - 200 - 20 - 25]$ ns
$=$ 131 ns read access time from $\overline{CAS}$.

The previous calculations indicate that $\overline{RAS}$ precharge and read access requirements will constrain memory selection. TMS4164-25 devices will not be able to meet either the $\overline{RAS}$ precharge time ($t_{w(RH)}$ = 150 ns) or the read access time ($t_{a(C)}$ = 165 ns). TMS4164-20 devices cannot meet the read access time ($t_{a(C)}$ = 135 ns); however, TMS4164-15 devices meet all timing requirements.

Now that the 128K word memory using TMS4164s has been analyzed, a brief description of a 64K word memory using TMS4416s will be given. The major difference between the two memory configurations lies in the addition of a 74LS155 used as a one-of-four selector (see Figure 6). The R/$\overline{W}$ line from the TMS99000 is used to select whether the upcoming access is to be a read or write cycle. MSF selects either the left or right bank of memory while MSE selects either the upper or lower bank. Thus, only one of the four banks of 16K word memories will be accessed on any given memory cycle. Because all of the inputs to the 74LS155 are set up before the start of each DRAM access (ALE starting low), there are no timing constraints when using TMS4416-20 or TMS4416-15 devices.

Two memory system configurations have been presented showing how the TMS4500A can be configured to work with the TMS99000 16-bit microprocessor. A memory mapping scheme has been provided that is flexible enough to work with many microcomputer applications using the TMS99000 without modification. Although both expandability and modularity have been considered in this design, other memory mapping schemes and processor speeds are possible.

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Multiply the specified maximum value by 0.9.

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Applications Brief

TMS4500A/8088 INTERFACE

This application brief presents a circuit configuration which interfaces the 8088 microprocessor to dynamic RAM memory via the TMS4500A-15 dynamic RAM controller. The memory array is 32K bytes deep and features the TMS4416 16K X 4 dynamic RAM. The TMS4416 was used for its modularity advantage over X1 DRAMs.

Figure 1 shows the schematic diagram of the circuit while Figure 2 depicts the timing diagram of a write access followed by a refresh followed by a read access grant memory cycle. The 8088 and TMS4500A both operate at 5 MHz requiring no wait states on normal memory accesses. The TMS4500A clock is shifted by one 15 MHz clock cycle via a 74S74 to ensure the proper ALE low to CLK low relationship to the TMS4500A. In order to cover the important TMS4500A interface requirements, the six-point design criteria will be used as presented in the "TMS4500A Dynamic RAM Controller Users Manual."

1. Refresh Time

The TMS4500A is configured for maximum division of the clock without inserting wait states by strapping TWST, FS1, and FS0 as follows: TWST = 0, FS1 = 1 and FS0 = 1.

This strap configuration divides the clock by 61 to yield a refresh rate of 3.123 ms (see TMS4500A Spec.).

2. Memory Precharge time

The memory precharge time must be calculated for consecutive access, refresh, and access grant cycles to ensure that the minimum $\overline{RAS}$ precharge time is satisfied.

a. Access Cycles

The precharge time for access cycles is given by:

$$t_{RP} = TCLCL + TCLCH - TCLRH - t_{ACH\text{-}REH} - t_{t(REH)} + TCHLL + t_{AEL\text{-}REL}^{*}$$

where

t_{RP}	=	$\overline{RAS}$ precharge time
TCLCL	=	CLK cycle period
TCLCH	=	CLK low time (2/3 TCLCL − 15, 8284A Spec.)
TCLRH	=	$\overline{RD}$ inactive delay (MAX 8088 Spec.)
$t_{AEH\text{-}REH}$	=	Time delay, ALE high to $\overline{RAS}$ starting high (MAX TMS4500A-15 Spec.)

	$t_{t(REH)}$	=	$\overline{RAS}$ rise time (MAX TMS4500A-15 Spec.)
	TCHLL	=	ALE inactive delay (MAX 8088 Spec.)
	$t_{AEL-REL}$	=	Time delay, ALE low to $\overline{RAS}$ starting low (MAX TMS4500A-15 Spec.*)
thus,	t_{RP}	=	(200 + 118 − 150 − 30 − 15 + 85 + 27) ns
		=	235 ns

*This value should otherwise be a minimum value; however, as all propagation delays on a given chip will tend to track each other, the maximum value is multiplied by a skew factor to reflect variations in same chip propagation delays. The skew factor for the TMS4500A is 0.9. All values follow by an asterisk are obtained by multiplying the specified maximum value by 0.9.

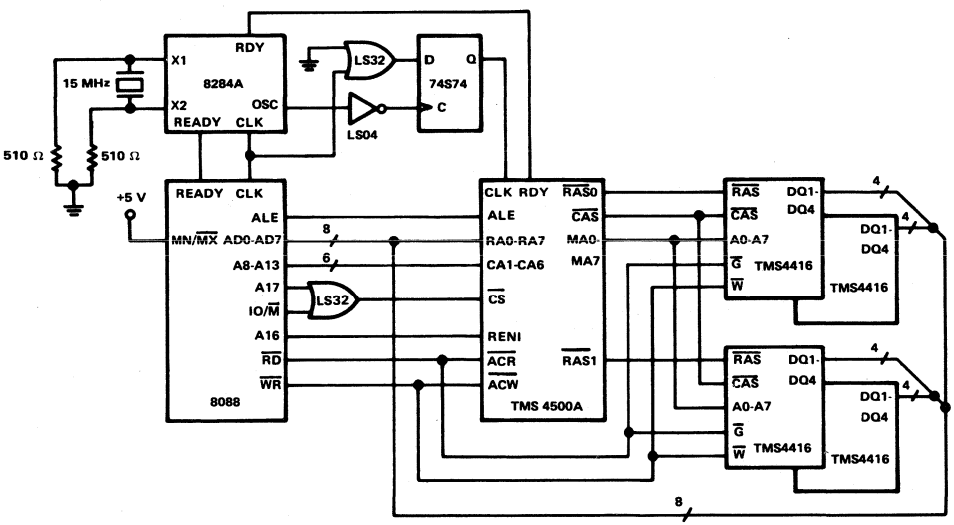

FIGURE 1 – TMS4500A/8088 INTERFACE SCHEMATIC

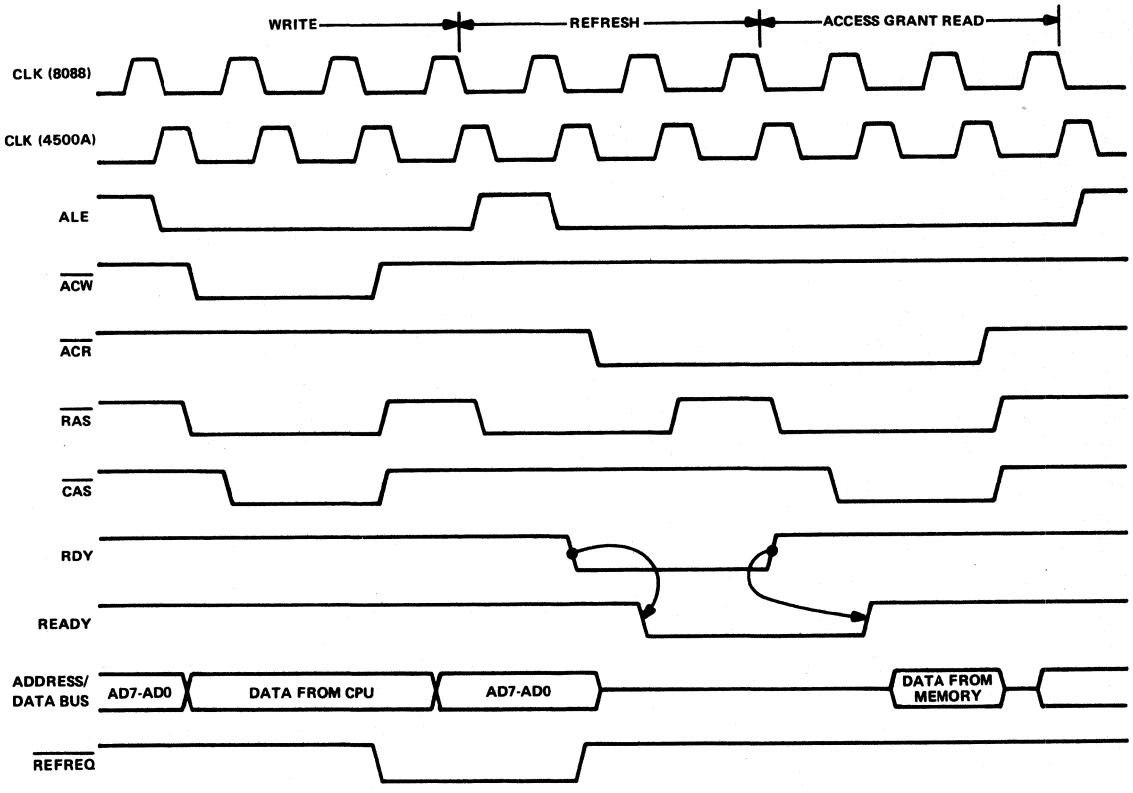

FIGURE 2 – TIMING DIAGRAM

b. Refresh Cycles

On refresh cycles the minimum precharge time occurs when $\overline{ACR}$ or $\overline{ACW}$ go high 20 ns before TMS4500A CLK low. If this occurs, refresh $\overline{RAS}$ will go low on the subsequent rising edge of the TMS4500A CLK.

The minimum precharge time for refresh cycles is given by:

	t_{RP}	=	$TCLCH + t_{ACH\text{-}CL} - t_{ACH\text{-}REH} - t_{t(REH)} + t_{CH\text{-}RRL}$*
where	$t_{ACH\text{-}CL}$	=	Time delay $\overline{ACX}$ high to CLK low (MIN TMS4500A-15 Spec.)
	$t_{ACH\text{-}REH}$	=	Time delay, $\overline{ACX}$ to $\overline{RAS}$ starting high (MAX TMS4500A-15 Spec.)
	$t_{CH\text{-}RRL}$	=	Time delay, CLK high till refresh $\overline{RAS}$ starting low (MAX TMS4500A-15 Spec.*)
thus,	t_{RP}	=	(118 + 20 − 30 − 15 + 45) ns
		=	138 ns

c. Access Grant Cycles

The precharge time for access grant cycles is given by:

	t_{RP}	=	$TCLCL - t_{CH\text{-}RRH} - t_{t(REH)} + t_{CH\text{-}REL}$*
where	$t_{CH\text{-}RRH}$	=	Time delay, CLK high to refresh $\overline{RAS}$ starting high (MAX TMS4500A-15 Spec.)
	$t_{CH\text{-}REL}$	=	Time delay, CLK high to access $\overline{RAS}$ starting low (MAX TMS4500A-15 Spec.*)
thus,	t_{RP}	=	(200 − 35 − 15 + 54) ns
		=	204 ns

3. ALE to CLK Relationship

The ALE low transition must not occur within 10 ns of the TMS4500A CLK low transition. This is guaranteed by the phase shift between the 8088 and TMS4500A clocks.

ALE low to CLK low time is given by:

	$t_{AEL\text{-}CL}$	=	$2(t_{OSC}) - t_{OLCH} - TCHLL + t_{p04} + t_{p74}$
where	t_{OSC}	=	OSC cycle period (8284A Spec.)
	t_{OLCH}	=	OSC low to CLK high (MAX 8284A Spec.)
	t_{p04}	=	Propagation delay, MSI gate (MIN 74LS04 Spec.)
	t_{p74}	=	Propagation delay, MSI gate (MIN 74S74 Spec.)
thus	$t_{AEL\text{-}CL}$	=	[2(66) − 22 − 85 + 5 + 4] ns
		=	34 ns

4. Row Address Setup and Hold Time

The setup time to the TMS4500A is given by:

	$t_{AV\text{-}AEL}$	=	$TAVAL - t_{p32}$
where	$t_{AV\text{-}AEL}$	=	Time delay, address, REN1, $\overline{CS}$ valid to ALE low (MIN TMS4500A-15 Spec.)

	TAVAL	=	Address valid to ALE low (TCLCH − 60, MIN 8088 Spec.)
	t_{p32}	=	Propagation delay, SSI gate, allowing for delay to $\overline{CS}$ (MAX 74LS32 Spec.)
thus,	t_{AV-AEL}	=	(118 − 60 − 22)ns
		=	36 ns

The row address setup time to the DRAMs is given by:

	t_{ASR}	=	TAVAL − $t_{RAV-MAV}$ + $t_{AEL-REL}$*
where	$t_{RAV-MAV}$	=	Time delay, row address valid to memory address valid (MAX TMS4500A-15 Spec.)
thus,	t_{ASR}	=	(118 − 60 − 40 + 27) ns
		=	45 ns

5. Data Valid to Write Enable

All writes to memory are early writes, which allows data to be set up to $\overline{CAS}$ instead of $\overline{W}$. The 8088 specifies that the data is valid a minimum of 0 ns to $\overline{WR}$ low. This gives a data setup time equal to $t_{ACL-CEL}$ (50 ns MIN) for this circuit.

6. Read Access time from $\overline{CAS}$

The required access time for both access and access grant memory cycles must be calculated.

The read access time from $\overline{CAS}$ on normal access cycles is given by:

	t_{CAC}	=	2(TCLCL) − TCLRL − $t_{ACL-CEL}$ − $t_{t(CEL)}$ − TDVCL
where	t_{CAC}	=	Access time from $\overline{CAS}$
	TCLRL	=	$\overline{RD}$ active delay (MAX 8088 Spec.)
	$t_{ACL-CEL}$	=	Time delay, $\overline{ACX}$ low to $\overline{CAS}$ starting low (MAX TMS4500A-15 Spec.)
	$t_{t(CEL)}$	=	$\overline{CAS}$ fall time (MAX TMS4500A-15 Spec.)
	TDVCL	=	Data valid delay (MIN 8088 Spec.)
thus	t_{CAC}	=	[2(200) − 165 − 90 − 15 − 30] ns
		=	100 ns

The read access time on access grant cycles is given by:

	t_{CAC}	=	2(TCLCL) + TCHCL − t_{CH-CEL} − $t_{t(CEL)}$ − TDVCL
where	TCHCL	=	CLK high time (1/3 TCLCL + 2, MIN 8284A Spec.)
	t_{CH-CEL}	=	Time delay, CLK high to access $\overline{CAS}$ starting low (MAX TMS4500A-15 Spec.)
thus,	t_{CAC}	=	[2(200) + 68 − 140 − 15 − 30] ns
		=	283 ns

The calculations of the design criteria for the TMS4500A interface have been completed. An inspection of the design criteria reveals that t_{CAC} on normal accesses constrains the choice of memories to TMS4416-15 (t_{CAC} = 80 ns). Slower memories can be used by decreasing the 8088 clock speed. For TMS4416-20 devices, the maximum CLK frequency as constrained by $\overline{CAS}$ access time is given by:

$$f_{CLK} = [1/2\ (t_{CAC} + T_{CLRL} + t_{ACL\text{-}CEL} + t_{t(CEL)} + TDVCL)]^{-1} \times 10^9$$

where f_{CLK} = Maximum 8088 clock frequency

t_{CAC} = $\overline{CAS}$ access time (MIN TMS4416-20 Spec.)

thus, $f_{CLK} = [1/2\ (120 + 165 + 90 + 15 + 30)]$ ns

$= 4.762$ MHz

A circuit configuration to interface dynamic memories to the 8088 microprocessor utilizing the TMS4500A dynamic RAM controller has been presented. The circuit design featured a 5 MHz 8088 interfaced to a TMS4500A-15 operating with no wait states. The memory array was implemented with TMS4416 dynamic RAMs for increased modularity.

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Applications Brief

TMS4500A/MC68000 INTERFACE

This application note provides several circuit configurations interfacing three speed ranges of the MC68000 microprocessor to dynamic RAM memory via the TMS4500A-15 dynamic RAM controller. The MC68000L6 operates with no wait states while the MC68000L8 and MC68000L10 operate with one wait on normal memory access cycles. The memory array is organized as 32K words featuring the TMS4416 16K × 4 dynamic RAM arranged as two rows of 16K × 16 bits with each row partitioned into 16K bytes of upper and 16K bytes lower memory. The TMS4416 was used for its modularity advantage over X1 DRAMs and upgradability to future 64K × 4 devices.

Two approaches for controlling access to the upper and lower bytes of memory are given. The first approach (Figure 1A) controls access to upper and lower memory by gating $\overline{CAS}$ with $\overline{UDS}$ and $\overline{LDS}$ providing an early write condition. Early write occurs when the $\overline{W}$ signal to the DRAM goes low prior to $\overline{CAS}$ low. Under this condition the data input to the DRAM is required to be set up prior to $\overline{CAS}$ instead of prior to $\overline{W}$, and the output buffers are disabled allowing the use of common I/O. This can be achieved on the TMS4164 by tying D and Q together; the TMS4416 is a common I/O device. The second approach (Figure 2A) controls access to upper and lower memory by gating R/$\overline{W}$ with $\overline{UDS}$ and $\overline{LDS}$ providing a late write condition ($\overline{CAS}$ low prior to $\overline{W}$ low). There are definite advantages and disadvantages to each of the implementations. From a system standpoint the gated $\overline{CAS}$ requires a smaller number of gates than the gated R/$\overline{W}$ version but would degrade $\overline{CAS}$ access time with the extra SSI gate (74LS32) delay. Another system criteria would be the choice of memory used with each implementation. For the gated $\overline{CAS}$ approach both TMS4416s and TMS4164s could be used with common I/O reducing layout signal routing complexity. The gated R/$\overline{W}$ implementation restricts the use of common I/O when using TMS4164s due to late write operation. In the late write cycle the Q outputs will go to an active state causing contention between the processor and the memory for the data bus. To use TMS4164s within the gated R/$\overline{W}$ system requires that the Q outputs be externally buffered to allow a bidirectional data bus which adds extra circuitry for the buffers. The timing diagrams for Figures 1A and 2A are given in Figure 1B and 2B, respectively.

Both methods of upper and lower byte control allow the use of read-modify-write (TAS instruction) cycles but the operational response of the DRAMs is slightly different. A read-modify-write is performed by first reading the data from a memory location then writing data back to that location in the same memory cycle. The TAS instruction (Test and Set an Operand) tests a byte operand and sets the negative and zero flags accordingly; the high order bit of the operand is set. This provides a means of synchronization in multiple processor environments. Figure 3 shows the read-modify-write timings for the gated $\overline{CAS}$ and gated R/$\overline{W}$ implementations. The two methods for controlling memory access have the advantages and disadvantages mentioned above plus another difference on read-modify-write cycles. The gated $\overline{CAS}$ approach actually does a page mode read then a page mode write (two $\overline{CAS}$ cycles for a single $\overline{RAS}$ cycle) to the same memory location while the gated

R/$\overline{W}$ approach does a normal read-modify-write to the DRAM. The choice of these methods would probably be determined by other factors in the system design; particularly the size of the memory array since the TMS4416 example would require less logic to implement but lends itself better to smaller memory designs.

The $\overline{DTACK}$ signal is derived by ANDing $\overline{UDS}$, $\overline{LDS}$, and R/$\overline{W}$ together, clocking RDY with a flip-flop and then ORing the two results. On normal accesses the RDY signal is high allowing either the $\overline{UDS}$, $\overline{LDS}$, or R/$\overline{W}$ signal to force $\overline{DTACK}$ low. On access grant cycles the low RDY signal holds $\overline{DTACK}$ high one clock period after the refresh cycle is complete. $\overline{UDS}$, $\overline{LDS}$ and R/$\overline{W}$ are ANDed together so that on read cycles $\overline{UDS}$ and/or $\overline{LDS}$ force $\overline{DTACK}$ low and on write cycles R/$\overline{W}$ forces $\overline{DTACK}$ low. This gating is necessary because $\overline{UDS}$ and $\overline{LDS}$ go low too late in the write cycle to provide sufficient $\overline{DTACK}$ setup time. It also provides the two $\overline{DTACK}$ pulses for read-modify-write cycles. For the MC68000L8/L10 design $\overline{DTACK}$ is delayed with a flip-flop to provide one wait state.

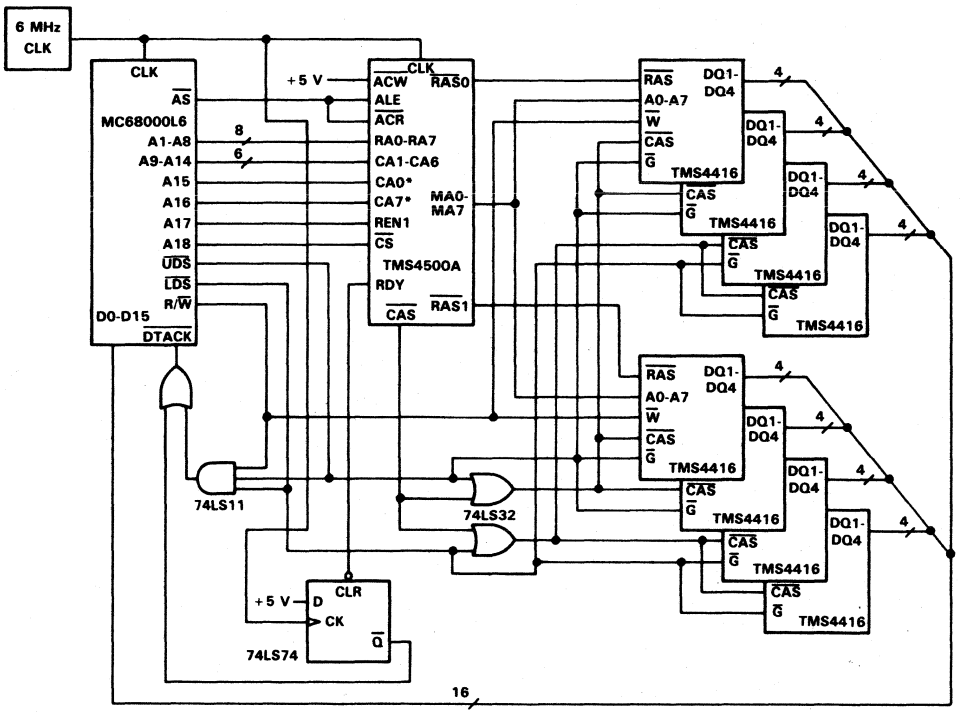


FIGURE 1A – TMS4500A/MC68000L6 INTERFACE SCHEMATIC (GATED $\overline{CAS}$)

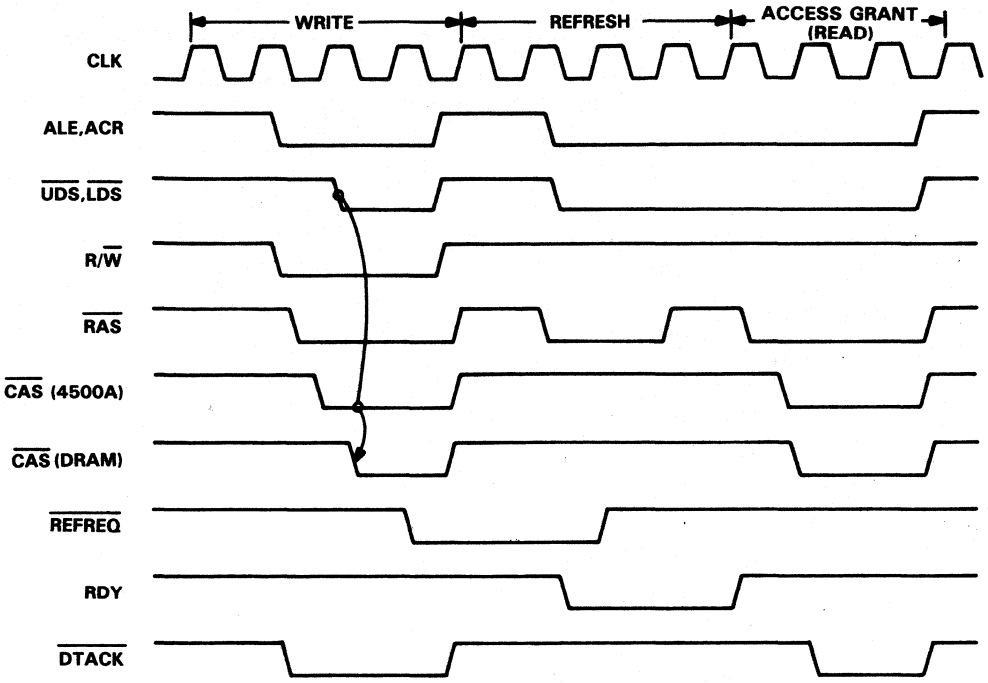
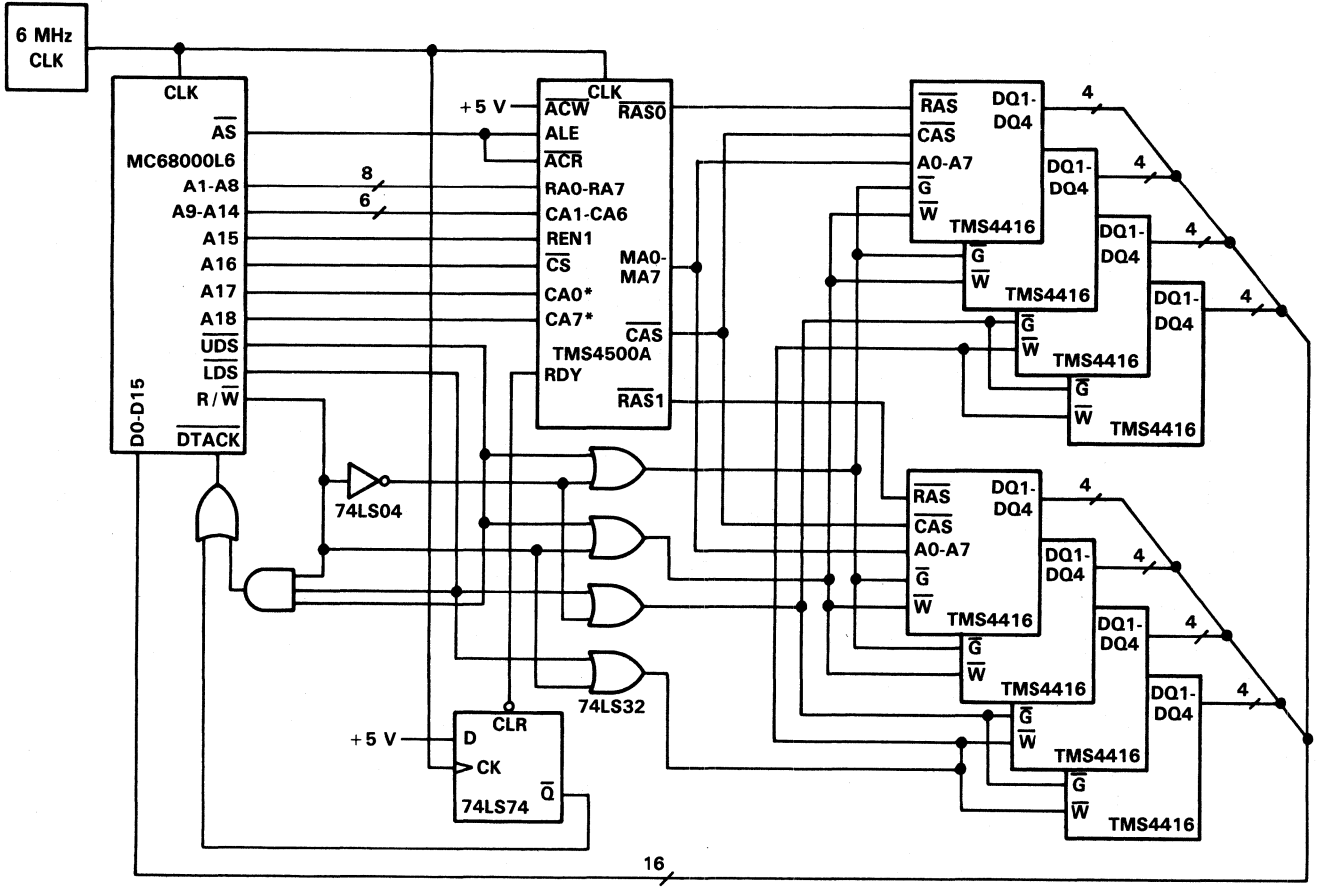


FIGURE 1B – TIMING DIAGRAM (GATED CAS)



*See text.

FIGURE 2A — TMS4500A/MC68000L6 INTERFACE SCHEMATIC (GATED R/$\overline{W}$)

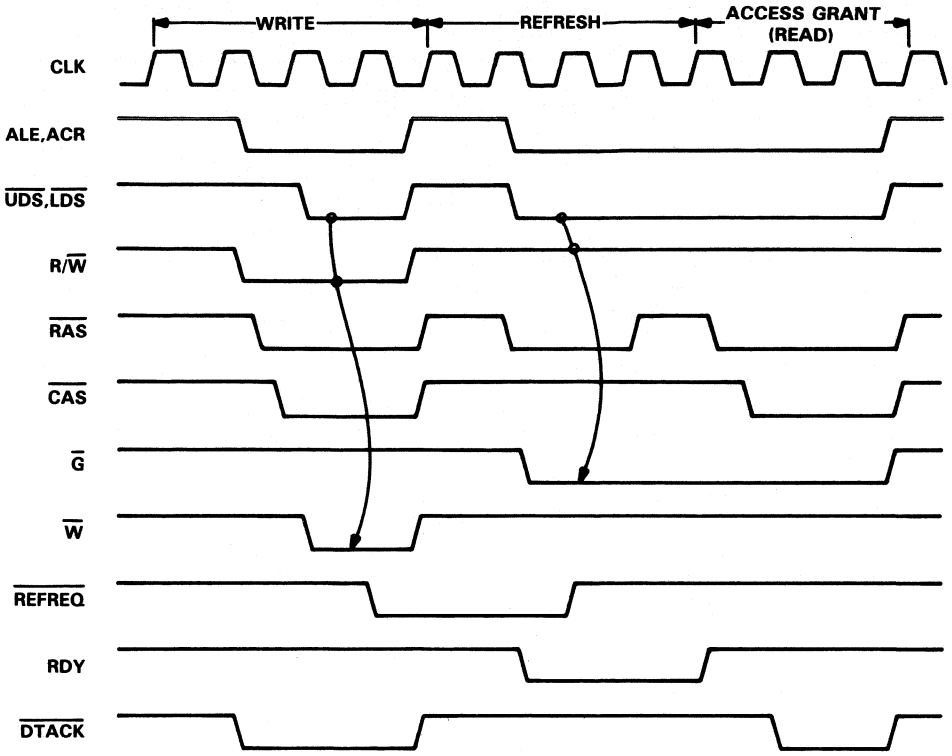


FIGURE 2B – TIMING DIAGRAM (GATED R/W)

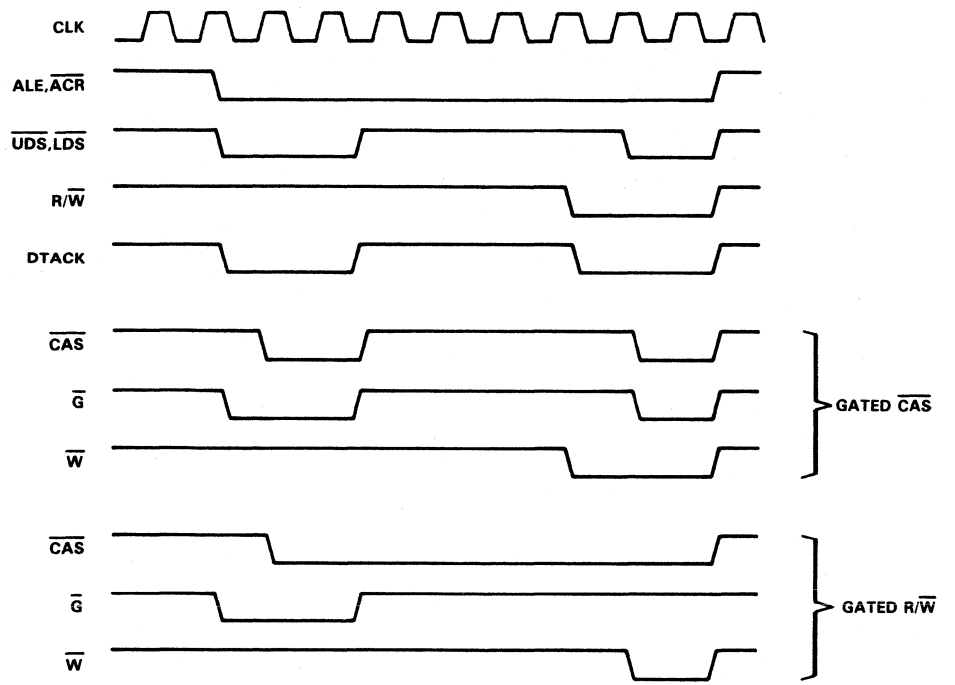


FIGURE 3 – READ-MODIFY-WRITE CYCLE TIMING

To cover the important aspects of the MC68000/TMS4500A interface, detailed calculations of the design criteria for the MC68000L6 and MC68000L10 will be given with only a short summary of the MC68000L8 design criteria. The results will then be compared with the TMS4416 and TMS4164 DRAM timing requirements to provide proper memory speed selections. Finally the designs will be weighed against each other to point out the strengths and weaknesses as related to system performance.

The six-point criteria will be used as presented in the "TMS4500A Dynamic RAM Controller Users Manual" in the following calculations.

MC68000L6 Design Calculations

1. Refresh interval

The TMS4500A is configured for maximum division of the clock without inserting wait states by strapping TWST, FS1, and FS0 as follows.

TWST = 0, FS1 = 1, FS0 = 1

This strap configuration divides the clock by 61 to yeild a refresh interval of 2.60 ms (see 4500A Spec.).

2. Memory precharge time

The memory precharge time must be calculated for consecutive access, refresh, and access grant cycles to ensure that the minimum $\overline{RAS}$ precharge time is satisfied.

a. Access cycles

The precharge time for access cycles is given by:

$$t_{RP} = t_{SH} - t_{AEH\text{-}REH} - t_{t(REH)} + t_{AEL\text{-}REL}^*$$

where t_{RP} = $\overline{RAS}$ precharge time
t_{SH} = $\overline{AS}$,$\overline{DS}$ width high (MIN MC68000L6 Spec.)
$t_{AEH\text{-}REH}$ = Time delay, ALE high to $\overline{RAS}$ starting high (MAX 4500A-15 Spec.)
$t_{AEL\text{-}REL}^*$ = Time delay, ALE low to $\overline{RAS}$ starting low (MAX 4500A-15 Spec.)

thus, $t_{RP} = (180 - 25 - 15 + 27)$ ns
$= 167$ ns

b. Refresh cycles

The minimum precharge time for refresh cycles is given by:

$$t_{RP} = 1.5(T) - t_{CLSH} - t_{AEH\text{-}REH} - t_{t(REH)} + t_{CH\text{-}RRL}^*$$

where T = Clock cycle time
t_{CLSH} = Clock low to $\overline{AS}$, $\overline{DS}$ high (MAX MC68000L6 Spec.)
$t_{CH\text{-}RRL}^*$ = Time delay, CLK high to refresh $\overline{RAS}$ starting low (MAX 4500A-15 Spec.*)

thus, $t_{RP} = [1.5(166) - 75 - 25 - 15 + 45]$ ns
$= 179$ ns

c. Access grant cycles

The precharge time for access grant cycles is given by:

$$t_{RP} = T - t_{CH\text{-}RRH} - t_{t(REH)} + t_{CH\text{-}REL}^*$$

where $t_{CH\text{-}RRH}$ = Time delay, CLK high to refresh $\overline{RAS}$ starting high (MAX 4500A-15 Spec.)

$t_{CH\text{-}REL}^*$ = Time delay, CLK high to access $\overline{RAS}$ starting low (MAX 4500A-15 Spec.*)

thus, $t_{RP} = (166 - 35 - 15 + 54)$ ns
$= 170$ ns

3. ALE to CLK relationship

The ALE low transition must not occur within 10 ns of the CLK low transition.

ALE low to CLK low time is given by:

$$t_{AEL\text{-}CL} = .5(T) - t_{CHSLx}$$

where t_{CHSLx} = Clock high to $\overline{AS}$, $\overline{DS}$ low (MAX, MC68000L6 Spec.)

thus $t_{AEL\text{-}CL} = [.5(166) - 65]$ ns
$= 18$ ns

* This value should otherwise be a minimum; however as all propagation delays on a given chip will tend to track each other, the maximum value is multiplied by a skew factor to reflect variations in same chip propagation delays. The skew factor for the TMS4500A is 0.9. All values followed by an asterisk are obtained by multiplying the specified maximum value by 0.9.

4. Row address setup and hold time

The row address setup time to the TMS4500A is guaranteed by the MC68000L6 address valid to $\overline{AS}$ low timing (t_{AVSL}).

$$t_{AV\text{-}AEL} = t_{AVSL} = 35 \text{ ns (MIN, MC68000L6 Spec.)}$$

The row address setup time to the DRAMs is given by:

$$t_{ASR} = t_{AVSL} - t_{RAV\text{-}MAV} + t_{AEL\text{-}REL}^{*}$$

where $t_{RAV\text{-}MAV}$ = Time delay, row address valid to memory address valid (MAX 4500A-15 Spec.)

thus, $t_{ASR} = (35 - 40 + 27)$ ns
$= 22$ ns

The row address hold time to the DRAMs is guaranteed by the TMS4500A to meet −20 or faster speed devices.

5. Data valid to write enable

In both circuit configurations, data valid to write low is guaranteed by the MC68000L6. For the circuit in Figure 1A this is accomplished by gating $\overline{CAS}$ with $\overline{UDS}$ and $\overline{LDS}$ to give an early write condition. For the circuit in Figure 2A R/$\overline{W}$ is gated with $\overline{UDS}$ and $\overline{LDS}$ to give a late write condition. Data valid to write enable for both circuits is given by:

$$t_{DS} = t_{DOSL} + t_{P32}$$

where t_{DS} = Data setup time
t_{DOSL} = Data out valid to $\overline{DS}$ low (MIN, MC68000L6 Spec.)
t_{P32} = Propagation delay (MIN, 74LS32 Spec.)

Thus $t_{DS} = (35 + 8)$ ns
$= 43$ ns

6. Read access time from $\overline{CAS}$

The required access time for both access and access grant memory cycles must be calculated.

The read access time from $\overline{CAS}$ on normal access cycles for the gated R/$\overline{W}$ configuration (Figure 2A) is given by:

$$t_{CAC} = 2.5(T) - t_{CHSLx} - t_{AEL\text{-}CEL} - t_{t(CEL)} - t_{DICL}$$

where t_{CAC} = Access time from $\overline{CAS}$
$t_{AEL\text{-}CEL}$ = Time delay, ALE low to $\overline{CAS}$ starting low (MAX 4500A-15 Spec.)
$t_{t(CEL)}$ = $\overline{CAS}$ fall time (MAX 4500A-15 Spec.)
t_{DICL} = Data in to clock low (MIN, MC68000L6 Spec.)

thus, $t_{CAC} = [2.5(166) - 65 - 150 - 15 - 25]$ ns
$= 160$ ns

The read access time on access grant cycles for the gated R/$\overline{W}$ configuration (Figure 2A) is given by:

$$t_{CAC} = 2.5(T) - t_{CH\text{-}CEL} - t_{t(CEL)} - t_{DICL}$$

where $t_{CH\text{-}CEL}$ = Time delay, CLK high to access $\overline{CAS}$ starting low (MAX 4500A-15 Spec.)

thus t_{CAC} = [2.5(166) − 140 − 15 − 25] ns
= 235 ns

For the gated $\overline{CAS}$ configuration one SSI gate (74LS32) delay must be subtracted from the above values.

MC68000L10 Design Calculations

The MC68000L8/L10 design requires extra hardware to meet the TMS4500A ALE to CLK low timings (t_{CL-AEL}, t_{AEL-CL}) and DRAM $\overline{CAS}$ access time (t_{CAC}). This is accomplished by providing two clocks (CLK, ϕ) which are approximately 90° out of phase with each other (See Figure 4B). The ϕ clock controls the low going edges of ALE and $\overline{DTACK}$ to ensure proper timing for both the TMS4500A and DRAM. The two flip-flops driving CLK ϕ in Figure 4A should be contained within the same package to minimize the skewing between the two outputs. A 74AS832 is used to derive ALE because of its necessary speed advantage over a 74S32. If the two flip-flops are not contained in the same package and a 74AS832 is not used then the MC68000L10 could not meet the $\overline{RAS}$ precharge and $\overline{CAS}$ access times of the TMS4164 or TMS4416. This restriction is not necessary for MC68000L8 operation.

The TMS4500A is strapped for zero wait state operation, with the processor wait state being provided by externally delaying $\overline{DTACK}$. If necessary two processor wait states may be inserted by strapping the TMS4500A for 1 wait state operation.

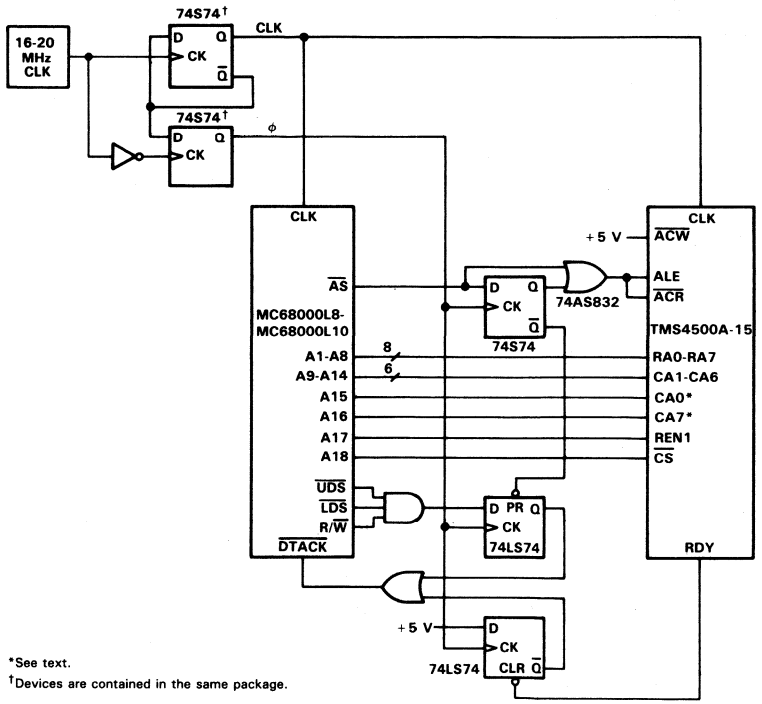


FIGURE 4A – TMS4500A/MC68000L8-MC68000L10 INTERFACE SCHEMATIC

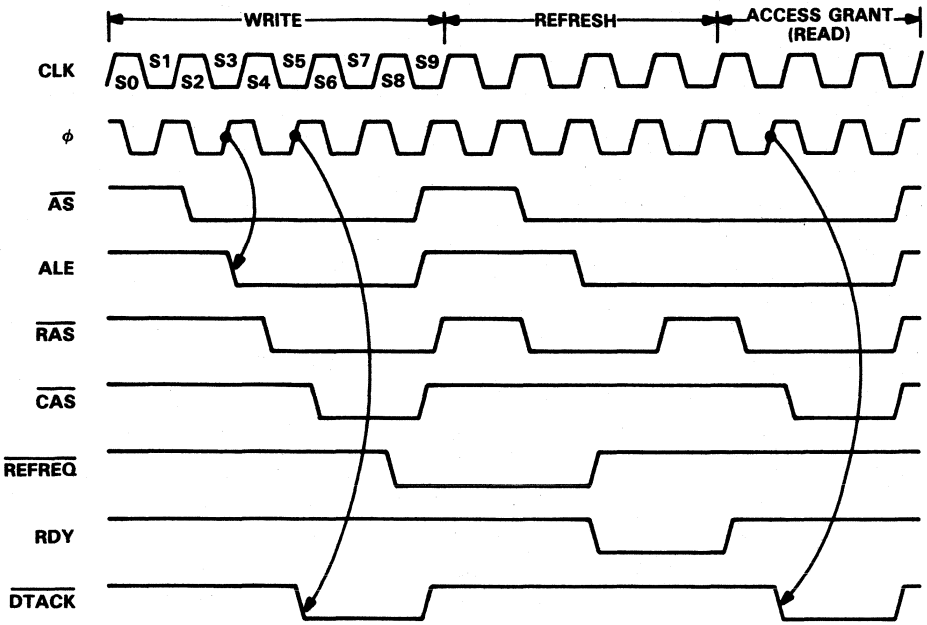


FIGURE 4B – TMS4500A/MC68000L8-MC68000L10 TIMING DIAGRAM

The following calculations reflect gated R/$\overline{W}$ operation.

1. Refresh time

Refresh interval = 1.56 ms

TWST = 0, FS1 = 1, FS0 = 1

2. Memory precharge time

a. Access cycles

$t_{RP} = 2(T) + t_D - t_{CLSH} - t_{P832} - t_{AEH-REH} - t_{tREH} + t_{P74} + t_{AEL-REL}$*

Where t_D = Delay between CLK and φ
t_{P832} = Propagation delay (MAX 74S832 Spec.)
t_{P74} = Propagation delay (MIN 74S74 Spec.)

$t_D = 1/2(t_C) + t_{P04} - t_S$

and t_C = 20 MHz clock cycle time
t_{P04} = Propagation delay (MIN 74S04 Spec.)
t_S = Skew between CLK and φ

thus, $t_D = [1/2(50) + 2 - 1]$ ns
$= 26$ ns

$t_{RP} = [2(100) + 26 - 50 - 5 - 25 - 15 + 4 + 27]$ ns
$= 162$ ns

b. Refresh cycles

$t_{RP} = 1.5(T) - t_{CLSH} - t_{P832} - t_{AEH\text{-}REH} - t_{tREH} + t_{CH\text{-}RRL}$*

$t_{RP} = [1.5(100) - 50 - 5 - 25 - 15 + 45]$ ns
$= 100$ ns

c. Access grant cycles

$t_{RP} = T - t_{CH\text{-}RRH} - t_{tREH} + t_{CH\text{-}REL}$*
$t_{RP} = (100 - 35 - 15 + 54)$ ns
$= 104$ ns

3. ALE to CLK relationship

ALE low is triggered by the rising edge ϕ after $\overline{AS}$ goes low, which exceeds the minimum 10 ns specification.

4. Row address setup and hold time

The row address setup time to the TMS4500A is given by

$t_{AV\text{-}AEL} = T - t_{CLAV} + t_D + t_{P74} + t_{Pmin832}$

where t_{CLAV} = Clock low to address valid (MAX MC68000L10 Spec.)
$t_{Pmin832}$ = Propagation delay (MIN 74AS832 Spec.)
thus $t_{AV\text{-}AEL} = (100 - 55 + 26 + 4 + 1)$ ns
$= 76$ ns

The row address setup time to the DRAM is given by:

$t_{ASR} = T - t_{CLAV} + t_D + t_{P74} + t_{Pmin832} - t_{RAV\text{-}MAV} + t_{AEL\text{-}REL}$*

thus $t_{ASR} = (100 - 55 + 26 + 4 + 1 - 40 + 27)$ ns
$= 63$ ns

5. Data valid to write enable

The data valid to write enable is dependent upon the t_{DOSL} timing of the MC68000 when $\overline{CAS}$ or $\overline{W}$ to the DRAMs is controlled as shown in Figure 1A or Figure 1B.

$t_{DS} = t_{DOSL} + t_{P32}$

thus $t_{DS} = (20 + 8)$ ns
$= 28$ ns

6. Read access time from $\overline{CAS}$

The read access time from $\overline{CAS}$ on normal access cycles for the gated R/$\overline{W}$ configuration is given by:

$t_{CAC} = 3.5\ (T) - 1/2(T) - t_D - t_{P74} - t_{P832} - t_{AEL\text{-}CEL} - t_{t(CEL)} - t_{DICL}$

$t_{CAC} = [3.5(100) - 1/2(100) - 26 - 9 - 5 - 150 - 15 - 15]$ ns
$= 80$ ns

The read access time on access grant cycles for the gated R/$\overline{W}$ configuration is given by:

$t_{CAC} = 2.5(T) - t_{CH-CEL} - t_{t(CEL)} - t_{DICL}$

$t_{CAC} = 2.5(100) - 140 - 15 - 15)$ ns
$= 80$ ns

MC68000L8 Design Calculations Results

The results for the calculations of the design criteria for the MC68000LS are given in Table 1.

TABLE 1 – MC68000LS DESIGN CRITERIA SUMMARY

DESIGN CRITERIA	MC68000L8
1. Refresh interval	1.95 ms
2. Memory precharge time	
a. Access cycles (t_{RP})	203 ns
b. Refresh cycles (t_{RP})	122 ns
c. Access grant cycles (t_{RP})	129 ns
3. ALE to CLK relationship	Guaranteed by clocking $\overline{AS}$ low on the rising edge of ϕ
4. Row address setup and hold times	
a. To the TMS4500A (t_{AV-AEL})	93 ns
b. To the DRAMs (t_{ASR})	79 ns
5. Data valid to write enable (t_{DS})	38 ns
6. Read access time from $\overline{CAS}$	
a. Access cycles (t_{CAC})	149 ns
b. Access grant cycles (t_{CAC})	142 ns

The proper choice of memory can be selected from Table 2 for each design. For the MC68000L6 and MC68000L8 designs there are no memory speed restrictions. However, the MC68000L10 design is restricted to only TMS4416-15 and TMS4164-12 devices; the limiting parameters being $\overline{RAS}$ precharge (t_{RP}) and $\overline{CAS}$ access time (t_{CAC}). To meet slower memory requirements the MC6800L10 clock frequency would have to be reduced. The maximum clock frequency for a desired memory speed can be determined by substituting in the necessary DRAM timing parameters and solving for the input clock period (T) in the design criteria for memory precharge time and read access time.

TABLE 2 – MEMORY SELECTION

MICROPROCESSOR	CLOCK FREQUENCY	MEMORY DEVICES				
		TMS4416		TMS4164		
		-15	-20	-12	-15	-20
MC68000L6	6 MHz	✓	✓	✓	✓	✓
MC68000L8	8 MHz	✓	✓	✓	✓	✓
MC68000L8 (Hybrid)	7.46 MHz	✓	✓	✓	✓	
MC68000L10	10 MHz	✓		✓		

Meeting DRAM timing requirements is only a small part of microprocessor system design. The ultimate goal is to achieve maximum performance with minimum hardware. Of the three designs the MC68000L6 interface requires the least amount of hardware while the MC68000L10 interface has the fastest processor/memory cycle time. To capitalize on the best of both designs a compromise can be made by substituting a MC68000L8 into the MC68000L6 design and operating at less than 8MHz without wait states. Operating under these conditions it can be shown that the processor/memory cycle time approaches that of the MC68000L10 design with a minimum hardware interface (see Table 3).

TABLE 3 – MICROPROCESSOR TO MEMORY CYCLE TIME*

MICROPROCESSOR	CLOCK		CYCLE TIME (t_C)	NUMBER OF WAIT STATES INSERTED (N)
	FREQUENCY	PERIOD		
MC68000L6	6 MHz	166 ns	664 ns	0
MC68000L8	8 MHz	125 ns	625 ns	1
MC68000L8 (Hybrid)	7.46 MHz	134 ns	536 ns	0
MC68000L10	10 MHz	100 ns	500 ns	1

*t_C = 4 (T) + N(T)
where T = microprocessor clock period
N = number of wait states inserted.

To determine the maximum speed that the MC68000L8 can operate without wait states it is necessary to recalculate the design criteria using the MC68000L6 equations with MC68000L8 timing parameters (results in Table 4). From these values the restricting parameter will be the ALE to CLK low timing (minimum 10 ns) requirement necessary for proper TMS4500A operation. Setting $t_{CL\text{-}AEL}$ equal to 12 ns (12 ns allows for 20% margin) and solving for T, yields a clock period of 134 ns (7.46 MHz) The design criteria for 7.46 MHz operation is also shown in Table 4. This "Hybrid" circuit meets TMS4416-15,-20 and TMS4164-12,-15 timing requirements and has a processor/memory cycle time approaching that of the MC68000L10 design. This illustration shows the advantage of operating without wait states when accessing DRAM, but does not directly reflect system throughput enhancement.

System throughput calculations require a much more detailed analysis taking into consideration the systems application, use of other types of memory (EPROM, PROM, ROM, and Statics), memory size and configuration, software, etc. It is beyond the scope of this application note to cover all of these variables in detail, although a brief overview can be given.

TABLE 4 – MC68000L8 (HYBRID) DESIGN CRITERIA SUMMARY*

DESIGN CRITERIA	MICROPROCESSOR	
	MC68000L8 @ 6 MHz	MC68000L8 @ 7.46 MHz
1. Refresh interval	1.95 ms	2.09 ms
2. Memory precharge time		
a. Access cycles (t_{RP})	167 ns	146 ns
b. Refresh cycles (t_{RP})	189 ns	141 ns
c. Access grant cycles (t_{RP})	170 ns	138 ns
3. ALE to CLK relationship	28 ns	12 ns
4. Row address setup and hold times		
a. To the TMS4500A ($t_{AV\text{-}AEL}$)	Guaranteed by t_{AVSL}	Guaranteed by t_{AVSL}
b. To the DRAM (t_{ASR})	17 ns	17 ns
5. Data valid to write enable (t_{DS})	38 ns	38 ns
6. Read access time from $\overline{CAS}$		
a. Access cycles (t_{CAC})	180 ns	100 ns
b. Access grant cycles (t_{CAC})	245 ns	165 ns

*Results reflect gated R/$\overline{W}$ operation.

All of the interface examples given in this application note used a tightly coupled processor/memory interface to maximize DRAM performance. The calculations and comparisons for the "Hybrid" circuit only reflect that the processor is executing strictly out of DRAM which is not always the case in many systems. As microprocessor speeds and memory size increase, the benefits of the tightly coupled memory array give way to asynchronous main memory configurations and cache memory

implementations in order to relieve the processor of wait states when accessing memory. Applications Notes SR-1, "An Introduction To Cache Memory Systems And The TMS2150", and DRC-1, "The TMS4500A In An Asynchronous Bus System", address the concepts of cache and asynchronous memory architecture in more detail than given here.

The percentage of time a microprocessor uses for internal operations as opposed to memory accesses is also a factor in determining system throughput when wait states are used. The greater the percentage of time that a microprocessor spends accessing memory with wait states, the greater the throughput degradation. Thus, for systems whose software requires extensive internal processor operations and few memory operations it may be more desirable to operate with wait states as opposed to the "Hybrid" approach. Table 5 gives an example of a few MC68000 instructions and their effect on throughput. The actual average instruction time will be dependent upon the instruction stream being executed, but this example will indicate how wait states affect the processor performance. The multiply and divide instructions which require a large percentage of internal operations make apparent the advantage of higher speed processors when doing extensive numeric processing; however if the memory intensive instructions predominate, the system running without wait states will execute faster even at slower clock frequencies. Systems which execute program mainly out of EPROM, PROM, ROM and Static memory and only use DRAM for data storage may also benefit from the use of the high speed processors. Each of the four designs has its own niche which is based on the necessary system application. Designs that require maximum memory performance and minimum component count may find the Hybrid interface more suitable, while systems requiring maximum processor performance would utilize the MC68000L8/L10 design.

TABLE 5 – AVERAGE INSTRUCTION CYCLE TIME

A. CLOCK CYCLES AND MEMORY CYCLES PER INSTRUCTION

INSTRUCTION	CLOCK CYCLES		MEMORY CYCLES	
	PER INSTRUCTION	TOTAL	PER INSTRUCTION	TOTAL
MOV AN@+	8		2	
MOV AN@–	10		2	
ADD AN@+	12		2	
ADD AN@–	14		2	
CMPI AN@+	12		3	
CMPI AN@–	14		3	
BRA	10		2	
JMP AN@	8		2	
JMP AN@(d)	10	98	2	20
MULS	70	168	1	21

B. AVERAGE CLOCK CYCLES/INSTRUCTION AND AVERAGE MEMORY CYCLES/INSTRUCTION

NUMBER OF INSTRUCTIONS	AVERAGE CLOCK CYCLES/ INSTRUCTION	AVERAGE MEMORY CYCLES/ INSTRUCTION
First nine instructions (excluding MULS)	10.8	2.2
Ten instructions	16.8	2.1

C. AVERAGE INSTRUCTION CYCLE TIME*

MICROPROCESSOR	AVERAGE INSTRUCTION CYCLE TIME	
	FIRST NINE INSTRUCTIONS	TEN INSTRUCTIONS
MC68000L6 (@ 6 MHz, 0 WS†)	1.800 μs	2.8 μs
MC68000L8 (@ 8 MHz, 1 WS)	1.625 μs	2.362 μs
MC68000L8 (Hybrid) (@ 7.46 MHz, 0 WS)	1.340 μs	2.252 μs
MC68000L10 (@ 10 MHz, 1 WS)	1.300 μs	1.890 μs

* Average instruction time = processor clock cycle time X [average clock cycles/instruction + (average memory cycles/instruction X N wait states)]
†WS = wait state.

D. RELATIVE PERFORMANCE

MICROPROCESSOR	RELATIVE PERFORMANCE	
	FIRST NINE INSTRUCTIONS	TEN INSTRUCTIONS
MC68000L6 (@ 6 MHz, 0 WS)	1.0	1.0
MC68000L8 (@ 8 MHz, 1 WS)	1.1	1.15
MC68000L8 (Hybrid) (@ 7.46 MHz, 0 WS)	1.25	1.19
MC68000L10 (@ 10 MHz, 1 WS)	1.27	1.32

As was mentioned earlier in the text, the designs have taken future memory upgradability into account. When 64K × 4 devices become available they will be pin compatible with the 16K × 4 allowing easy memory expansion. The TMS4416 only requires 14 address lines to address its entire memory array (8 rows, 6 columns) thus leaving two unused address inputs to the TMS4500A (CA0, CA7). The TMS4416 uses inputs A1-A6 for its 6 column addresses, disregarding A0, A7 (see TMS4416 spec.). These two unused inputs to the TMS4500A will be needed to complete the address space for the 64K × 4 devices (8 row, 8 column). In Figures 1A and 2A, 14 consecutive address lines are used to address the TMS4416s which provides a linear address space. For 64K × 4 expansion, A15 and A16 of the MC68000 will be connected to CA0 and CA7 of the TMS4500A respectively. This configuration does not provide a linear address range for the 64K × 4 upgrade but, this would be transparent to the microprocessor and not effect system performance.

For the circuits presented the memory upgrade would expand the memory size from 64K bytes to 256K bytes by simply changing devices. If the memory array of TMS4416s was expanded to take full advantage of the TMS4500As drive capability (32 devices), it would provide 256K bytes of memory. This could then be upgraded to a megabyte of memory by substituting the 64K × 4 devices. Applications Note SMAA001 "TMS4416/TMS4500A Evaluation Board" provides in detail the techniques and advantages of designing for future memory upgradability.

This completes the TMS4500A/MC68000 design requirements. Four MC68000 interfaces were given with two configurations for controlling accesses to upper and lower memory. Two of the designs operate without wait states and two with wait states to illustrate a wide spectrum of operation. The memory was implemented with TMS4416s for their modularity advantage over the X1 DRAMs, and upgradability to future 64K × 4 DRAMs. A brief discussion of the strengths and weaknesses for the four designs was given to provide some insight into the necessary system requirements that need to be considered to achieve maximum system performance for a given application.

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Applications Brief

AN INTRODUCTION TO CACHE MEMORY SYSTEMS AND THE TMS2150

As the typical operating speeds of processors have increased to provide for the ever increasing need for computing power, the necessity of developing a memory hierarchy (the incorporation of two or more memory technologies in the same system) has become apparent. One of these memory technologies is selected on the basis of fast access time (with associated high cost per bit) to allow minimum system cycle time. The other technologies are chosen with the lowest possible cost per bit relative to speed in order to achieve the maximum system memory capacity. In a system with a multiple level hierarchy, the speed/cost relationship depends upon the frequency of access and the total memory requirement at that level. By proper use of this hierarchy through coordination of hardware, system software, and in some cases user software, the overall memory system will reflect the characteristics that approximate the fast access time of the fast memory technology and the low cost per bit of the low cost memory technology. Large computer systems have made use of this memory optimization technique to maintain very large data bases and high throughput (see Figure 1). Many smaller processor systems use this technique to allow mass storage of data, where a tape or disk is the low cost memory and RAM (Random Access Memory) is the fast memory technology.

Memory hierarchy is now extending to the RAM memory used in microcomputer systems because of the increase in processor speeds. Typically, Dynamic RAM (DRAM) is used as the bulk or main memory and High Speed Static RAM (HSS) serves as the fast access memory. This HSS RAM is usually 1K to 8K words deep and serves as a fast buffer memory between the processor and the main memory. This small, fast buffer memory is called "cache" memory as it is the storage location for a carefully selected portion of the data from the main memory. The addresses for that portion of memory currently in the buffer memory is saved in the cache tag RAM (a small memory that is used to store the addresses of the data that has been mapped to cache).

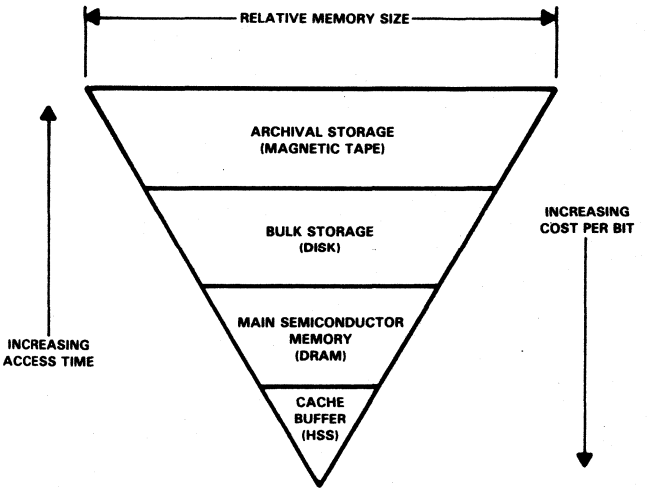


FIGURE 1 – MEMORY SIZE VS. ACCESS TIME AND COST PER BIT

When the processor accesses main memory, the processor address is compared to the addresses currently present in the cache tag RAM. In the case where a match occurs, the required data is resident in the cache and the access is called a "hit," and is completed in the cycle time of the fast memory. If there is no match (a "miss"), the main memory is accessed, and the processor must be delayed to allow for the slower access cycle of the main memory. The determination of whether a hit has occured is the responsibility of the cache tag RAM. Figure 2 shows the relative placement of the processor, main memory, cache, and cache tag RAM within a system.

Since there must be comparisons made between the current processor address and the addresses in the cache, the cache tag RAM must have a very fast access time to prevent the degradation of processor accesses even when a match occurs. Previously, the memory used for the cache tag RAM was the same as that used for the cache; which, due to added delays through comparision logic, meant that the full benefits of the cache were not realized.

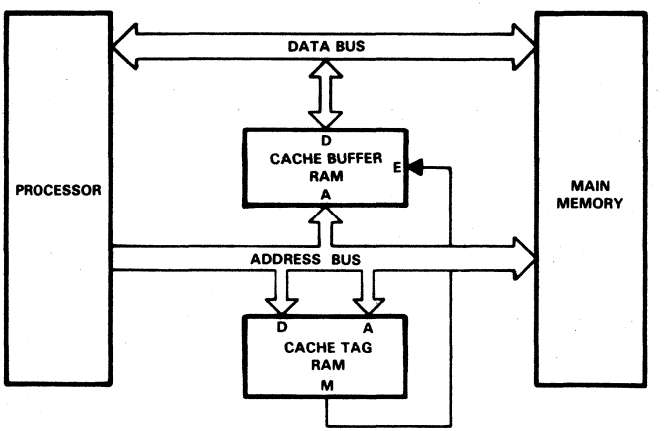
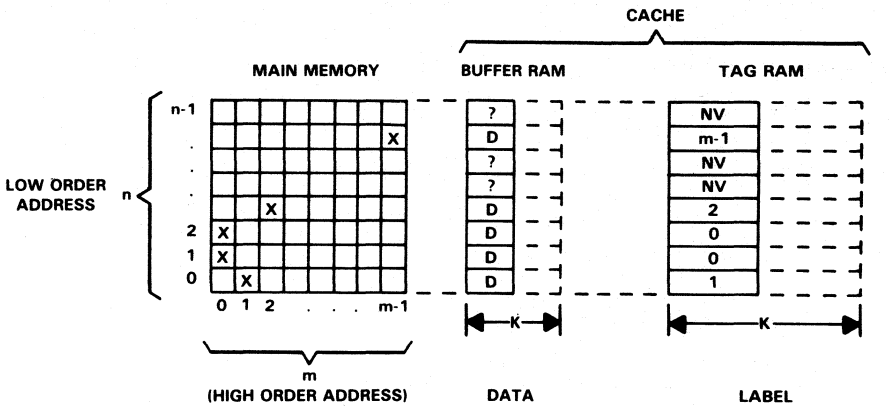


FIGURE 2 – TYPICAL MEMORY SYSTEM WITH CACHE

The TMS2150 Cache Tag RAM has been designed to reduce this cache access degradation to a minimum by incorporating the matching logic on-chip thus providing match recognition times compatible to the access time of the cache buffer memory.

The TMS2150 implements the "set-associative" type of cache address matching. This algorithm may be more clearly understood by considering main memory as an (m) by (n) array of blocks and the cache is an (n) by (k) array (see Figure 3). Each block is composed of (x) words and transfers between main memory and cache memory always move all (x) words in that block. Corresponding to every block in the buffer RAM is a tag address specifying which block of main memory is currently resident in the buffer RAM at that location. The set-associative algorithm maps each modulo (n) group of (m) blocks into the corresponding (n) row of the cache. The low order address lines of the processor covering the sets (n) select a row of the cache buffer and the corresponding row in the tag RAM. The data is stored in the cache buffer and the high order address specifying the block (m) is saved in the tag RAM. The high order address then becomes the tag.



K = Number of BUFFER/TAG groups for multiple cache systems
X = Blocks moved to cache
D = Valid data from main memory
? = Areas of cache that have not been loaded from main memory
NV = Code to indicate non-valid label
0, 1, 2, m-1 = Labels from high order address specifing the block moved from main memory.

FIGURE 3 – SET-ASSOCIATIVE CACHE ADDRESS MATCHING

There are several algorithms used to determine which areas of main memory should be resident in cache and which should be replaced (first-in, first-out; least recently used; or random). Since programs typically have the property of locality (over short periods of time, most accesses are to a small group of memory addresses), these replacement algorithms can make the cache have the majority of processor accesses resulting in hits. The hit ratio (number of hits × 100%/number of memory accesses) runs 90% and higher in systems with well coordinated memory to cache mapping routines. Note that as the block size (x) increases, the replacement mapping algorithm options have greater impact on the cache performance.

Many microprocessors are operating with memory access times of 130 ns or less when running at maximum frequency. After allowing for address buffering, decoding, and propogation delays through data buffers, the maximum access time that can be tolerated is 75 ns or less before processor throughput is affected. For large memory systems, DRAM can be used to achieve a cost effective memory; however these can not meet a 75 ns access requirement. If the actual system throughputs for a system with cache and one without cache are compared, the advantages of cache become obvious.

For comparison of the two architectures, assume that a processor is implemented in which 30% of the active cycles involve main memory (the other 70% used for instruction decoding and internal operations). Also assume that the processor cycles at 250 ns with a required memory access time of 75 ns, but if the memory is not ready the cycle time is extended by 100 ns

increments till satisfied. This processor using 150 ns DRAMs would require one delay increment on main memory accesses and 200 ns DRAMS would require two delay increments. The average cycle time can be calculated for each memory speed as follows:

$$\text{Average Cycle Time} = [(\text{INT}) \times (\text{CYC})] + [(\text{MEM}) \times (\text{CYC} + \text{DEL})]$$

where INT = percent of time doing internal operations
CYC = processor cycle time
MEM = percent of time doing memory accesses
DEL = number of delay increments × 100 ns

For a processor using 150 ns DRAMs:

$$\text{Average Cycle Time} = [(70\%) \times (250 \text{ ns})] + [(30\%) \times (250 + 100)]$$
$$= 280 \text{ ns}$$

For a processor using 200 ns DRAMs:

$$\text{Average Cycle Time} = [(70\%) \times (250 \text{ ns})] + [(30\%) \times (250 + 200)]$$
$$= 310 \text{ ns}$$

For the same system with cache memory assume a 90% hit ratio with 75 ns cache and 200 ns DRAM:

$$\text{Average Cycle Time} = [\text{INT} \times \text{CYC}] + [\text{MEM} \times [(\text{HIT} \times \text{CAC}) + (\text{MIS} \times (\text{CYC} + \text{DEL}))]]$$

where INT = percent of time doing internal operations
CYC = processor cycle time
MEM = percent of time doing memory accesses
DEL = number of delay increments × 100 ns
HIT = percent of memory accesses hit cache
MIS = percent of memory accesses miss cache
CAC = cache memory access cycle time

$$\text{Average Cycle Time} = [70\% \times 250] + [30\% \times [(90\% \times 250) + (10\% \times (250 + 200))]]$$
$$= 253 \text{ ns}$$

This value represents a 10% improvement with 200 ns devices over the non-cache implementation with 150 ns parts and 18% using 200 ns parts. This performance improvement can be further demonstrated for those systems using custom or bit-slice processors where the memory cycle time as well as access time is of concern. For this example, consider a processor with a cycle time of 50 ns and main memory cycle time of 250 ns (use the same access ratios as in the previous example):

$$\text{ACT (Without Cache)} = [(70\%) \times (50)] + [(30\%) \times (250)]$$
$$= 110 \text{ ns}$$

$$\text{ACT (With Cache)} = [70\% \times 50] + [30\% \times [(90\% \times 50) + (10\% \times 250)]$$
$$= 56 \text{ ns}$$

This represents a 49% decrease in average cycle time for the processor using 50 ns cache memory. If the main memory was rated at a cycle time of 500 ns, either using very slow main memory, error detection/correction, or due to allocation of alternate cycles for some other activity (multi-processors, direct memory access, display refresh, etc.); the cache would still give an average cycle time of 63.5 ns, which is an improvement of 65% over the 185 ns average cycle time for a non-cache system.

The following figures show several applications for TMS2150 in cache memory systems. Figure 4 shows a cache memory configuration that has a 32-megaword main memory (represented as 32-megabytes since only an eight-bit data bus is used) with a block size of 2. In this particular example, a cache containing 512-two word blocks was chosen thus defining the main (n)x(m) array as being 512 sets of 32,768-two word blocks. The 32-megaword memory requires an address bus of 25 lines. The least significant address (A0) is used as a word select for one of the two words in each block. The next least significant address lines (A1 — A9) are used as the set select inputs to the cache buffer RAM and the cache tag RAM. The remaining high order address lines (A10 — A24) form the label or tag which is stored and compared by the tag RAM.

Since the label in this example is composed of 15 address lines, two TMS2150s are used as an expanded tag. The 15 address lines are the data inputs to the tag RAM and the 16th data input is tied to +5 V so that after RESET invalid data cannot force a match. The match output of the two TMS2150s are ANDed together to form the enable for the cache data buffer. In this manner, if the contents of either TMS2150 does not contain a match, the cache is not enabled. This ANDed MATCH signal is also used by the control circuitry to notify the system that the address is not present in the cache so that main memory might be accessed. The control circuit is also responsible for the reseting of the cache upon power-up, which is accomplished with a low pulse on the RESET input of the TMS2150. After reset, no matches will occur at any locations until that location has been written.

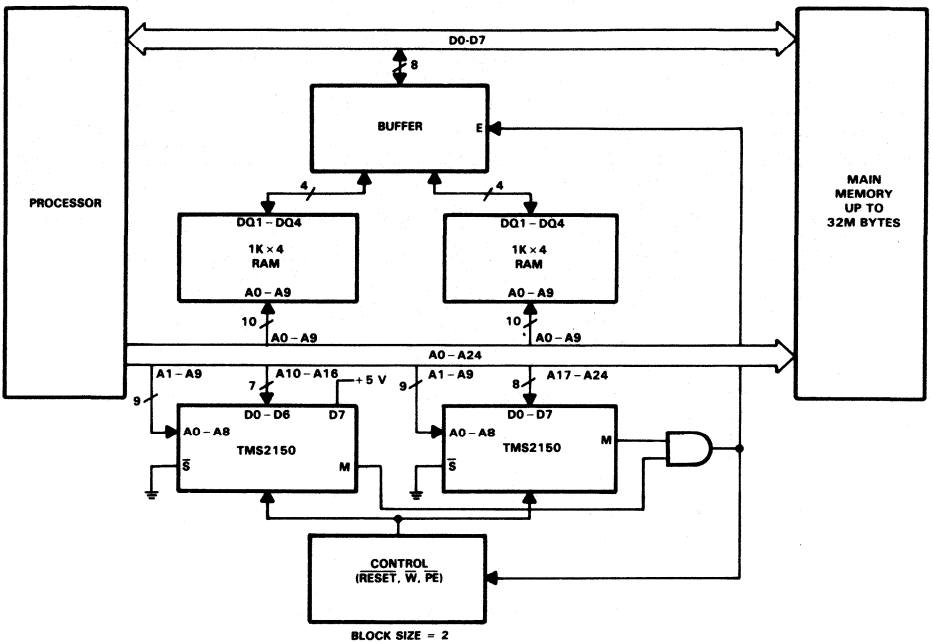


FIGURE 4 – CACHE MEMORY CONFIGURATION

In the example shown in Figure 5, the expansion of the cache RAM is carried out in both depth (more sets) and width (wider tag). The block size has been chosen as one such that the 1K cache now represents 1024 blocks of one word each. The high order addresses are still used as the label to the tag RAM but now A9 is used to select between two TMS2150 pairs each containing labels for 512 of the cache memory blocks. Addresses lines A0 – A8 are thus used as the set address inputs. If the chip select ($\overline{S}$) is at logic one (deselected), the TMS2150 match output (M) is high, so an AND gate can be used to enable the cache data buffers and also to notify the control circuit if access needs to be made into the main memory. The logic for this system is shown so that the upper pair is compared for the first 512 blocks within cache and the lower pair is compared for the second depending on the state of address A9.

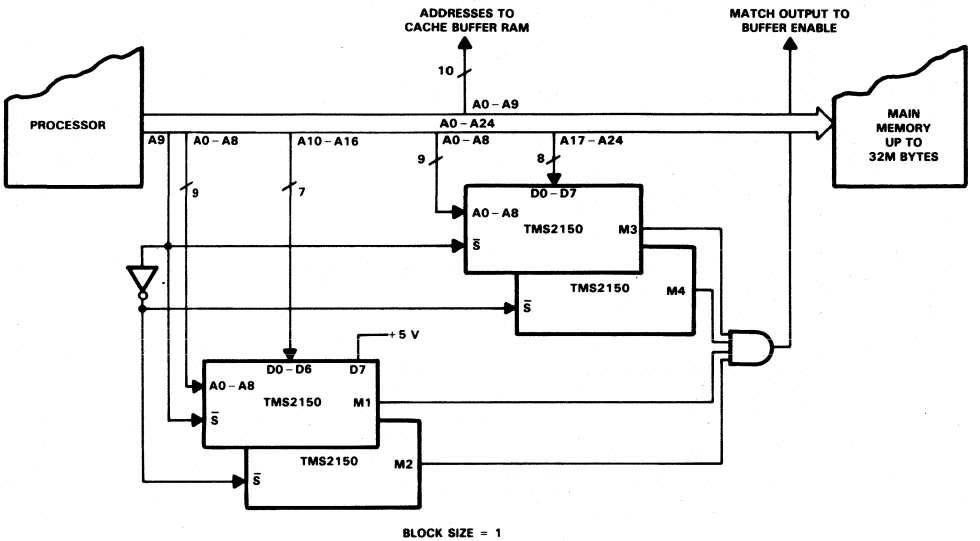


FIGURE 5 – CACHE MEMORY CONFIGURATION

A dual cache structure (K = 2) is shown in Figure 6. The 1 megaword main memory is divided into 1024 sets of 256 four-word blocks. In this example, A0 and A1 are used to select which one of the four words within a block are accessed, and A2 – A10 select which of the 512 block labels are to be compared. Addresses A12 – A19 form the eight-bit label for the block. Address A11 is used by the cache control logic in conjunction with the possible processor status lines as chip select inputs. The match outputs from the two TMS2150s A1 and A2 are NANDed to form an active low enable to the cache data buffers and to serve as request to the control logic. The match outputs from B1 and B2 also are NANDed to perform a similar function for cache RAM B. If no match is found in cache RAM A or B, the control logic will initiate an access from main memory. The purpose of the dual cache architecture is to allow for rapid switching between multiple tasks or programs since the processor can have access to one cache while the controller moves data between main memory and the other cache. The dual or multiple cache approach also yields more replacement options than the single cache architecture. When an access results in a miss in the single cache system, the data in cache is replaced by the current data even though the old data may still be useful. By using "independent" caches, the control can determine which data is most expendible and replace that block while the other caches keep their potentially useful data.

Cache memory architecture can enhance the throughput of many microprocessor systems, allowing large, low-cost memory to perform like high speed RAM. The TMS2150 reduces the tag memory implementation cost and complexity and provides label comparison times comparible to the access times of high-speed memories. These additional benefits make high-performance microprocessor designs that can utilize the same techniques of optimizing cost/memory size/throughput that had previously been found only in larger computer applications.

MOS Memory
Applications Engineering

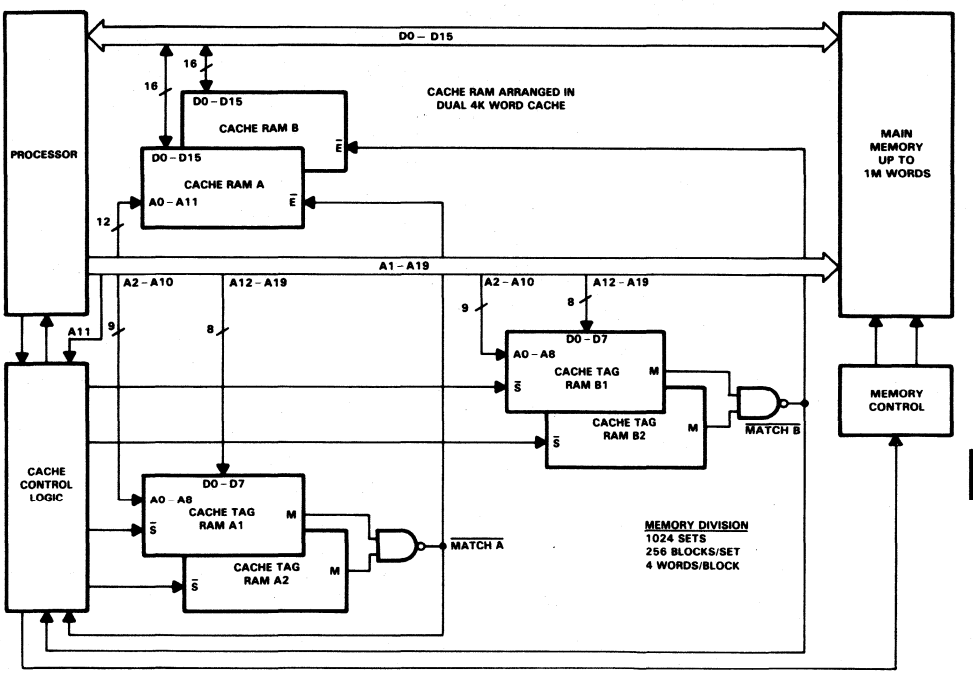


FIGURE 6 – CACHE MEMORY CONFIGURATION: DUAL CACHE (K = 2)

HIGH DENSITY ROMS IN CONSUMER GAME SYSTEMS

This application report will introduce the reader to the options available with the TI high density ROM family. Two chip select options have been implemented for these devices: a standard addressing scheme and a bank select option that divides the device into 8K banks. The bank select versions will allow the higher density ROMs to work with most of the game systems now on the market even though the systems will not directly address 16K of memory.

Most of the game systems on the market use a 74138 one-of-eight decoder to provide the chip select signals. The exceptions to this use a similar method for generating chip selects and this discussion is applicable to them. Since most of the systems used for games do their chip select decoding in 8K byte blocks, the 8K bank select architecture is ideal for systems that have restricted address space.

The bank select ROM (TMS47128) is put into the system with the bank select lines connected to the appropriate system chip select outputs (see Figure 1). These systems will only have one chip select active at a time. If the bank select inputs of the ROM are programmed active low, the device outputs will be tri-stated unless one of the system chip selects is active. This allows the chip selects of the ROM to be tied active and let the bank select inputs control the accessed bank and output impedence. Most of the memory accesses in a game system will be to ROM so having the device active all the time will not significantly increase system current consumption. In fact the system may operate more reliably due to the lack of current spikes caused by powering the ROM on and off.

The limiting factor in most game systems on the market is the lack of ROM address space. By providing a family of high density ROMs with the bank select feature TI has given these games extended capabilities and the software offers the opportunity to write more colorful and complicated programs.

MOS Memory
Applications Engineering

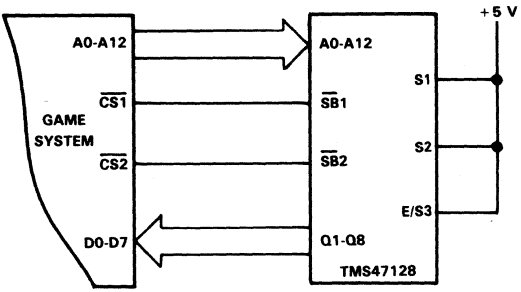


Figure 1. Game System/TMS47128 Interface

EXPLANATION OF NEW LOGIC SYMBOLS FOR MEMORIES

1. INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be partially explained below.

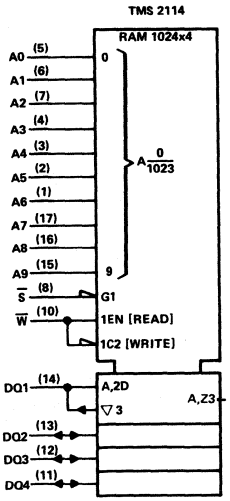
The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

Internationally, IEC Technical Committee TC-3 has prepared a new document (Publication 617-12) that will consolidate the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 has revised the publication IEEE Std 91/ANSI Y32.14. Texas Instruments participated in the work of both organizations and this 1984 Edition of the MOS Memory Data Book introduces new logic symbols in anticipation of the new standards. When changes are made as the standards develop, future editions of this book will take those changes into account.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will finally contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book.

2. EXPLANATION OF A TYPICAL SYMBOL FOR A STATIC MEMORY

The TMS 2114 symbol will be explained in detail. This symbol includes almost all the features found in the others. Section 4, Diagramatic Summary, should be referred to while reading this explanation.



By convention all input lines are located on the left and output lines are located on the right. When an exception is made, an arrowhead shows reverse signal flow. The input/output lines (DQ1 through DQ4) illustrate this.

The polarity indicator ◺ indicates that the external low level causes the internal 1 state (the active state) at an input or that the internal 1 state causes the external low level at an output. The effect is similar to specifying positive logic and using the negation symbol o .

The rest of this discussion concerns features inside the symbol outline. The address inputs are arranged in the order of their assigned binary weights and the range of the addresses are shown as A $\frac{m}{n}$ where m is the decimal equivalent of the lowest address and n is the highest. The inputs and outputs affected by these addresses are designated by the letter A.

The letter Z followed by a number is used to transfer a signal from one point in a symbol to another. Here the signal at output A,Z3 transfers to the 3 at the left side of the symbol in order to form an input/output port. The A means the output comes from the storage location selected by the address inputs.

The ▽ symbol designates a three-state output. Three-state outputs will always be controlled by an EN function. When EN stands at its internal 1 state, the outputs are enabled. When EN stands at its internal 0 state, the three-state outputs stand at their high-impedance states.

Since the boxes associated with DQ2, DQ3, and DQ4 have no internal qualifying symbols, it is to be understood that these boxes are identical to the box associated with DQ1.

Any D input is associated with storage. Whatever internal state is taken on by the D input is stored. The letter A (in A,Z3) indicates that the state of the D input will be stored in a cell selected by the A inputs. If the D input is disabled, the storage element retains its content.

Various types of relationships between ports can be indicated by what is called dependency notation. A letter indicating the type of dependency (e.g., C, G, Z) is placed at the affecting input (or output) and this is followed by a number. Each affected input (or output) is labeled with that same number. The Z symbol explained above is one form of dependency notation. Several other types of dependency have been defined but their use has not been anticipated in this book.

The numeral 2 at the D input indicates that the D input is affected by another input, in this case a C input (i.e., 1C2). When a C input stands at its internal 1 state, it enables the affected D input(s). When the C input stands at its internal 0 state, it disables the D input(s) so that it (they) can no longer alter the contents of the storage element(s).

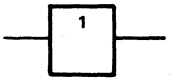
The C input is itself affected by another input. The numeral 1 in front of the C shows that a dependency relationship exists with a G input. The letter G indicates an AND relationship. When a G input stands at its internal 1 state (low in this case), the affected inputs (EN and C2 here) are enabled. When the G input stands at its internal 0 state, it imposes the 0 state on the affected inputs.

Pin 10 has two functions. Its function as a C input has just been explained. Note that for the C input function to stand at its 1 state, pin 10 must be low and pin 8 must also be low. The other function of pin 10 is as an EN input. This controls the 3-state outputs. This EN input is also affected by the AND relationship with pin 8 so for the EN function to stand at its internal 1 state (enabling the outputs), pin 10 must be high and pin 8 must be low.

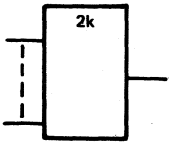
Labels within square brackets are merely supplementary and should be self-explanatory.

3. CACHE ADDRESS COMPARATOR

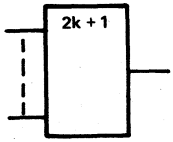
The block diagram for the TMS 2150 uses the RAM symbol (explained in Section 2) and also the following:



Buffer without special amplification. If special amplification is included, the numeral 1 is replaced by ▷.



Even-parity element. The output stands at its 1-state if an even number of inputs stand at their 1-states.

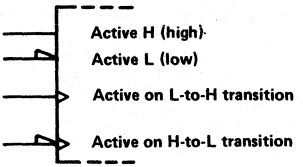


Odd-parity element. The output stands at its 1-state if an odd number of inputs stand at their 1-states.

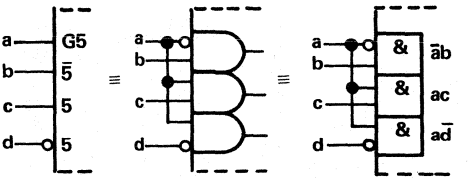
NOTE: TMS 2150 uses one of these to generate even parity by adding the output as a ninth bit.

4. DIAGRAMATIC SUMMARY

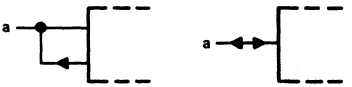
INPUTS



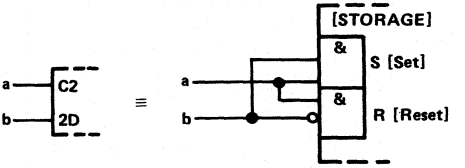
G (AND) DEPENDENCY



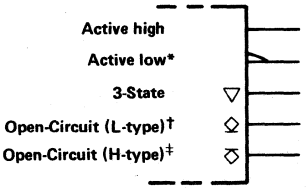
INPUT/OUTPUT



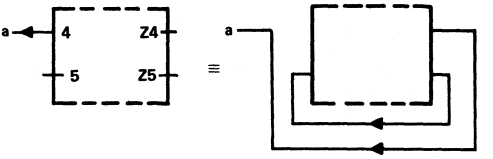
C (CONTROL) DEPENDENCY



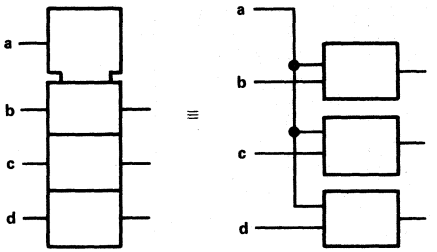
OUTPUTS



Z (INTERCONNECTION) DEPENDENCY



COMMON CONTROL BLOCK



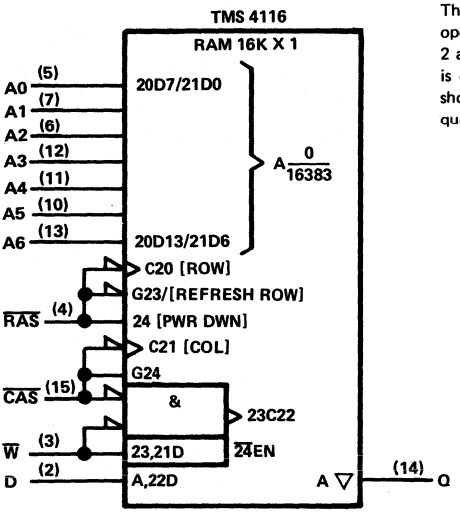
* The active-low indicator may be used in combination with the 3-state and open-circuit indicators.

† L-types include N-channel open-drain and P-channel open-source outputs.

‡ H-types include P-channel open-drain and N-channel open-source outputs.

5. EXPLANATION OF A TYPICAL SYMBOL FOR A DYNAMIC MEMORY

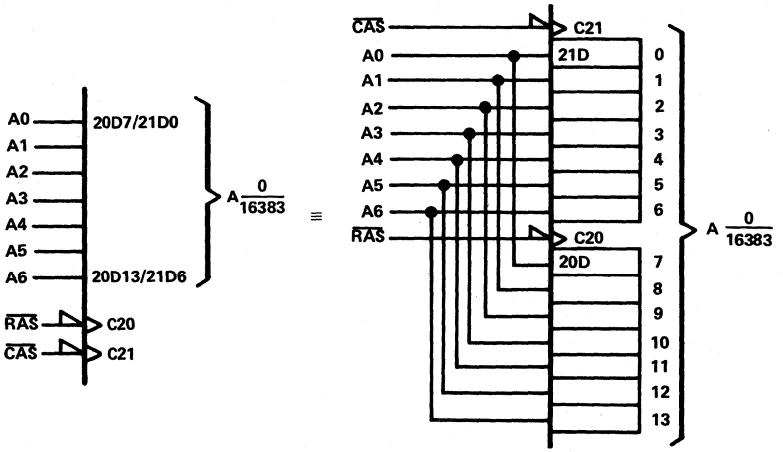
5.1 THE TMS 4116 SYMBOL



The TMS 4116 symbol will be explained in detail for each operating function. The assumption is made that Sections 2 and 4 have been read and understood. While this symbol is complex, so is the device it represents and the symbol shows how the part will perform depending on the sequence in which signals are applied.

5.2 ADDRESSING

The symbol above makes use of an abbreviated form to show the multiplexed, latched addresses. The blocks representing the address latches are implied but not shown.

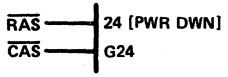


When $\overline{RAS}$ goes low, it momentarily enables (through C20, ▷ indicates a dynamic input) the D inputs of the seven address registers 7 through 13. When $\overline{CAS}$ goes low, it momentarily enables (through C21) the D inputs of the seven address registers 0 through 6. The outputs of the address registers are the 14 internal address lines that select 1 of 16,384 cells.

5.3 REFRESH

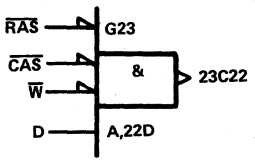
When $\overline{RAS}$ goes low, row refresh starts. It ends when $\overline{RAS}$ goes high. The other input signals required to carry out refreshing are not indicated by the symbol.

5.4 POWER DOWN



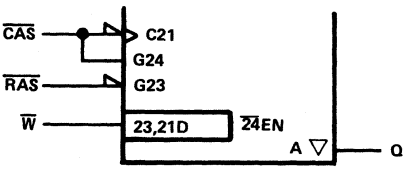
$\overline{CAS}$ is AND'ed with $\overline{RAS}$ (through G24) so when $\overline{RAS}$ and $\overline{CAS}$ are both high, the device is powered down.

5.5 WRITE



By virtue of the AND relationship between $\overline{CAS}$ and $\overline{W}$ (explicitly shown), when either one of these inputs goes low with the other one and $\overline{RAS}$ already low ($\overline{RAS}$ is AND'ed by G23), the D input is momentarily enabled (through C22). In an "early-write" cycle it is $\overline{W}$ that goes low first; this causes the output to remain off as explained below.

5.6 READ



The AND'ed result of $\overline{RAS}$ and $\overline{W}$ (produced by G23) is clocked into a latch (through C21) at the instant $\overline{CAS}$ goes low. This result will be a "1" if $\overline{RAS}$ is low and $\overline{W}$ is high. The complement of $\overline{CAS}$ is shown to be AND'ed with the output of the latch (by G24 and $\overline{24}$). Therefore, as long as $\overline{CAS}$ stays low, the output is enabled. In the "early-write" cycle referred to above, a "0" was stored in the latch by $\overline{W}$ being low when $\overline{CAS}$ went low, so the output remained disabled.

If you have questions on this Explanation of New Logic Symbols, please contact:

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IEEE Standards may be purchased from:

Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

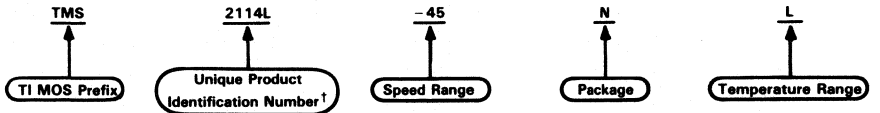
American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

general

Electrical characteristics presented in this catalog, unless otherwise noted, apply to device type(s) listed in the page heading, regardless of package. Factory orders for devices described should include the complete part-type numbers listed on each page.

MOS NUMBERING SYSTEM

EXAMPLE:



TMS Commercial MOS
SMJ Military MOS

Max Access		Package	Temperature Range
-4	45 ns, -20 200 ns	FP Plastic Chip Carrier	E -40°C to 80°C
-5	55 ns, -25 250 ns	J Cerpak/Cerdip	L 0°C to 70°C
-7	70 ns, -30 300 ns	JD Side Braze	M -55°C to 125°C
-10	100 ns, -35 350 ns	MC Chip-on-Board	S -55°C to 100°C
-12	120 ns, -45 450 ns	N Plastic DIP	
-15	150 ns		

† Inclusion of an "L" in the product identification indicates the device operates at low power.

manufacturing information

Die-attach is by standard gold silicon eutectic or by conductive polymer.

Thermal compression gold wire bonding is used on plastic packaged circuits. Typical bond strength is 5 grams. Bond strength is monitored on a lot-to-lot basis. Any preseal bond strength of less than 2 grams causes rejection of the entire lot of devices. On hermetic devices either thermal compression or ultrasonic wire bonding is used. All hermetic MOS LSI devices produced by TI are capable of withstanding 5×10^{-7} atm cc/sec inspection any may be screened to 5×10^{-8} atm cc/sec fine leak, if desired by the customer, for special applications.

All packages are capable of withstanding a shock of 3000 g. All packages are capable of passing a 20,000 g acceleration (centrifuge) test in the Y-axis. Pin strength is measured by a pin-shearing test. All pins are able to withstand the application of a force of 6 pounds at 45° in the peel-off direction.

dual-in-line packages

A pin-to-pin spacing of 2.54 mm (100 mils) has been selected for standard dual-in-line packages (both plastic and ceramic).

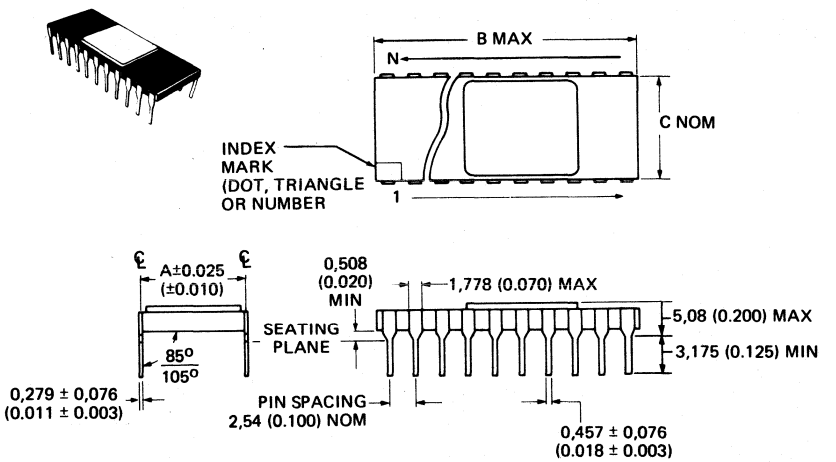
TI uses three types of hermetically sealed ceramic dual-in-line packages: cerdip, cerpak, and sidebrazed. The cerdip and cerpak packages have tin-plated leads. The sidebraze package has gold-plated leads. The plastic package may have tin-plated leads, 60/40 solder-plated leads, or 60/40 hot-solder-dipped-finished-leads.

chip-on-board

TI will bond some MOS memory circuits (particularly ROMs) directly to a printed circuit board specified by the customer. This custom packaging technique for consumer applications utilizes a plastic sealant molded over the silicon directly mounted and ultrasonic wire bonded to a printed circuit board. Board material as well as dimensions are specified by the customer.

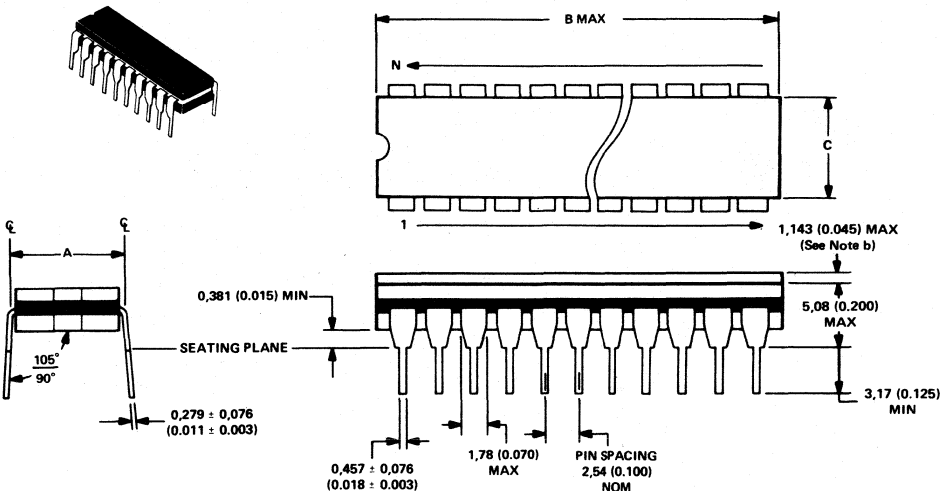
All measurements are given using both metric and English systems. Under the metric system, the measurements are given in millimeters; under the English system, the measurements are given in inches. The English system measurements are indicated in parentheses next to the metric.

ceramic packages — side braze (JD suffix)



DIM. \ PINS	16	18	20	22	24	24	28	40
A ± 0,025 (±0.010)	7,62 (0.300)	7,62 (0.300)	7,62 (0.300)	10,16 (0.400)	7,62 (0.300)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)
B(MAX)	20,57 (0.810)	23,11 (0.910)	25,65 (1.010)	27,94 (1.100)	30,86 (1.215)	32,77 (1.290)	35,94 (1.415)	51,31 (2.020)
C(NOM)	7,493 (0.295)	7,493 (0.295)	7,493 (0.295)	10,03 (0.395)	7,493 (0.295)	15,11 (0.595)	15,11 (0.595)	15,11 (0.595)

ceramic packages – cerdip/300 mil cerpak (J suffix)

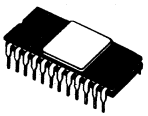


DIM. \ PINS	16*	18	20	24
A(MAX)	8,255 (0.325)	8,255 (0.325)	8,255 (0.325)	8,255 (0.325)
B(MAX)	19,56 (0.770)	22,86 (0.900)	24,38 (0.960)	32,00 (1.260)
C(MAX)	7,645 (0.301)	7,645 (0.301)	7,645 (0.301)	7,645 (0.301)

* Dimensions A, B, and C are applicable for both 16-pin cerdip and cerpak.

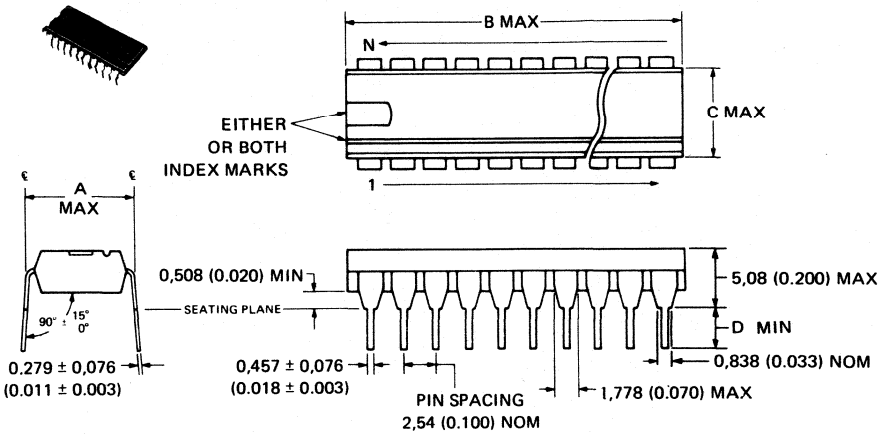
NOTES: a. All dimensions are shown in millimeters and parenthetically in inches. Millimeter dimensions govern.
b. Cerpak only.

ceramic packages — 600 mil cerpak (J suffix)



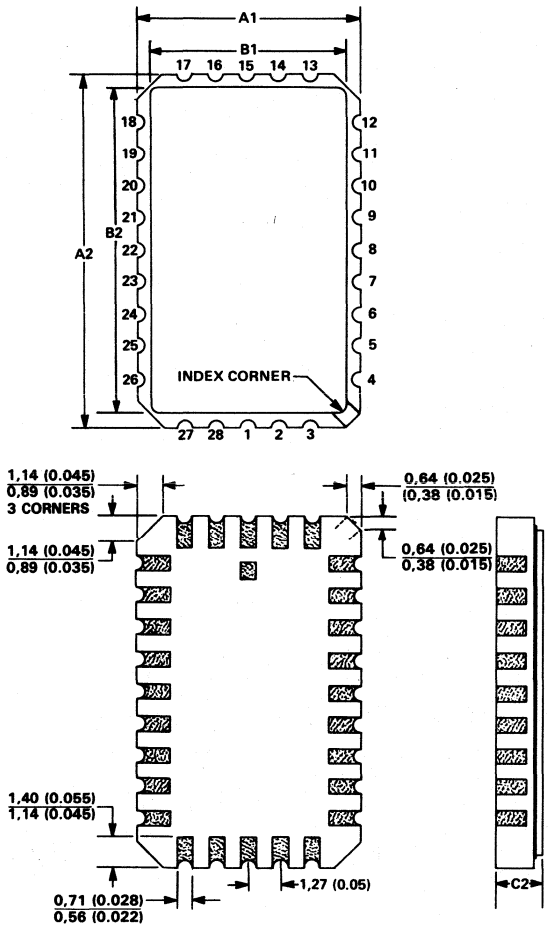
DIM. \ PINS	24	28
A (MAX)	15,88 (0.625)	15,88 (0.625)
B (MAX)	32,77 (1.290)	37,85 (1.490)
C (MAX)	15,24 (0.600)	15,24 (0.600)

plastic packages (N suffix)



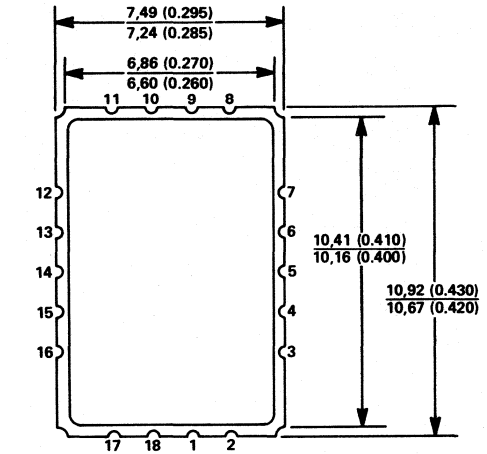
DIM. \ PINS	16	18	20	22	24	28	40
A (MAX)	8,255 (0.325)	8,255 (0.325)	8,255 (0.325)	10,80 (0.425)	15,88 (0.625)	15,88 (0.625)	15,49 (0.61)
B (MAX)	22,1 (0.870)	23,37 (0.920)	27,18 (1.070)	28,45 (1.120)	32,26 (1.270)	36,58 (1.440)	53,1 (2.090)
C (MAX)	6,858 (0.270)	6,858 (0.270)	6,858 (0.270)	9.017 (0.355)	13,97 (0.550)	13,97 (0.550)	13,97 (0.550)
D (MIN)	3,175 (0.125)	3,175 (0.125)	3,175 (0.125)	3,175 (0.125)	2,921 (0.115)	2,921 (0.115)	3,175 (0.125)

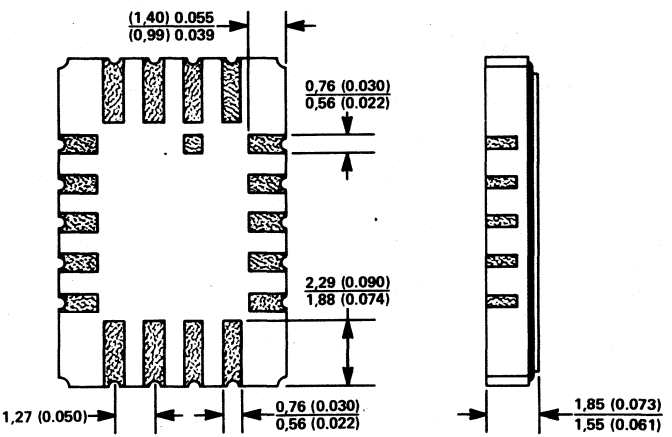
ceramic chip carrier package (FE suffix)



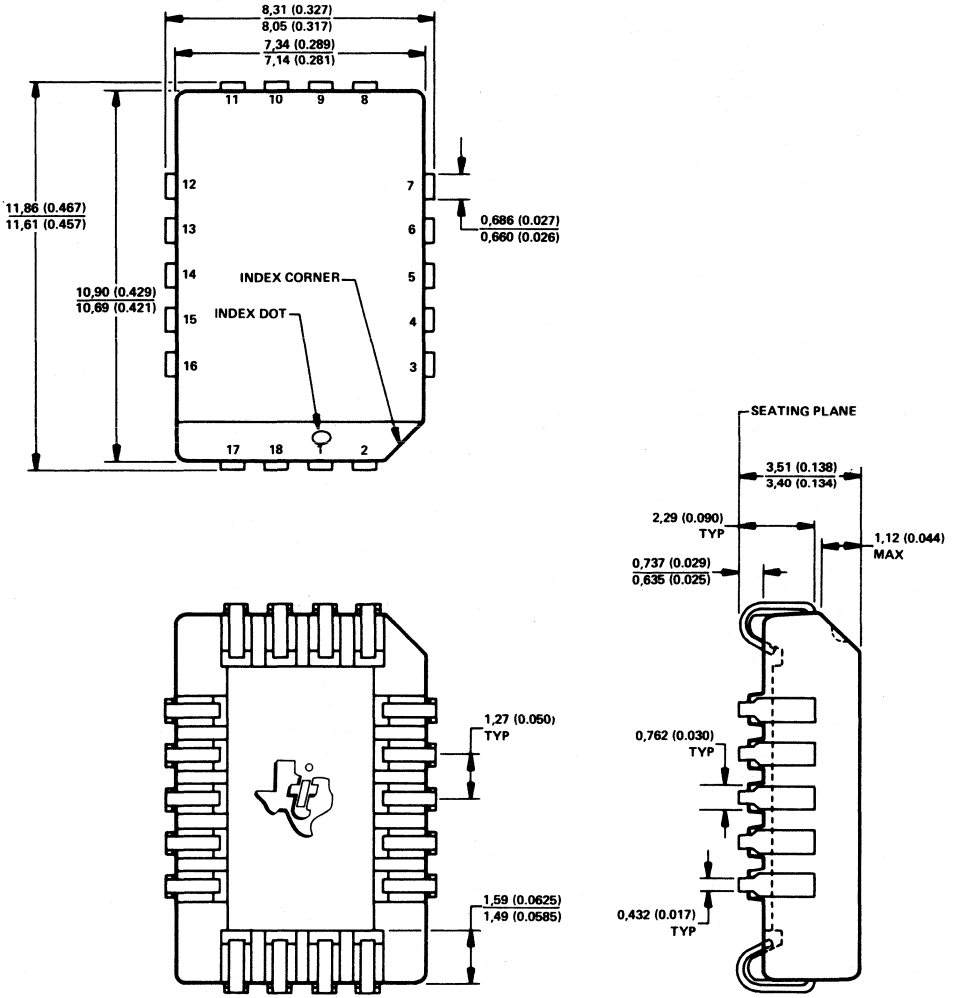
NUMBER OF TERMINALS	A1		A2		B1		B2		C2	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
28	8,76 (0.345)	9,02 (0.355)	13,84 (0.545)	14,10 (0.555)	7,80 (0.307)	7,95 (0.313)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)
32	11,30 (0.445)	11,56 (0.455)	13,84 (0.545)	14,10 (0.555)	10,34 (0.407)	13,03 (0.513)	12,88 (0.507)	13,03 (0.513)	1,65 (0.065)	2,01 (0.079)

ceramic chip carrier package (FG suffix)

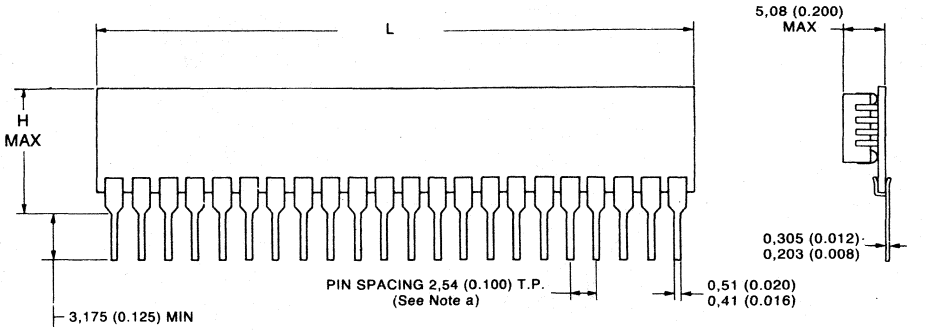




plastic chip carrier package (FP suffix)



single-in-line packages (S I P)



NOTE a. Each pin centerline is located within 0.25 (0.010) of its true longitudinal position.

PACKAGES		L		H MAX
TMXXXX	X A	55.8 (2.2)	X	9.7 (.380)
	C	55.8 (2.2)	X	11.4 (.450)
	D	55.8 (2.2)	X	17.8 (.700)
	E	60.9 (2.4)	X	11.4 (.450)
	F	60.9 (2.4)	X	9.7 (.380)
	G	60.9 (2.4)	X	17.8 (.700)
	H	68.6 (2.7)	X	9.7 (.380)
	L	76.2 (3.0)	X	17.8 (.700)
	M	78.7 (3.1)	X	11.4 (.450)
	N	81.3 (3.2)	X	17.8 (.700)
	P	88.9 (3.5)	X	11.4 (.450)
	Q	69.6 (2.7)	X	11.4 (.450)
	R	68.6 (2.7)	X	11.9 (.470)
	T	76.2 (3.0)	X	11.4 (.450)
	J	76.2 (3.0)	X	9.7 (.380)
	K	76.2 (3.0)	X	17.8 (.700)

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